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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64i-b-5qfn32

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# 1. Feature List

The EFM8BB3 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - · Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 50 MHz maximum operating frequency
- Memory:
  - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- · Power:
  - Internal LDO regulator for CPU core voltage
  - · Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
  - Up to 25 pins 5 V tolerant under bias
  - Selectable state retention through reset events
  - · Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- · Clock Sources:
  - Internal 49 MHz oscillator with accuracy of ±2%
  - Internal 24.5 MHz oscillator with ±2% accuracy
  - · Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
  - External crystal/RC Oscillator (up to 25 MHz)

- Analog:
  - 12/10-Bit Analog-to-Digital Converter (ADC)
  - Internal temperature sensor
  - 4 x 12-Bit Digital-to-Analog Converters (DAC)
  - 2 x Low-current analog comparators with adjustable reference
- · Communications and Digital Peripherals:
  - 2 x UART, up to 3 Mbaud
  - SPI™ Master / Slave, up to 12 Mbps
  - SMBus™/I2C™ Master / Slave, up to 400 kbps
  - I<sup>2</sup>C High-Speed Slave, up to 3.4 Mbps
  - 16-bit CRC unit, supporting automatic CRC of flash at 256byte boundaries
  - 4 Configurable Logic Units
- · Timers/Counters and PWM:
  - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 6 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
  - · Full memory and register inspection
  - · Four hardware breakpoints, single-stepping
- · Pre-programmed UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

## EFM8BB3 Data Sheet Ordering Information

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Voltage DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-B-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F32G-B-QFN32	32	2304	29	2 <sup>1</sup>	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F32G-B-QFP32	32	2304	28	2 <sup>1</sup>	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F32G-B-QFN24	32	2304	20	2 <sup>1</sup>	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F32G-B-QSOP24	32	2304	21	2 <sup>1</sup>	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F16G-B-QFN32	16	2304	29	2 <sup>1</sup>	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F16G-B-QFP32	16	2304	28	2 <sup>1</sup>	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F16G-B-QFN24	16	2304	20	2 <sup>1</sup>	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F16G-B-QSOP24	16	2304	21	2 <sup>1</sup>	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F64I-B-QFN32	64	4352	29	4	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F64I-B-QFP32	64	4352	28	4	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F64I-B-QFN24	64	4352	20	4	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F64I-B-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +125 °C	QSOP24
EFM8BB31F32I-B-QFN32	32	2304	29	2 <sup>1</sup>	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F32I-B-QFP32	32	2304	28	2 <sup>1</sup>	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F32I-B-QFN24	32	2304	20	2 <sup>1</sup>	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F32I-B-QSOP24	32	2304	21	2 <sup>1</sup>	13	6	7	Yes	-40 to +125 °C	QSOP24
EFM8BB31F16I-B-QFN32	16	2304	29	2 <sup>1</sup>	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F16I-B-QFP32	16	2304	28	2 <sup>1</sup>	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F16I-B-QFN24	16	2304	20	2 <sup>1</sup>	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F16I-B-QSOP24	16	2304	21	2 <sup>1</sup>	13	6	7	Yes	-40 to +125 °C	QSOP24
Note:										

1. DAC0 and DAC1 are enabled on devices with 2 DACs available.

#### 3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- · Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to ±2% over supply and temperature corners.
- 49 MHz internal oscillator (HFOSC1), accurate to ±2% over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, CMOS, and high-frequency crystal clock options (EXTCLK).
- · Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
  - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

#### 3.5 Counters/Timers and PWM

#### Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- · Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- · Capture on rising, falling or any edge
- · Compare function for arbitrary waveform generation
- · Software timer (internal compare) mode
- · Can accept hardware "kill" signal from comparator 0 or comparator 1

Device Package	Pin for Bootload Mode Entry
QFN32	P3.7 / C2D
QFP32	P3.7 / C2D
QFN24	P3.0 / C2D
QSOP24	P3.0 / C2D

# Table 3.3. Summary of Pins for Bootload Mode Entry

## 4.1.4 Flash Memory

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Write Time <sup>1,2</sup>	t <sub>WRITE</sub>	One Byte,	19	20	21	μs
		F <sub>SYSCLK</sub> = 24.5 MHz				
Erase Time <sup>1,2</sup>	t <sub>ERASE</sub>	One Page,	5.2	5.35	5.5	ms
		F <sub>SYSCLK</sub> = 24.5 MHz				
V <sub>DD</sub> Voltage During Programming <sup>3</sup>	V <sub>PROG</sub>		2.2	_	3.6	V
Endurance (Write/Erase Cycles)	N <sub>WE</sub>		20k	100k	—	Cycles
CRC Calculation Time	t <sub>CRC</sub>	One 256-Byte Block	_	5.5	_	μs
		SYSCLK = 49 MHz				

## Table 4.4. Flash Memory

## Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.

2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.

3. Flash can be safely programmed at any voltage above the supply monitor threshold (V<sub>VDDM</sub>).

4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

### 4.1.5 Power Management Timing

## Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Тур	Мах	Units
Idle Mode Wake-up Time	t <sub>IDLEWK</sub>		2		3	SYSCLKs
Suspend Mode Wake-up Time	t <sub>SUS-</sub>	SYSCLK = HFOSC0	_	170	_	ns
	PENDWK	CLKDIV = 0x00				
Snooze Mode Wake-up Time	t <sub>SLEEPWK</sub>	SYSCLK = HFOSC0	—	12	—	μs
		CLKDIV = 0x00				

# 4.1.8 Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Crystal Frequency	f <sub>XTAL</sub>		0.02	_	25	MHz
Crystal Drive Current	I <sub>XTAL</sub>	XFCN = 0	—	0.5	—	μA
		XFCN = 1	_	1.5	_	μA
		XFCN = 2	—	4.8	—	μA
		XFCN = 3	_	14	_	μA
		XFCN = 4	_	40	_	μA
		XFCN = 5	—	120	_	μA
		XFCN = 6	_	550	_	μA
		XFCN = 7		2.6		mA

## Table 4.8. Crystal Oscillator

EFM8BB3 Data Sheet Electrical Specifications

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Note: 1. Conversion Time does not inclu	ide Tracking	Time. Total Conversion Time is:				
Total Conversion Time = [RPT where RPT is the number of con 2. Absolute input pin voltage is lim 3. The offset is determined using of positive.	× (ADTK + N nversions re lited by the N curve fitting s	IUMBITS + 1) × T(SARCLK)] + (T(AD presented by the ADRPT field and AD $/_{IO}$ supply. since the specification is measured us	CCLK) × 4) DCCLK is the sing linear se	e clock selec	ted for the A	DC. is always

### 4.1.16 SMBus

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit				
Standard Mode (100 kHz Class)										
I2C Operating Frequency	f <sub>I2C</sub>		0	_	70 <sup>2</sup>	kHz				
SMBus Operating Frequency	f <sub>SMB</sub>		40 <sup>1</sup>	_	70 <sup>2</sup>	kHz				
Bus Free Time Between STOP and START Conditions	t <sub>BUF</sub>		9.4	_	_	μs				
Hold Time After (Repeated) START Condition	t <sub>HD:STA</sub>		4.7	—	_	μs				
Repeated START Condition Setup Time	t <sub>SU:STA</sub>		9.4		_	μs				
STOP Condition Setup Time	t <sub>SU:STO</sub>		9.4	—	_	μs				
Data Hold Time	t <sub>HD:DAT</sub>		0	_	—	μs				
Data Setup Time	t <sub>SU:DAT</sub>		4.7	_	—	μs				
Detect Clock Low Timeout	t <sub>TIMEOUT</sub>		25	_	_	ms				
Clock Low Period	t <sub>LOW</sub>		4.7	_	_	μs				
Clock High Period	tніgн		9.4	_	50 <sup>3</sup>	μs				
Fast Mode (400 kHz Class)										
I2C Operating Frequency	f <sub>I2C</sub>		0	_	256 <sup>2</sup>	kHz				
SMBus Operating Frequency	f <sub>SMB</sub>		40 <sup>1</sup>	_	256 <sup>2</sup>	kHz				
Bus Free Time Between STOP and START Conditions	t <sub>BUF</sub>		2.6		_	μs				
Hold Time After (Repeated) START Condition	t <sub>HD:STA</sub>		1.3	_	_	μs				
Repeated START Condition Setup Time	t <sub>SU:STA</sub>		2.6	_	_	μs				
STOP Condition Setup Time	t <sub>SU:STO</sub>		2.6	_	_	μs				
Data Hold Time	t <sub>HD:DAT</sub>		0	_	—	μs				
Data Setup Time	t <sub>SU:DAT</sub>		1.3	—	—	μs				
Detect Clock Low Timeout	t <sub>TIMEOUT</sub>		25	—	—	ms				
Clock Low Period	t <sub>LOW</sub>		1.3	_	—	μs				
Clock High Period	t <sub>HIGH</sub>		2.6		50 <sup>3</sup>	μs				

## Table 4.16. SMBus Peripheral Timing Performance (Master Mode)

#### Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.

2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.

3. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

#### 4.3 Absolute Maximum Ratings

Stresses above those listed in Table 4.19 Absolute Maximum Ratings on page 32 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

#### Table 4.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T <sub>BIAS</sub>		-55	125	°C
Storage Temperature	T <sub>STG</sub>		-65	150	°C
Voltage on VDD	V <sub>DD</sub>		GND-0.3	4.2	V
Voltage on VIO <sup>2</sup>	V <sub>IO</sub>		GND-0.3	V <sub>DD</sub> +0.3	V
Voltage on I/O pins or RSTb, excluding	V <sub>IN</sub>	V <sub>IO</sub> > 3.3 V	GND-0.3	5.8	V
P3.0-P3.3 (QFN32 and QSOP24) of P3.0-P3.3 (QFN32 and QFP32)		V <sub>IO</sub> < 3.3 V	GND-0.3	V <sub>IO</sub> +2.5	V
Voltage on P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	V <sub>IN</sub>		GND-0.3	V <sub>DD</sub> +0.3	V
Total Current Sunk into Supply Pin	I <sub>VDD</sub>		—	200	mA
Total Current Sourced out of Ground Pin	I <sub>GND</sub>		200	_	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I <sub>IO</sub>		-100	100	mA
Operating Junction Temperature	TJ	T <sub>A</sub> = -40 °C to 85 °C	-40	105	°C
		T <sub>A</sub> = -40 °C to 125 °C (I-grade parts only)	-40	130	°C

#### Note:

1. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.

# 5. Typical Connection Diagrams

### 5.1 Power

Figure 5.1 Power Connection Diagram on page 33 shows a typical connection diagram for the power pins of the device.



Figure 5.1. Power Connection Diagram

Pin	Pin Name	Description	Crossbar Capability	Additional Digital	Analog Functions
Number				Functions	
1	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
2	VIO	I/O Supply Power Input			
3	VDD	Supply Power Input			
4	RSTb /	Active-low Reset /			
	C2CK	C2 Debug Clock			
5	P3.7 /	Multifunction I/O /			
	C2D	C2 Debug Data			
6	P3.4	Multifunction I/O			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19
					CMP1P.8
					CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18
					CMP1P.7
					CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17
					CMP1P.6
					CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.16
				CLU1B.15	CMP1P.5
				CLU2B.15	CMP1N.5
				CLU3A.15	

## Table 6.1. Pin Definitions for EFM8BB3x-QFN32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.15
				CLU2OUT	CMP1P.4
				CLU1A.15	CMP1N.4
				CLU2B.14	
				CLU3A.14	
16	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.14
				I2C0_SCL	CMP1P.3
				CLU1B.14	CMP1N.3
				CLU2A.15	
				CLU3B.15	
17	P2.0	Multifunction I/O	Yes	P2MAT.0	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	
18	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.13
				CLU0B.15	CMP0P.9
				CLU1B.13	CMP0N.9
				CLU2A.13	
19	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.12
				CLU0A.15	
				CLU1B.12	
				CLU2A.12	
20	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.11
				CLU0B.14	
				CLU1A.13	
				CLU2B.13	
21	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.10
				CLU0A.14	
				CLU1A.12	
				CLU2B.12	
22	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.9
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.9	
				CLU3A.9	
31	P0.2	Multifunction I/O	Yes	P0MAT.2	XTAL1
				INT0.2	ADC0.1
				INT1.2	CMP0P.1
				CLU0OUT	CMP0N.1
				CLU0A.9	
				CLU2B.8	
				CLU3A.8	
32	P0.1	Multifunction I/O	Yes	P0MAT.1	ADC0.0
				INT0.1	CMP0P.0
				INT1.1	CMP0N.0
				CLU0B.8	AGND
				CLU2A.9	
				CLU3B.9	

### 7.2 QFN32 PCB Land Pattern



Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2.	QFN32 PCB L	and Pattern	Dimensions
------------	-------------	-------------	------------

Dimension	Min	Мах
C1	_	4.10
C2	—	4.10
X1	—	0.2
X2	_	3.0
Y1	—	0.7
Y2	_	3.0
e	_	0.4

# 8. QFP32 Package Specifications

## 8.1 QFP32 Package Dimensions



Figure 8.1. QFP32 Package Drawing

## Table 8.1. QFP32 Package Dimensions

Dimension	Min	Тур	Мах
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.30	0.37	0.45
с	0.09	_	0.20
D	9.00 BSC		
D1	7.00 BSC		
е	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.50 0.60 0.70		

Dimension	Min	Тур	Мах
ааа		0.20	
bbb		0.20	
ссс		0.10	
ddd		0.20	
theta	0°	3.5°	7°
Note:			

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC outline MS-026.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

#### 8.2 QFP32 PCB Land Pattern



Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2.	QFP32 PCB	Land Pattern	Dimensions
------------	-----------	--------------	------------

Dimension	Min	Мах
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

#### Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

5. The stencil thickness should be 0.125 mm (5 mils).

6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

7. A No-Clean, Type-3 solder paste is recommended.

8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.



Figure 8.3. QFP32 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

#### 9.2 QFN24 PCB Land Pattern



Figure 9.2. QFN24 PCB Land Pattern Drawing

## Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Мах	
C1	3.00		
C2	3.00		
e	0.4 REF		
X1	0.20		
X2	1.80		
Y1	0.80		
Y2	1.80		
Y3	0.4		
f	2.50 REF		
с	0.25	0.35	



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).