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Details

Product Status	Not For New Designs
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UQFN Exposed Pad
Supplier Device Package	32-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64i-b-5qfn32r

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Voltage DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-B-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F32G-B-QFN32	32	2304	29	2 ¹	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F32G-B-QFP32	32	2304	28	2 ¹	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F32G-B-QFN24	32	2304	20	2 ¹	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F32G-B-QSOP24	32	2304	21	2 ¹	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F16G-B-QFN32	16	2304	29	2 ¹	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F16G-B-QFP32	16	2304	28	2 ¹	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F16G-B-QFN24	16	2304	20	2 ¹	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F16G-B-QSOP24	16	2304	21	2 ¹	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F64I-B-QFN32	64	4352	29	4	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F64I-B-QFP32	64	4352	28	4	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F64I-B-QFN24	64	4352	20	4	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F64I-B-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +125 °C	QSOP24
EFM8BB31F32I-B-QFN32	32	2304	29	2 ¹	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F32I-B-QFP32	32	2304	28	2 ¹	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F32I-B-QFN24	32	2304	20	2 ¹	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F32I-B-QSOP24	32	2304	21	2 ¹	13	6	7	Yes	-40 to +125 °C	QSOP24
EFM8BB31F16I-B-QFN32	16	2304	29	2 ¹	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F16I-B-QFP32	16	2304	28	2 ¹	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F16I-B-QFN24	16	2304	20	2 ¹	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F16I-B-QSOP24	16	2304	21	2 ¹	13	6	7	Yes	-40 to +125 °C	QSOP24

Note:

1. DAC0 and DAC1 are enabled on devices with 2 DACs available.

3. System Overview

3.1 Introduction

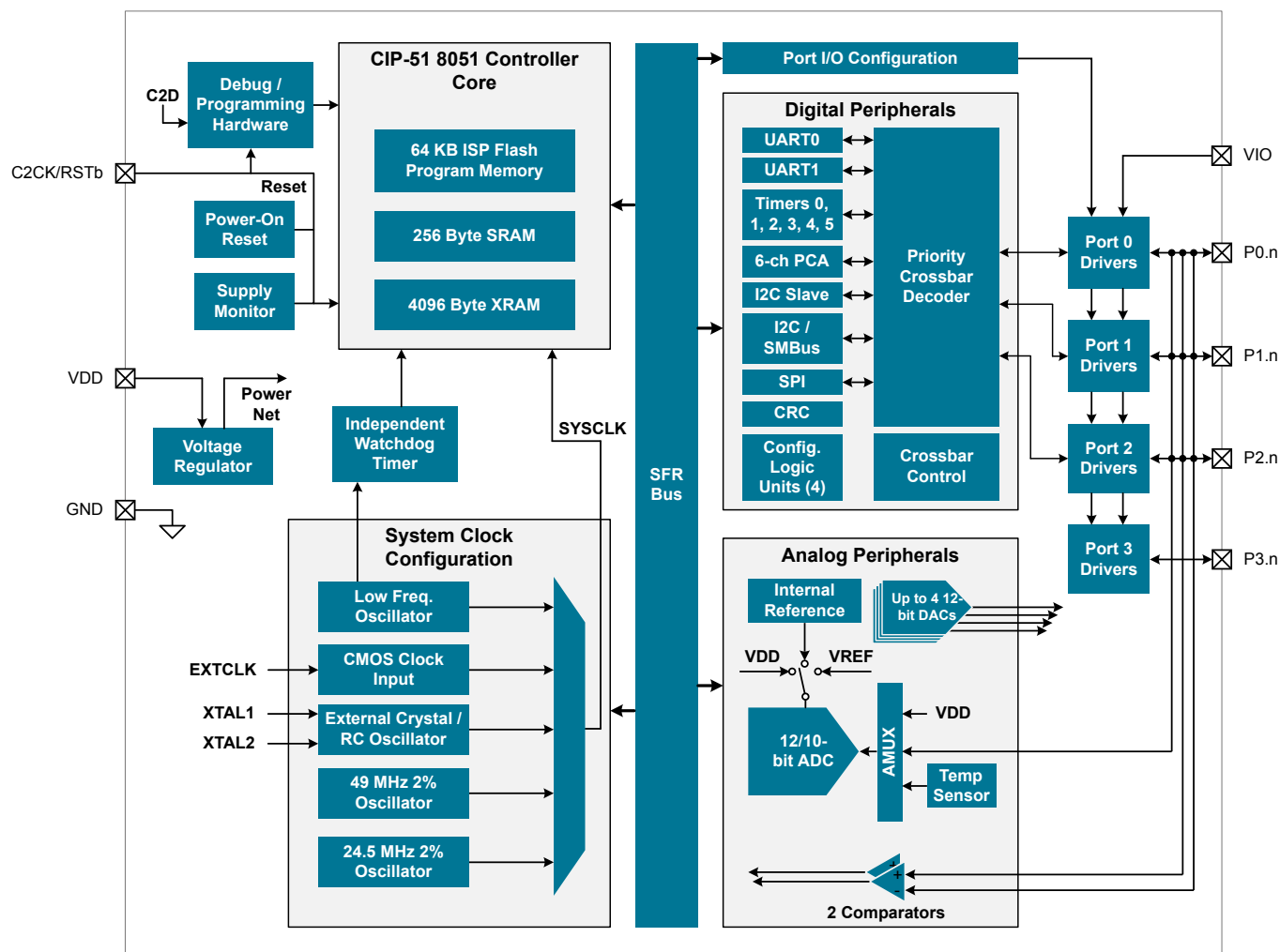


Figure 3.1. Detailed EFM8BB3 Block Diagram

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to $\text{SYSCLK}/2$ (transmit) or $\text{SYSCLK}/8$ (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- Single-byte buffer on transmit and receive
- Auto-baud detection
- LIN break and sync field detection
- CTS / RTS hardware flow control

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes
- Supports external clock frequencies up to 12 Mbps in master or slave mode
- Support for all clock phase and polarity modes
- 8-bit programmable clock rate (master)
- Programmable receive timeout (slave)
- Two byte FIFO on transmit and receive
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- Support for multiple masters on the same data lines

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive FIFOs (one byte) to help increase throughput in faster applications

Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- Additional input options:
 - Internal connection to LDO output
 - Direct connection to GND
 - Direct connection to VDD
 - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ± 20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

3.9 Debugging

The EFM8BB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [Application Notes] tile.

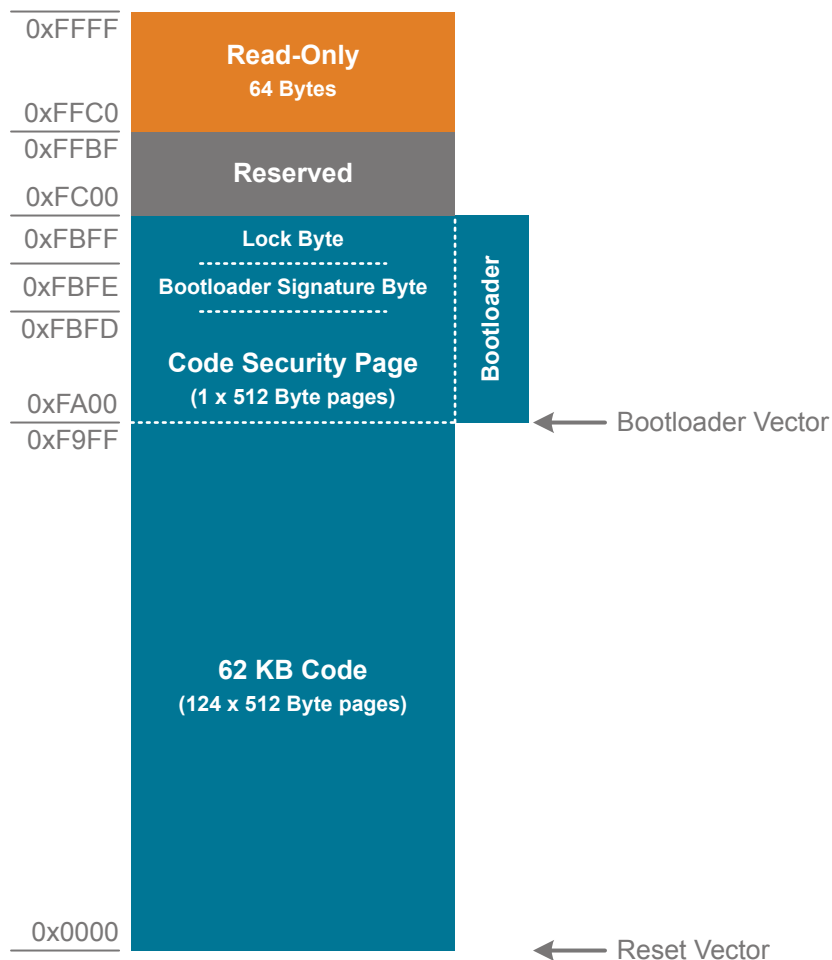


Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 14](#), unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO ^{2,3}	V _{IO}		2.2	—	V _{DD}	V
System Clock Frequency	f _{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T _A	G-grade devices	−40	—	85	°C
		I-grade devices	−40	—	125	°C

Note:

1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. GPIO levels are undefined whenever VIO is less than 1 V.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I_{DD}		—	120	740	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I_{DD}		—	0.2	4.5	μA
Analog Peripheral Supply Currents (-40 °C to +125 °C)						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 24.5 MHz, $T_A = 25\text{ °C}$	—	120	135	μA
High-Frequency Oscillator 1	I_{HFOSC1}	Operating at 49 MHz, $T_A = 25\text{ °C}$	—	770	1200	μA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, $T_A = 25\text{ °C}$	—	3.7	6	μA
ADC0 ⁴	I_{ADC}	High Speed Mode 1 Msps, 10-bit conversions Normal bias settings $V_{DD} = 3.0\text{ V}$	—	1210	1600	μA
		Low Power Mode 350 ksps, 12-bit conversions Low power bias settings $V_{DD} = 3.0\text{ V}$	—	415	560	μA
Internal ADC0 Reference ⁵	I_{VREFFS}	High Speed Mode	—	700	790	μA
		Low Power Mode	—	170	210	μA
On-chip Precision Reference	I_{VREFP}		—	75	—	μA
Temperature Sensor	I_{TSENSE}		—	68	120	μA
Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3) ⁶	I_{DAC}		—	125	—	μA
Comparators (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	—	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	25	—	μA
Comparator Reference	I_{CPREF}		—	24	—	μA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	μA

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	751	—	mV
Offset Error ¹	E_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	19	—	mV
Slope	M		—	2.82	—	mV/ $^{\circ}\text{C}$
Slope Error ¹	E_M		—	29	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity	LIN	$T = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	—	± 0.4	—	$^{\circ}\text{C}$
		$T = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ (I-grade parts only)	—	-0.6 to 1.2	—	$^{\circ}\text{C}$
Turn-on Time	t_{ON}		—	3.5	—	μs
Note: 1. Represents one standard deviation from the mean.						

4.1.13 Comparators

Table 4.13. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Low- est Power)	t_{RESP3}	+100 mV Differential	—	1.5	—	μ s
		-100 mV Differential	—	3.5	—	μ s
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

Table 4.17. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	$f_{\text{CSO}} / 3$
Bus Free Time Between STOP and START Conditions	t_{BUF}	$2 / f_{\text{CSO}}$
Hold Time After (Repeated) START Condition	$t_{\text{HD:STA}}$	$1 / f_{\text{CSO}}$
Repeated START Condition Setup Time	$t_{\text{SU:STA}}$	$2 / f_{\text{CSO}}$
STOP Condition Setup Time	$t_{\text{SU:STO}}$	$2 / f_{\text{CSO}}$
Clock Low Period	t_{LOW}	$1 / f_{\text{CSO}}$
Clock High Period	t_{HIGH}	$2 / f_{\text{CSO}}$

Note:
1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

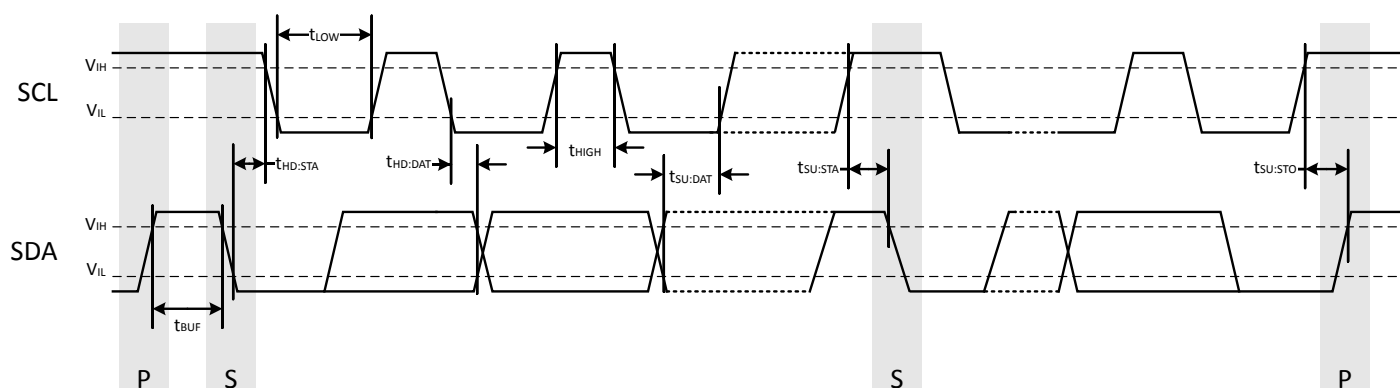


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFN24 Packages	—	30	—	°C/W
		QFN32 Packages	—	26	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QSOP24 Packages	—	65	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

6.2 EFM8BB3x-QFP32 Pin Definitions

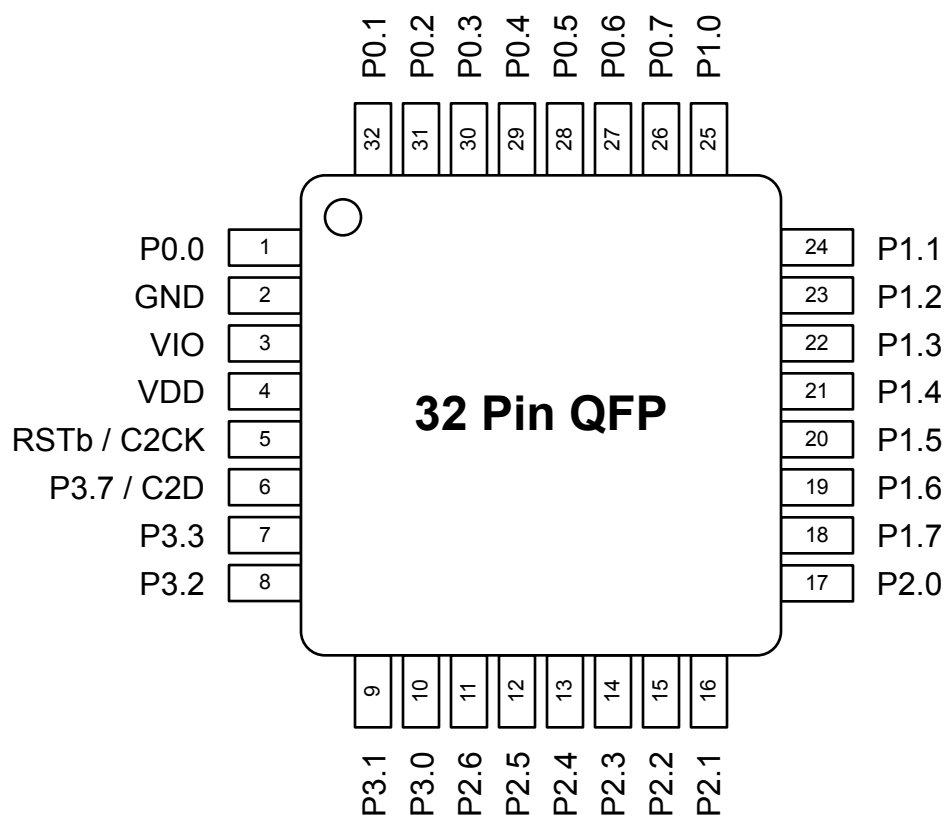


Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8BB3x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2

6.3 EFM8BB3x-QFN24 Pin Definitions

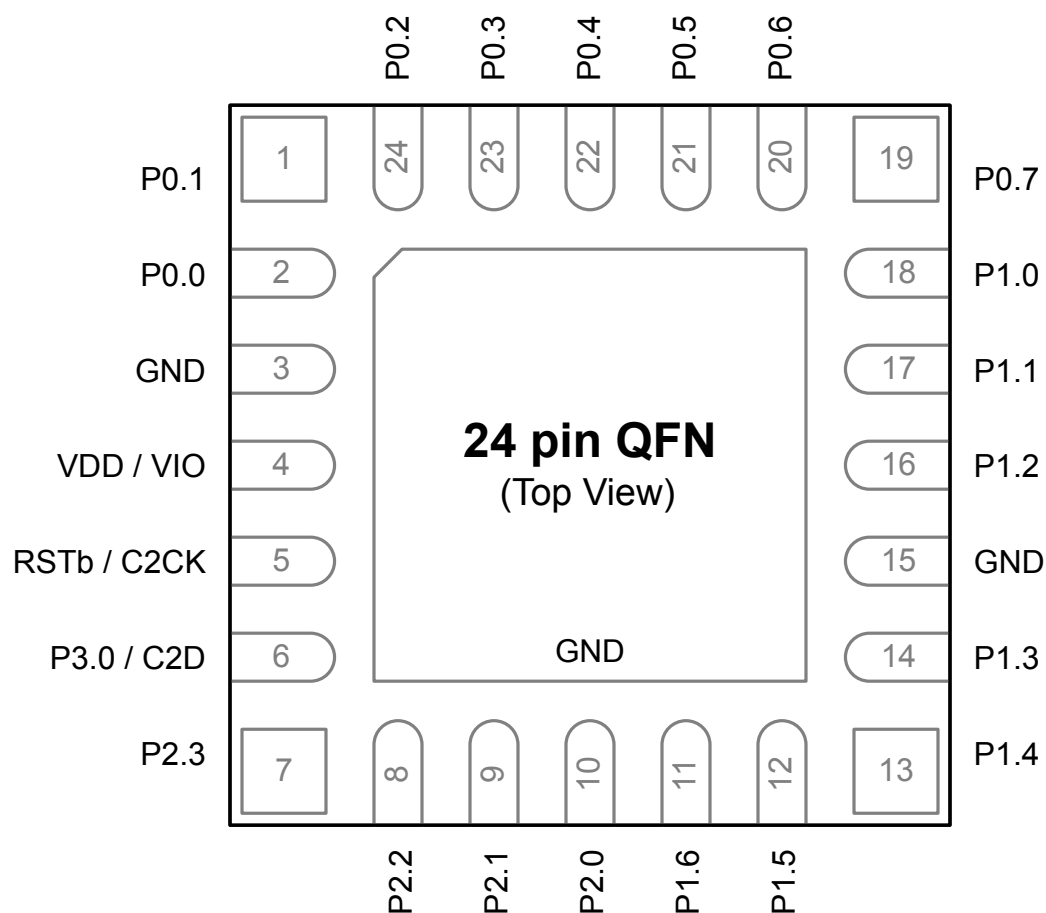


Figure 6.3. EFM8BB3x-QFN24 Pinout

Table 6.3. Pin Definitions for EFM8BB3x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13	ADC0.10 CMP1P.4 CMP1N.4
13	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12	ADC0.9 CMP1P.3 CMP1N.3
14	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2
15	GND	Ground			
16	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8
17	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7
18	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8
19	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7
20	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6
21	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1OUT CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.1 CMP1N.1
22	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4 CMP1P.0 CMP1N.0
23	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

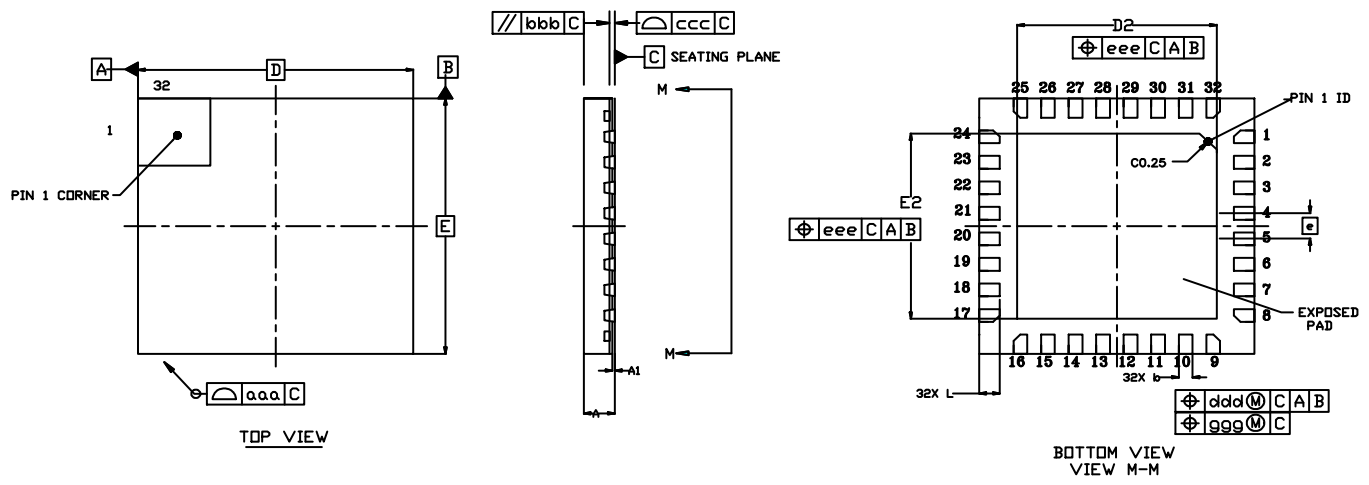


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.035	0.05
b	0.15	0.20	0.25
D	4.00 BSC.		
D2	2.80	2.90	3.00
e	0.40 BSC.		
E	4.00 BSC.		
E2	2.80	2.90	3.00
L	0.20	0.30	0.40
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10
ggg	—	—	0.05

Dimension	Min	Max
Note: <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on the IPC-SM-782 guidelines. 4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 6. The stencil thickness should be 0.125 mm (5 mils). 7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 8. A 2 x 1 array of 0.7 mm x 1.6 mm openings on a 0.9 mm pitch should be used for the center pad. 9. A No-Clean, Type-3 solder paste is recommended. 10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. 		

9.3 QFN24 Package Marking

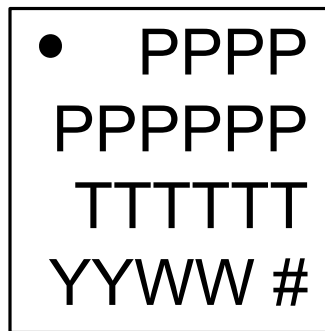


Figure 9.3. QFN24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

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