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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64i-b-qfp32">https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64i-b-qfp32</a>

## 1. Feature List

The EFM8BB3 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 50 MHz maximum operating frequency
- Memory:
  - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
  - Up to 25 pins 5 V tolerant under bias
  - Selectable state retention through reset events
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 49 MHz oscillator with accuracy of  $\pm 2\%$
  - Internal 24.5 MHz oscillator with  $\pm 2\%$  accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
  - External crystal/RC Oscillator (up to 25 MHz)
- Analog:
  - 12/10-Bit Analog-to-Digital Converter (ADC)
  - Internal temperature sensor
  - 4 x 12-Bit Digital-to-Analog Converters (DAC)
  - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
  - 2 x UART, up to 3 Mbaud
  - SPI™ Master / Slave, up to 12 Mbps
  - SMBus™/I2C™ Master / Slave, up to 400 kbps
  - I2C High-Speed Slave, up to 3.4 Mbps
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
  - 4 Configurable Logic Units
- Timers/Counters and PWM:
  - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 6 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-programmed UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Voltage DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-B-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F32G-B-QFN32	32	2304	29	2 <sup>1</sup>	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F32G-B-QFP32	32	2304	28	2 <sup>1</sup>	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F32G-B-QFN24	32	2304	20	2 <sup>1</sup>	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F32G-B-QSOP24	32	2304	21	2 <sup>1</sup>	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F16G-B-QFN32	16	2304	29	2 <sup>1</sup>	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F16G-B-QFP32	16	2304	28	2 <sup>1</sup>	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F16G-B-QFN24	16	2304	20	2 <sup>1</sup>	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F16G-B-QSOP24	16	2304	21	2 <sup>1</sup>	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F64I-B-QFN32	64	4352	29	4	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F64I-B-QFP32	64	4352	28	4	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F64I-B-QFN24	64	4352	20	4	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F64I-B-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +125 °C	QSOP24
EFM8BB31F32I-B-QFN32	32	2304	29	2 <sup>1</sup>	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F32I-B-QFP32	32	2304	28	2 <sup>1</sup>	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F32I-B-QFN24	32	2304	20	2 <sup>1</sup>	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F32I-B-QSOP24	32	2304	21	2 <sup>1</sup>	13	6	7	Yes	-40 to +125 °C	QSOP24
EFM8BB31F16I-B-QFN32	16	2304	29	2 <sup>1</sup>	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F16I-B-QFP32	16	2304	28	2 <sup>1</sup>	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F16I-B-QFN24	16	2304	20	2 <sup>1</sup>	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F16I-B-QSOP24	16	2304	21	2 <sup>1</sup>	13	6	7	Yes	-40 to +125 °C	QSOP24

**Note:**

1. DAC0 and DAC1 are enabled on devices with 2 DACs available.

## 3. System Overview

### 3.1 Introduction

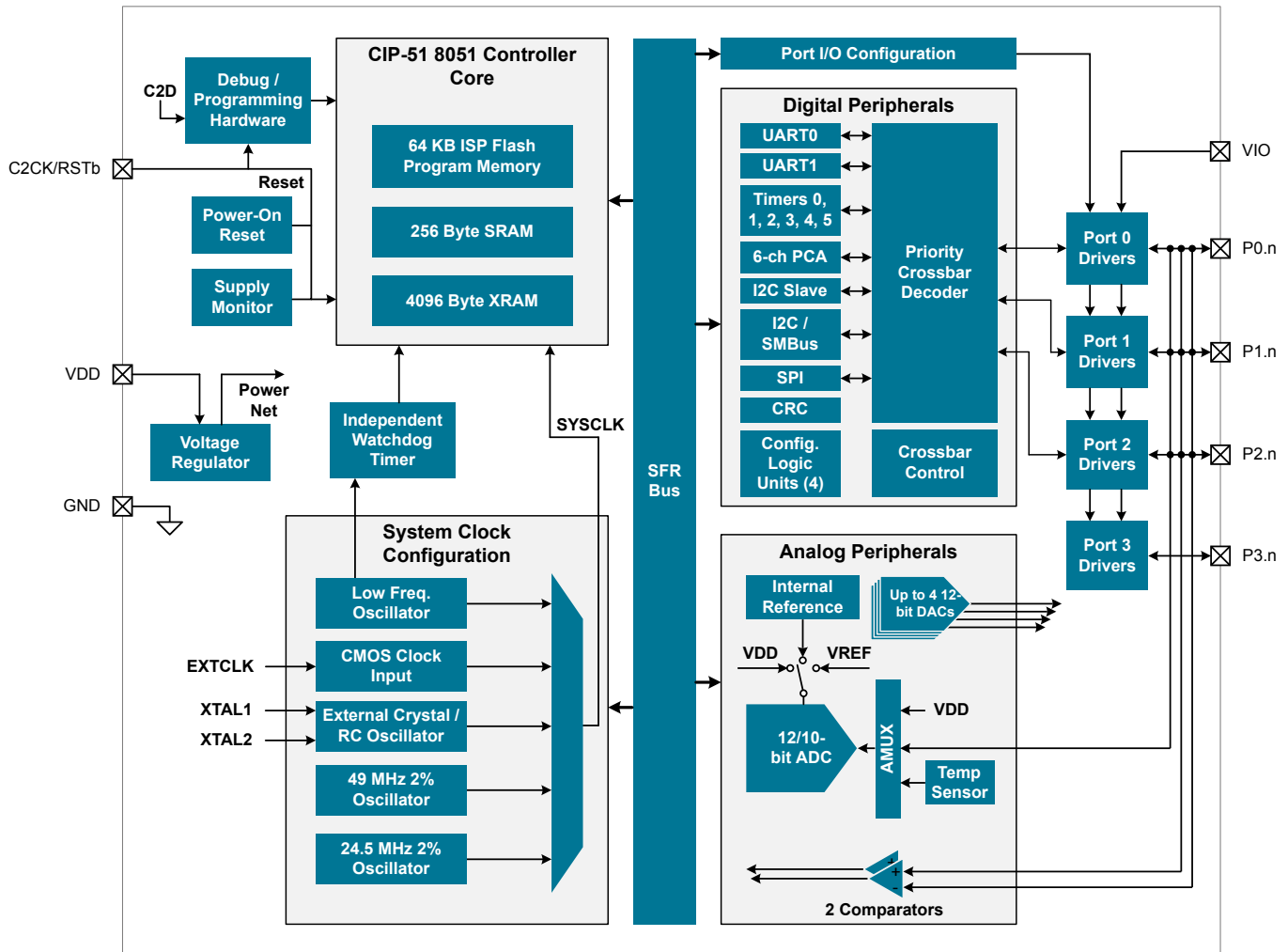


Figure 3.1. Detailed EFM8BB3 Block Diagram

### 3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

**Table 3.1. Power Modes**

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	<ul style="list-style-type: none"> <li>Core halted</li> <li>All peripherals clocked and fully operational</li> <li>Code resumes execution on wake event</li> </ul>	Set IDLE bit in PCON0	Any interrupt
Suspend	<ul style="list-style-type: none"> <li>Core and peripheral clocks halted</li> <li>HFOSC0 and HFOSC1 oscillators stopped</li> <li>Regulator in normal bias mode for fast wake</li> <li>Timer 3 and 4 may clock from LFOSC0</li> <li>Code resumes execution on wake event</li> </ul>	<ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0</li> <li>Set SUSPEND bit in PCON1</li> </ol>	<ul style="list-style-type: none"> <li>Timer 4 Event</li> <li>SPI0 Activity</li> <li>I2C0 Slave Activity</li> <li>Port Match Event</li> <li>Comparator 0 Falling Edge</li> <li>CLUn Interrupt-Enabled Event</li> </ul>
Stop	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on any reset source</li> </ul>	<ol style="list-style-type: none"> <li>Clear STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	Any reset source
Snooze	<ul style="list-style-type: none"> <li>Core and peripheral clocks halted</li> <li>HFOSC0 and HFOSC1 oscillators stopped</li> <li>Regulator in low bias current mode for energy savings</li> <li>Timer 3 and 4 may clock from LFOSC0</li> <li>Code resumes execution on wake event</li> </ul>	<ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0</li> <li>Set SNOOZE bit in PCON1</li> </ol>	<ul style="list-style-type: none"> <li>Timer 4 Event</li> <li>SPI0 Activity</li> <li>I2C0 Slave Activity</li> <li>Port Match Event</li> <li>Comparator 0 Falling Edge</li> <li>CLUn Interrupt-Enabled Event</li> </ul>
Shutdown	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on pin or power-on reset</li> </ul>	<ol style="list-style-type: none"> <li>Set STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	<ul style="list-style-type: none"> <li>RSTb pin reset</li> <li>Power-on reset</li> </ul>

### 3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

## Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

## Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

## 3.6 Communications and Other Digital Peripherals

### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

## 3.7 Analog

### 12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12- and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 12-bit and 10-bit modes
- Supports an output update rate of up to 350 ksps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated temperature sensor

### 12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Supports an update rate of 200 ksps
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

## 4.1.13 Comparators

Table 4.13. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	$t_{RESP0}$	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Low- est Power)	$t_{RESP3}$	+100 mV Differential	—	1.5	—	$\mu$ s
		-100 mV Differential	—	3.5	—	$\mu$ s
Positive Hysteresis Mode 0 (CPMD = 00)	$HYS_{CP+}$	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	$HYS_{CP-}$	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	$HYS_{CP+}$	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	$HYS_{CP-}$	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	$HYS_{CP+}$	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	$HYS_{CP-}$	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	$HYS_{CP+}$	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV



### 4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.19 Absolute Maximum Ratings on page 32](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 4.19. Absolute Maximum Ratings**

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	$T_{BIAS}$		-55	125	°C
Storage Temperature	$T_{STG}$		-65	150	°C
Voltage on VDD	$V_{DD}$		GND-0.3	4.2	V
Voltage on VIO <sup>2</sup>	$V_{IO}$		GND-0.3	$V_{DD}+0.3$	V
Voltage on I/O pins or RSTb, excluding P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	$V_{IN}$	$V_{IO} > 3.3\text{ V}$	GND-0.3	5.8	V
		$V_{IO} < 3.3\text{ V}$	GND-0.3	$V_{IO}+2.5$	V
Voltage on P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	$V_{IN}$		GND-0.3	$V_{DD}+0.3$	V
Total Current Sunk into Supply Pin	$I_{VDD}$		—	200	mA
Total Current Sourced out of Ground Pin	$I_{GND}$		200	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	$I_{IO}$		-100	100	mA
Operating Junction Temperature	$T_J$	$T_A = -40\text{ °C to }85\text{ °C}$	-40	105	°C
		$T_A = -40\text{ °C to }125\text{ °C}$ (I-grade parts only)	-40	130	°C

**Note:**

1. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.

## 6. Pin Definitions

### 6.1 EFM8BB3x-QFN32 Pin Definitions

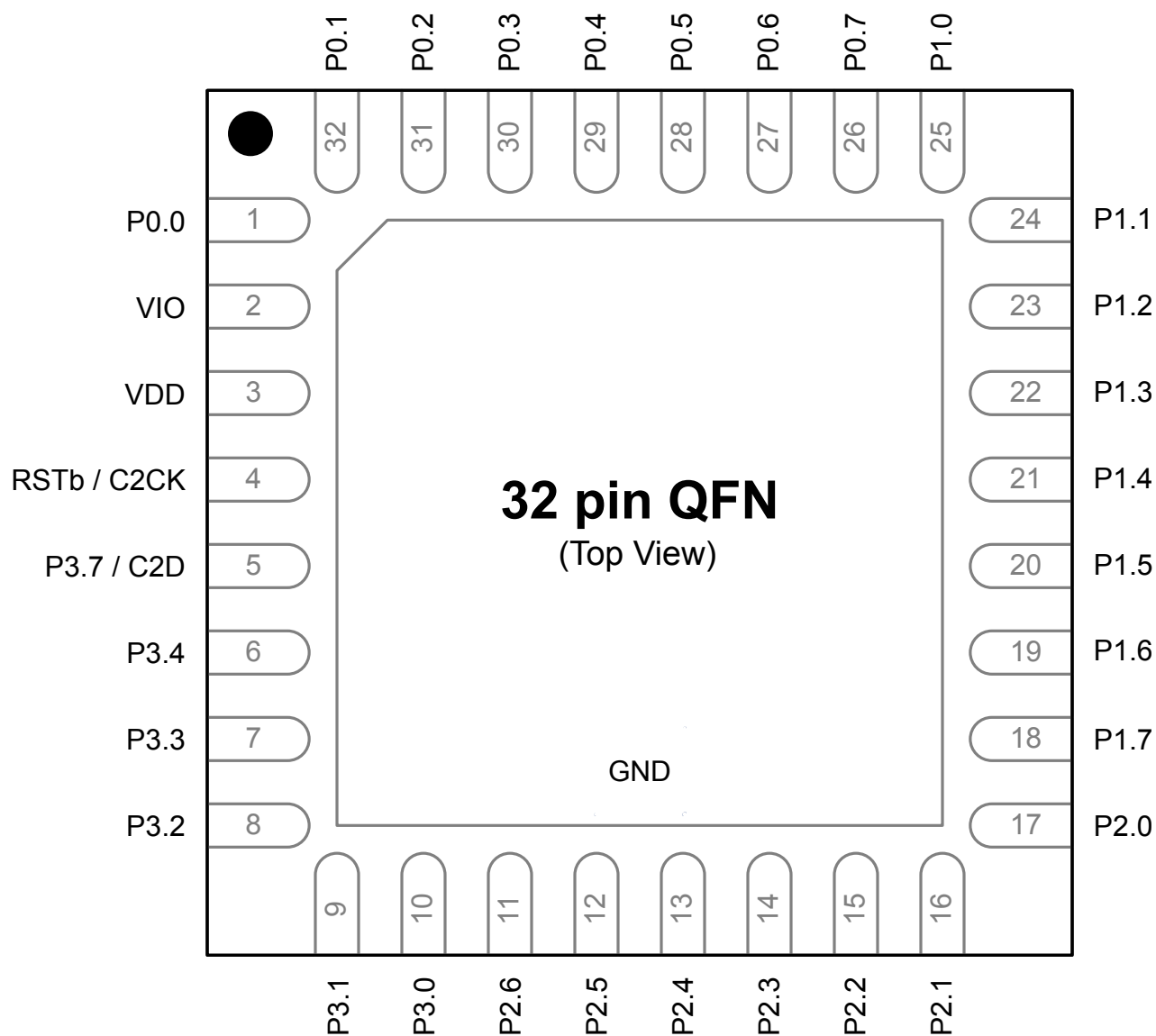


Figure 6.1. EFM8BB3x-QFN32 Pinout

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
Center	GND	Ground			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2

### 6.3 EFM8BB3x-QFN24 Pin Definitions

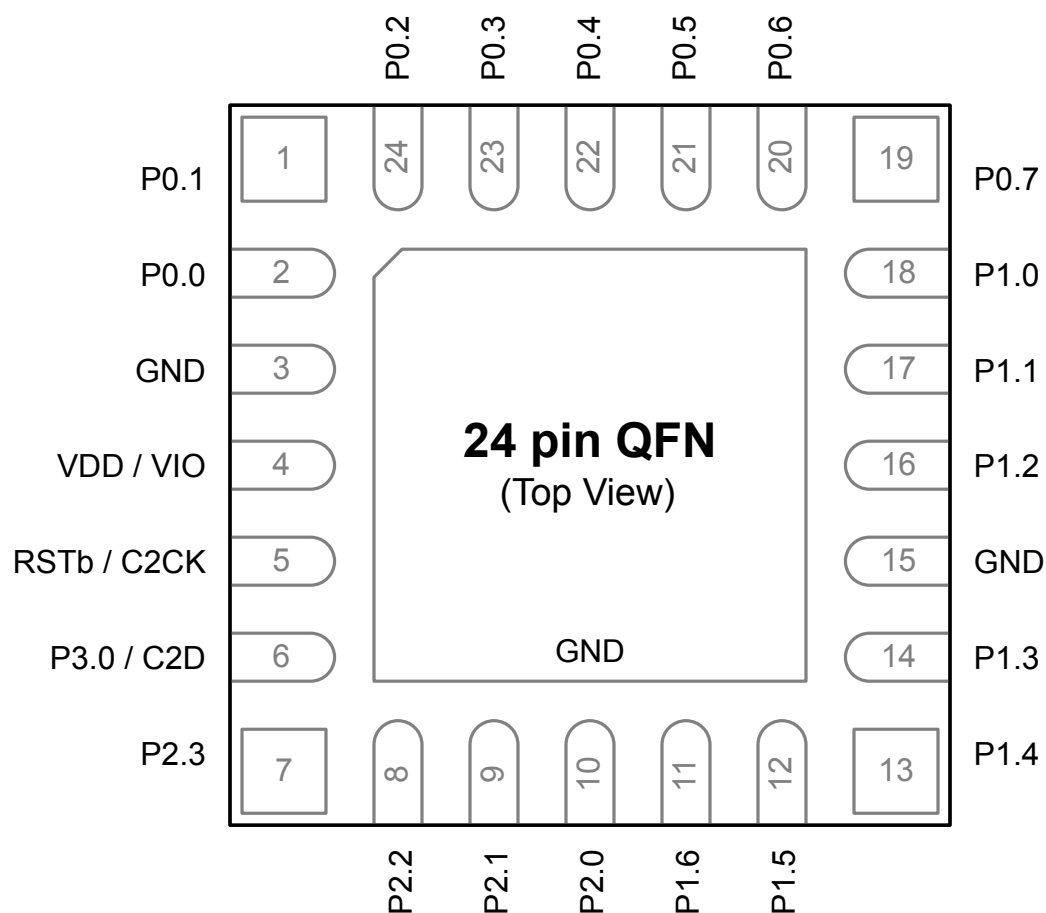


Figure 6.3. EFM8BB3x-QFN24 Pinout

Table 6.3. Pin Definitions for EFM8BB3x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

## 6.4 EFM8BB3x-QSOP24 Pin Definitions

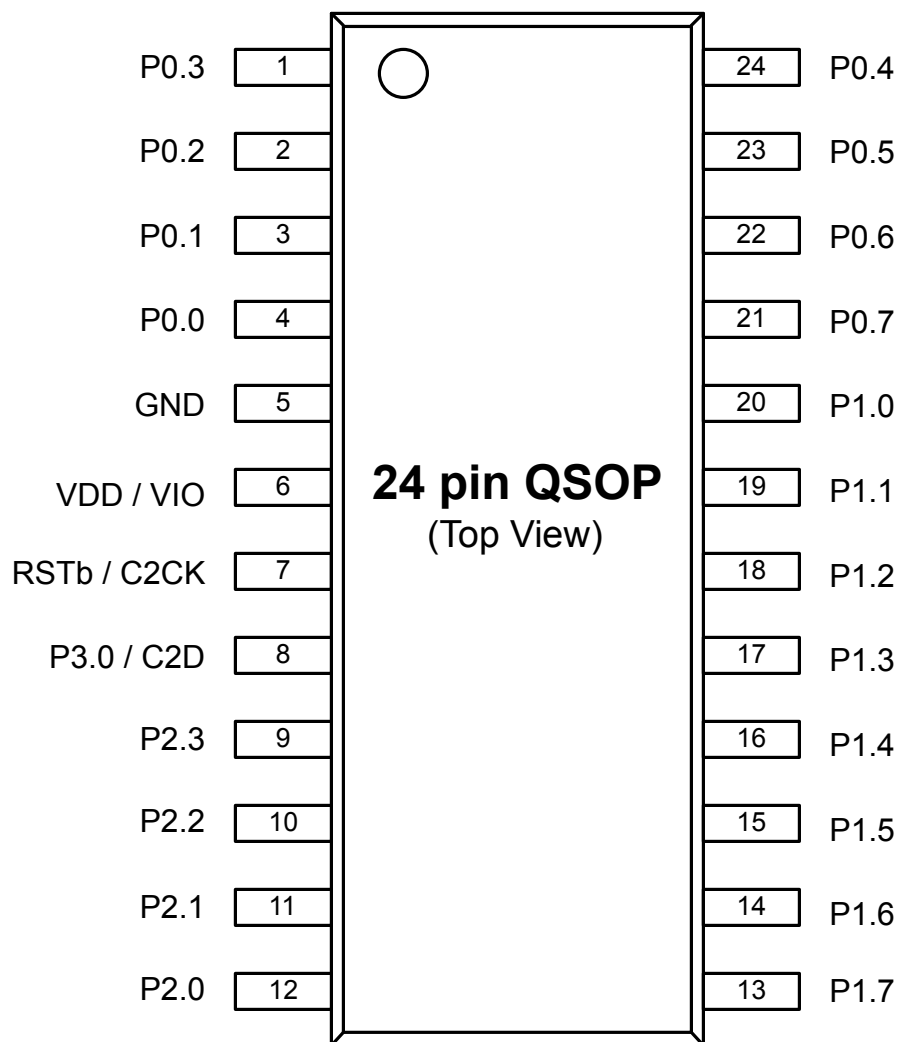


Figure 6.4. EFM8BB3x-QSOP24 Pinout

Table 6.4. Pin Definitions for EFM8BB3x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
5	GND	Ground			
6	VDD / VIO	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
10	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2

Dimension	Min	Max
<b>Note:</b> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.</li> <li>3. This Land Pattern Design is based on the IPC-7351 guidelines.</li> <li>4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.</li> <li>5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.</li> <li>6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>7. The stencil thickness should be 0.125 mm (5 mils).</li> <li>8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.</li> <li>9. A 2 x 2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center pad.</li> <li>10. A No-Clean, Type-3 solder paste is recommended.</li> <li>11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol>		

### 7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).



Dimension	Min	Typ	Max
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
theta	0°	3.5°	7°

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Dimension	Min	Typ	Max
e	0.40 BSC		
e1	0.45 BSC		
J	1.60	1.70	1.80
K	1.60	1.70	1.80
L	0.35	0.40	0.45
L1	0.25	0.30	0.35
aaa	—	0.10	—
bbb	—	0.10	—
ccc	—	0.08	—
ddd	—	0.1	—
eee	—	0.1	—

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-248 but includes custom features which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 9.2 QFN24 PCB Land Pattern

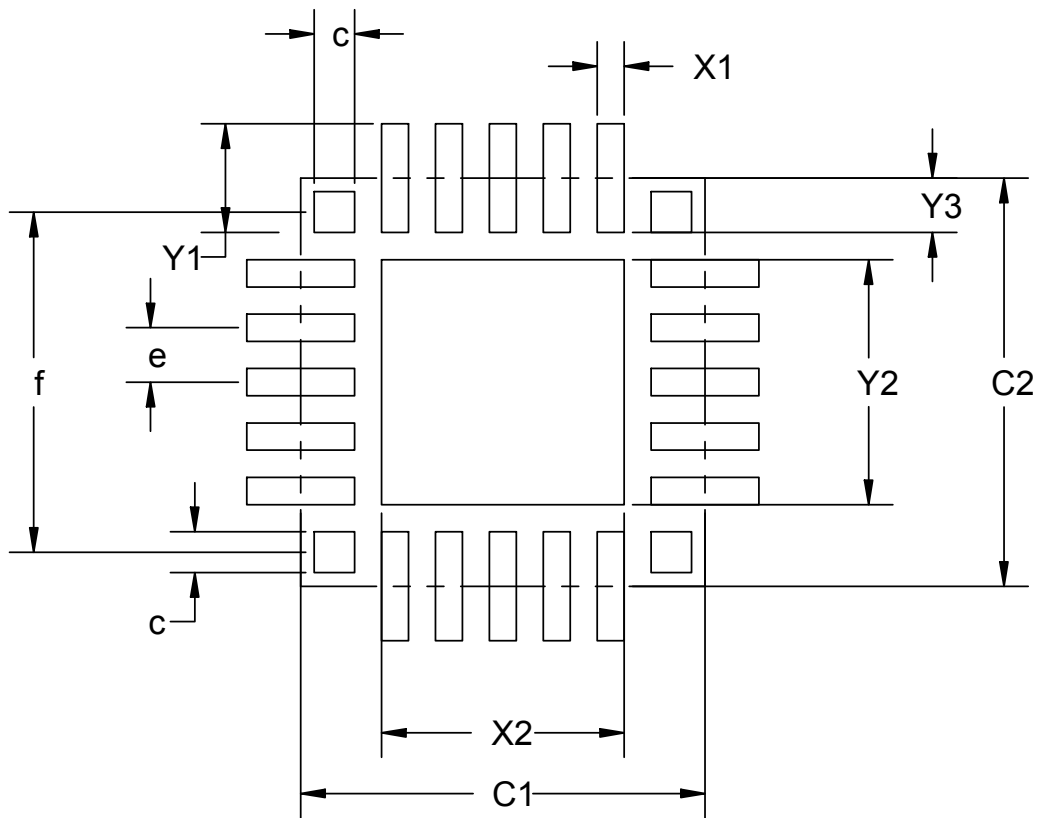


Figure 9.2. QFN24 PCB Land Pattern Drawing

Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Max
C1		3.00
C2		3.00
e		0.4 REF
X1		0.20
X2		1.80
Y1		0.80
Y2		1.80
Y3		0.4
f		2.50 REF
c	0.25	0.35

### 10.3 QSOP24 Package Marking



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

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