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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	104
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	98K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2388fbd144-551

- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as the system clock. When used as the CPU clock, does not allow CAN and USB to run.
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Boundary scan for simplified board testing.
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.

3. Applications

- Industrial control
- Medical systems
- Protocol converter
- Communications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2388FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					External bus	Ethernet	USB device host OTG+ 4 kB FIFO	CAN channels	SD/MMC	GP DMA	ADC channels	DAC channels	Temp range
		Local bus	Ethernet buffer	GP/USB	RTC	Total									
LPC2388FBD144	512	64	16	16	2	98	MiniBus: 8 data, 16 address, and 2 chip select lines	RMII	yes	2	yes	yes	8	1	−40 °C to +85 °C

5. Block diagram

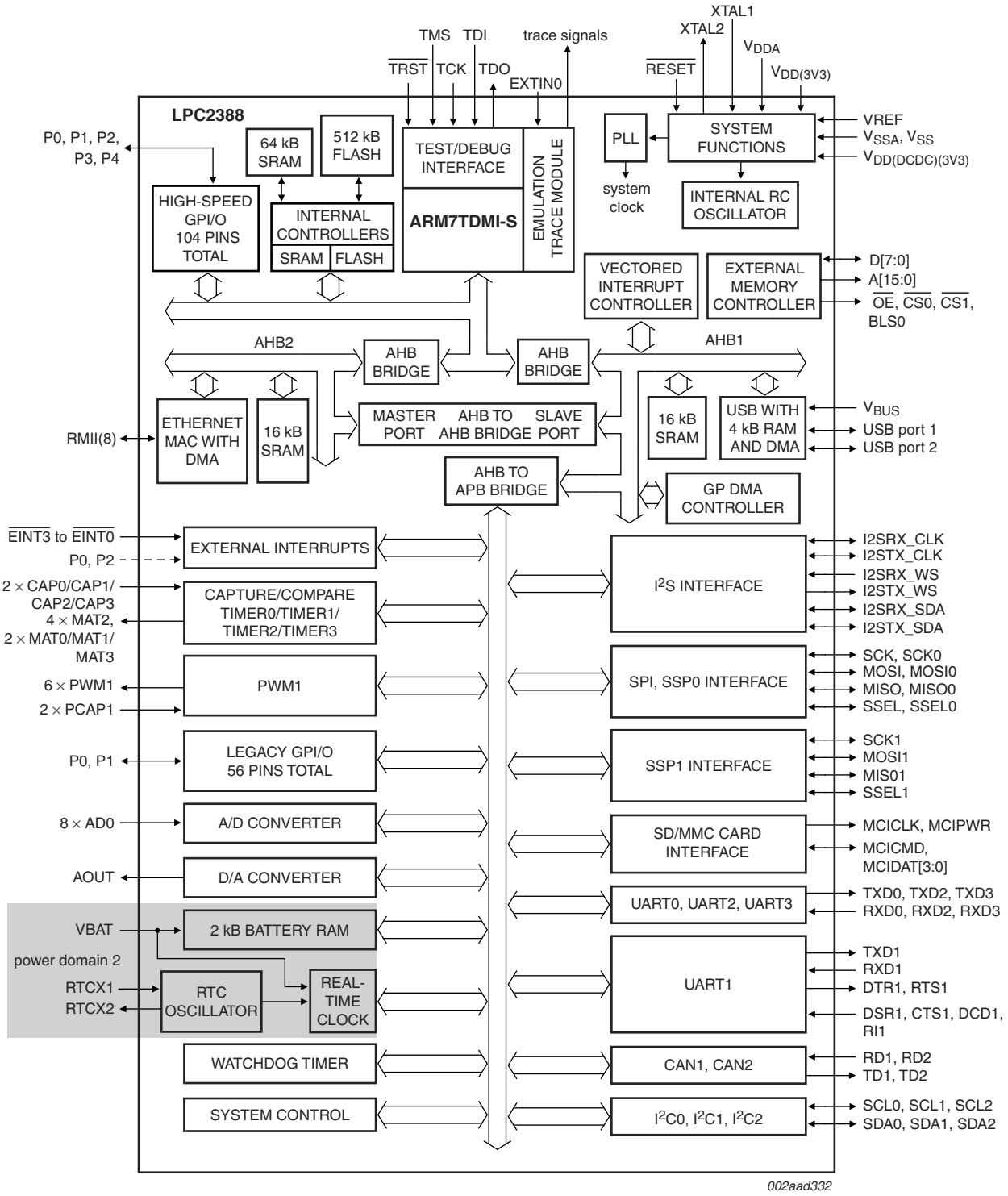


Fig 1. LPC2388 block diagram

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0[14]/ USB_HSTEN2/ USB_CONNECT2/ SSEL1	48[1]	I/O	**P0[14] —** General purpose digital input/output pin.
		O	**USB_HSTEN2 —** Host Enabled status for USB port 2.
		O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
		I/O	**SSEL1 —** Slave Select for SSP1.
P0[15]/TXD1/ SCK0/SCK	89[1]	I/O	**P0[15] —** General purpose digital input/output pin.
		O	**TXD1 —** Transmitter output for UART1.
		I/O	**SCK0 —** Serial clock for SSP0.
		I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	90[1]	I/O	**P0 [16] —** General purpose digital input/output pin.
		I	**RXD1 —** Receiver input for UART1.
		I/O	**SSEL0 —** Slave Select for SSP0.
		I/O	**SSEL —** Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	87[1]	I/O	**P0[17] —** General purpose digital input/output pin.
		I	**CTS1 —** Clear to Send input for UART1.
		I/O	**MISO0 —** Master In Slave Out for SSP0.
		I/O	**MISO —** Master In Slave Out for SPI.
P0[18]/DCD1/ MOSI0/MOSI	86[1]	I/O	**P0[18] —** General purpose digital input/output pin.
		I	**DCD1 —** Data Carrier Detect input for UART1.
		I/O	**MOSI0 —** Master Out Slave In for SSP0.
		I/O	**MOSI —** Master Out Slave In for SPI.
P0[19]/DSR1/ MCICLK/SDA1	85[1]	I/O	**P0[19] —** General purpose digital input/output pin.
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**MCICLK —** Clock output line for SD/MMC interface.
		I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[20]/DTR1/ MCICMD/SCL1	83[1]	I/O	**P0[20] —** General purpose digital input/output pin.
		O	**DTR1 —** Data Terminal Ready output for UART1.
		I	**MCICMD —** Command line for SD/MMC interface.
		I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[21]/RI1/ MCIPWR/RD1	82[1]	I/O	**P0[21] —** General purpose digital input/output pin.
		I	**RI1 —** Ring Indicator input for UART1.
		O	**MCIPWR —** Power Supply Enable for external SD/MMC power supply.
		I	**RD1 —** CAN1 receiver input.
P0[22]/RTS1/ MCIDAT0/TD1	80[1]	I/O	**P0[22] —** General purpose digital input/output pin.
		O	**RTS1 —** Request to Send output for UART1.
		O	**MCIDAT0 —** Data line for SD/MMC interface.
		O	**TD1 —** CAN1 transmitter output.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P2[2]/PWM1[3]/ CTS1/ PIPESTAT1	105[1]	I/O	**P2[2] —** General purpose digital input/output pin.
		O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
		I	**CTS1 —** Clear to Send input for UART1.
		O	**PIPESTAT1 —** Pipeline Status, bit 1.
P2[3]/PWM1[4]/ DCD1/ PIPESTAT2	100[1]	I/O	**P2[3] —** General purpose digital input/output pin.
		O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
		I	**DCD1 —** Data Carrier Detect input for UART1.
		O	**PIPESTAT2 —** Pipeline Status, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACESYNC	99[1]	I/O	**P2[4] —** General purpose digital input/output pin.
		O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**TRACESYNC —** Trace Synchronization.
P2[5]/PWM1[6]/ DTR1/ TRACEPKT0	97[1]	I/O	**P2[5] —** General purpose digital input/output pin.
		O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
		O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**TRACEPKT0 —** Trace Packet, bit 0.
P2[6]/PCAP1[0]/ RI1/ TRACEPKT1	96[1]	I/O	**P2[6] —** General purpose digital input/output pin.
		I	**PCAP1[0] —** Capture input for PWM1, channel 0.
		I	**RI1 —** Ring Indicator input for UART1.
		O	**TRACEPKT1 —** Trace Packet, bit 1.
P2[7]/RD2/ RTS1/ TRACEPKT2	95[1]	I/O	**P2[7] —** General purpose digital input/output pin.
		I	**RD2 —** CAN2 receiver input.
		O	**RTS1 —** Request to Send output for UART1.
		O	**TRACEPKT2 —** Trace Packet, bit 2.
P2[8]/TD2/ TXD2/ TRACEPKT3	93[1]	I/O	**P2[8] —** General purpose digital input/output pin.
		O	**TD2 —** CAN2 transmitter output.
		O	**TXD2 —** Transmitter output for UART2.
		O	**TRACEPKT3 —** Trace Packet, bit 3.
P2[9]/ USB_CONNECT1/ RXD2/ EXTIN0	92[1]	I/O	**P2[9] —** General purpose digital input/output pin.
		O	**USB_CONNECT1 —** USB port 1 Soft Connect control. Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the SoftConnect USB feature.
		I	**RXD2 —** Receiver input for UART2.
		I	**EXTIN0 —** External Trigger Input.
P2[10]/$\overline{\text{EINT0}}$	76[6]	I/O	**P2[10] —** General purpose digital input/output pin. **Note:** LOW on this pin while RESET is LOW forces on-chip boot-loader to take over control of the part after a reset.
		I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P2[11]/$\overline{\text{EINT1}}$/ MCIDAT1/ I2STX_CLK	75[6]	I/O	**P2[11] —** General purpose digital input/output pin.
		I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
		O	**MCIDAT1 —** Data line for SD/MMC interface.
		I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
P2[12]/$\overline{\text{EINT2}}$/ MCIDAT2/ I2STX_WS	73[6]	I/O	**P2[12] —** General purpose digital input/output pin.
		I	**$\overline{\text{EINT2}}$ —** External interrupt 2 input.
		O	**MCIDAT2 —** Data line for SD/MMC interface.
		I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
P2[13]/$\overline{\text{EINT3}}$/ MCIDAT3/ I2STX_SDA	71[6]	I/O	**P2[13] —** General purpose digital input/output pin.
		I	**$\overline{\text{EINT3}}$ —** External interrupt 3 input.
		O	**MCIDAT3 —** Data line for SD/MMC interface.
		I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
P3[0] to P3[31]		I/O	**Port 3:** Port 3 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect block. Pins 8 through 22, and 27 through 31 of this port are not available.
P3[0]/D0	137[1]	I/O	**P3[0] —** General purpose digital input/output pin.
		I/O	**D0 —** External memory data line 0.
P3[1]/D1	140[1]	I/O	**P3[1] —** General purpose digital input/output pin.
		I/O	**D1 —** External memory data line 1.
P3[2]/D2	144[1]	I/O	**P3[2] —** General purpose digital input/output pin.
		I/O	**D2 —** External memory data line 2.
P3[3]/D3	2[1]	I/O	**P3[3] —** General purpose digital input/output pin.
		I/O	**D3 —** External memory data line 3.
P3[4]/D4	9[1]	I/O	**P3[4] —** General purpose digital input/output pin.
		I/O	**D4 —** External memory data line 4.
P3[5]/D5	12[1]	I/O	**P3[5] —** General purpose digital input/output pin.
		I/O	**D5 —** External memory data line 5.
P3[6]/D6	16[1]	I/O	**P3[6] —** General purpose digital input/output pin.
		I/O	**D6 —** External memory data line 6.
P3[7]/D7	19[1]	I/O	**P3[7] —** General purpose digital input/output pin.
		I/O	**D7 —** External memory data line 7.
P3[23]/CAP0[0]/ PCAP1[0]	45[1]	I/O	**P3[23] —** General purpose digital input/output pin.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
		I	**PCAP1[0] —** Capture input for PWM1, channel 0.
P3[24]/CAP0[1]/ PWM1[1]	40[1]	I/O	**P3[24] —** General purpose digital input/output pin.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
		O	**PWM1[1] —** Pulse Width Modulator 1, output 1.

via the EMC, as well as the SRAM located on another AHB, if it is not being used by the USB block. However, using memory other than the Ethernet SRAM, especially off-chip memory, will slow Ethernet access to memory and increase the loading of its AHB.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.10.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.
  - Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.
- Physical interface:
  - Attachment of external PHY chip through standard RMII interface.
  - PHY register access is available via the MIIM interface.

7.11.3 USB OTG Controller

USB OTG (On-The-Go) is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG Controller integrates the Host Controller, device controller, and a master-only I^2C interface to implement OTG dual-role device functionality. The dedicated I^2C interface controls an external OTG transceiver.

7.11.3.1 Features

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

7.12 CAN controller and acceptance filters

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.12.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- Full CAN messages can generate interrupts.

- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz ((16, 22.05, 32, 44.1, 48) kHz).
- Configurable word select period in master mode (separately for I^2S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I^2S input and I^2S output.

7.21 General purpose 32-bit timers/external event counters

The LPC2388 includes four 32-bit Timer/Counters. The Timer/Counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The Timer/Counter also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.21.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit prescaler.
- Counter or Timer operation.
- Up to four 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.22 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2388. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

7.22.1 Features

- LPC2388 has one PWM block with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

7.23 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

7.23.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the RTC clock, the Internal RC oscillator (IRC), or the APB peripheral clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring, for increased reliability.

7.24 RTC and battery RAM

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power in Power-down mode. On the LPC2388, the RTC can be clocked by a separate 32.768 kHz oscillator or by a programmable prescale divider based on the APB clock. Also, the RTC is powered by its own power supply pin, VBAT, which can be connected to a battery or to the same 3.3 V supply used by the rest of the device.

The VBAT pin supplies power only to the RTC and the Battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that can be used by external hardware to restore chip power and resume operation.

7.24.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.

- An alarm output pin is included to assist in waking up from Power-down mode, or when the chip has had power removed to all functions except the RTC and Battery RAM.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values.
- 2 kB data SRAM powered by VBAT.
- RTC and Battery RAM power supply is isolated from the rest of the chip.

7.25 Clocking and power control

7.25.1 Crystal oscillators

The LPC2388 includes three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2388 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

7.25.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy.

Upon power-up or any chip reset, the LPC2388 uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.25.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator operates at frequencies of 1 MHz to 24 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 7.25.2 for additional information.

7.25.1.3 RTC oscillator

The RTC oscillator can be used as the clock source for the RTC and/or the WDT. Also, the RTC oscillator can be used to drive the PLL and the CPU.

7.25.2 PLL

The PLL accepts an input clock frequency in the range of 32 kHz to 50 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and the USB block.

The PLL input, in the range of 32 kHz to 50 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	core and external rail		3.0	3.6	V
$V_{DD(DCDC)(3V3)}$	DC-to-DC converter supply voltage (3.3 V)			3.0	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			−0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		−0.5	+4.6	V
$V_{i(VREF)}$	input voltage on pin VREF			−0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		−0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(3V3)}$ supply voltage is present	[2]	−0.5	+6.0	V
		other I/O pins	[2][3]	−0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current	per supply pin	[4]	-	100	mA
I_{SS}	ground current	per ground pin	[4]	-	100	mA
T_{stg}	storage temperature		[5]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[6]	−2000	+2000	V

[1] The following applies to the Limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

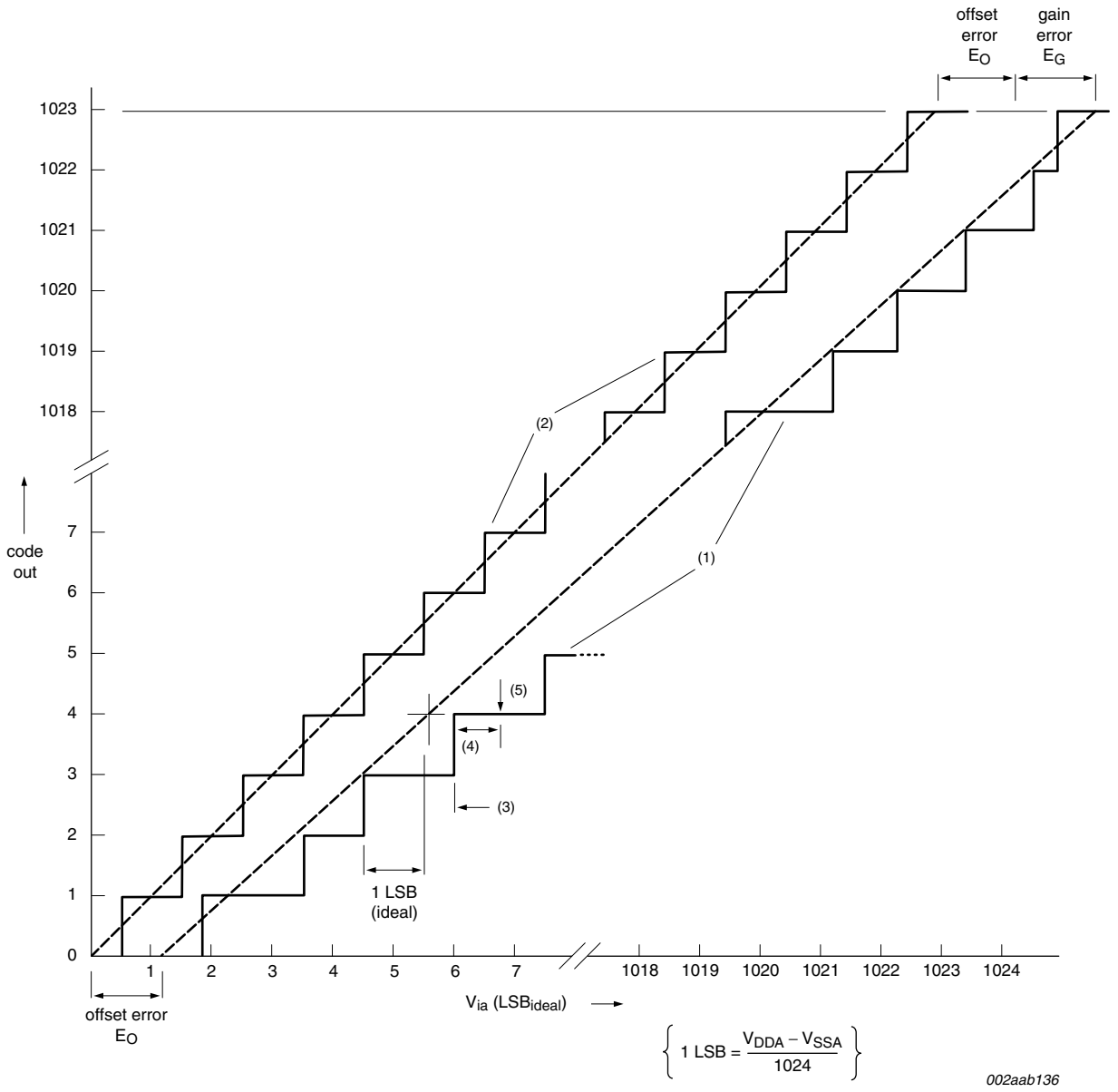
[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The peak current is limited to 25 times the corresponding maximum current.

[5] Dependent on package type.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 4. ADC characteristics

11. Application information

11.1 Suggested USB interface solutions

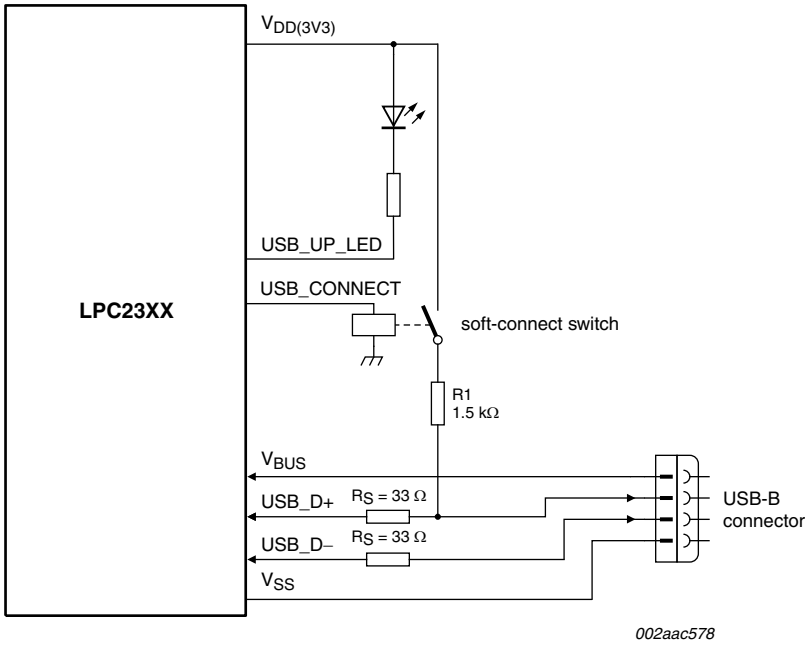


Fig 9. LPC2388 USB interface on a self-powered device

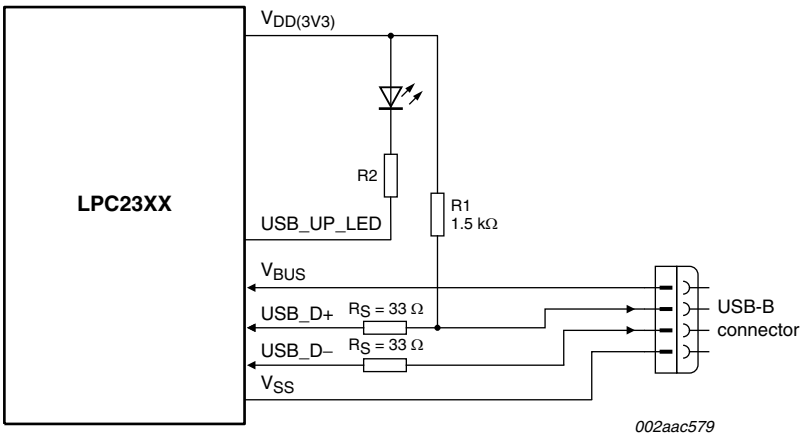


Fig 10. LPC2388 USB interface on a bus-powered device

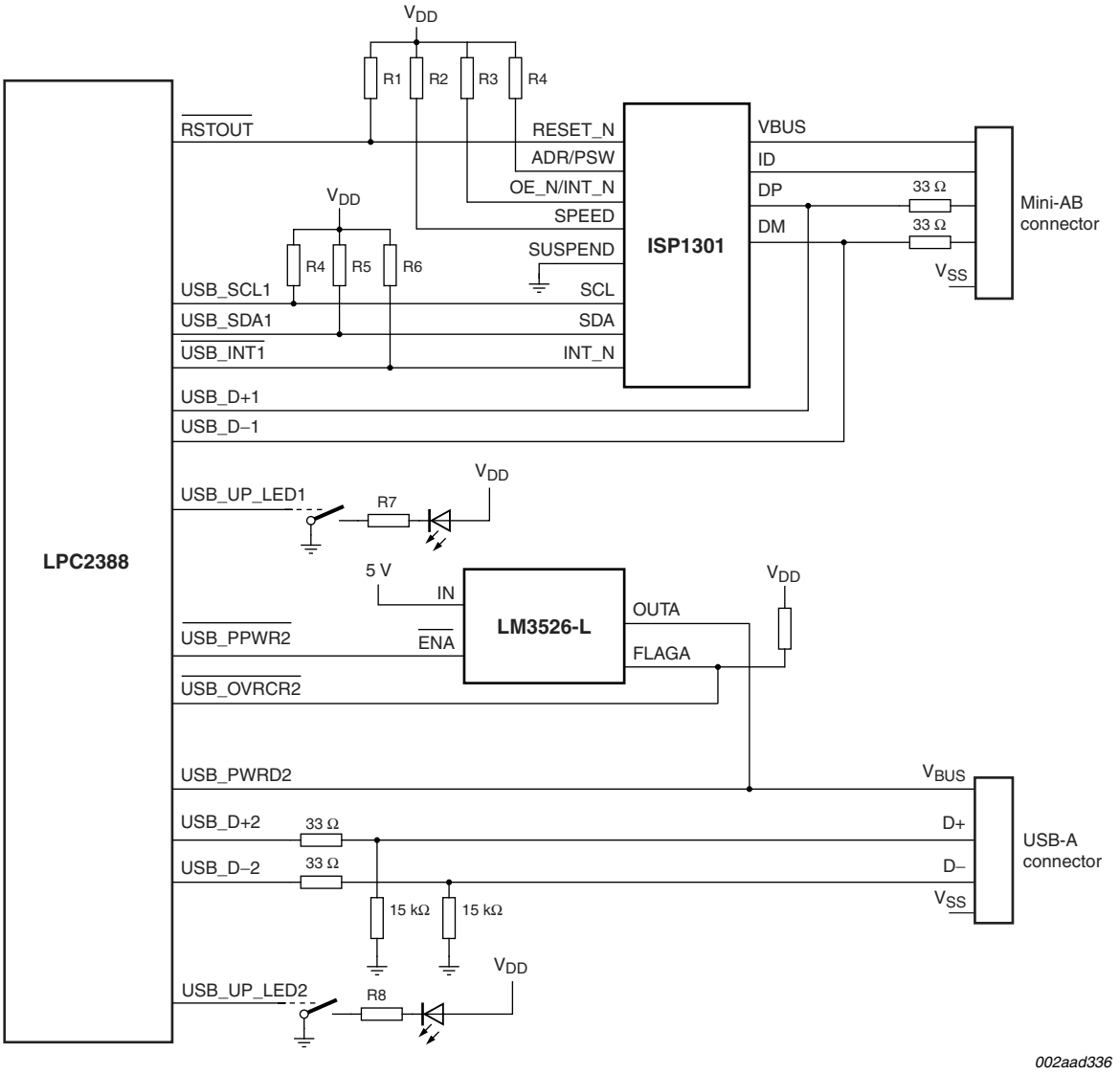


Fig 11. LPC2388 USB OTG port configuration: USB port 1 OTG dual-role device, USB port 2 host

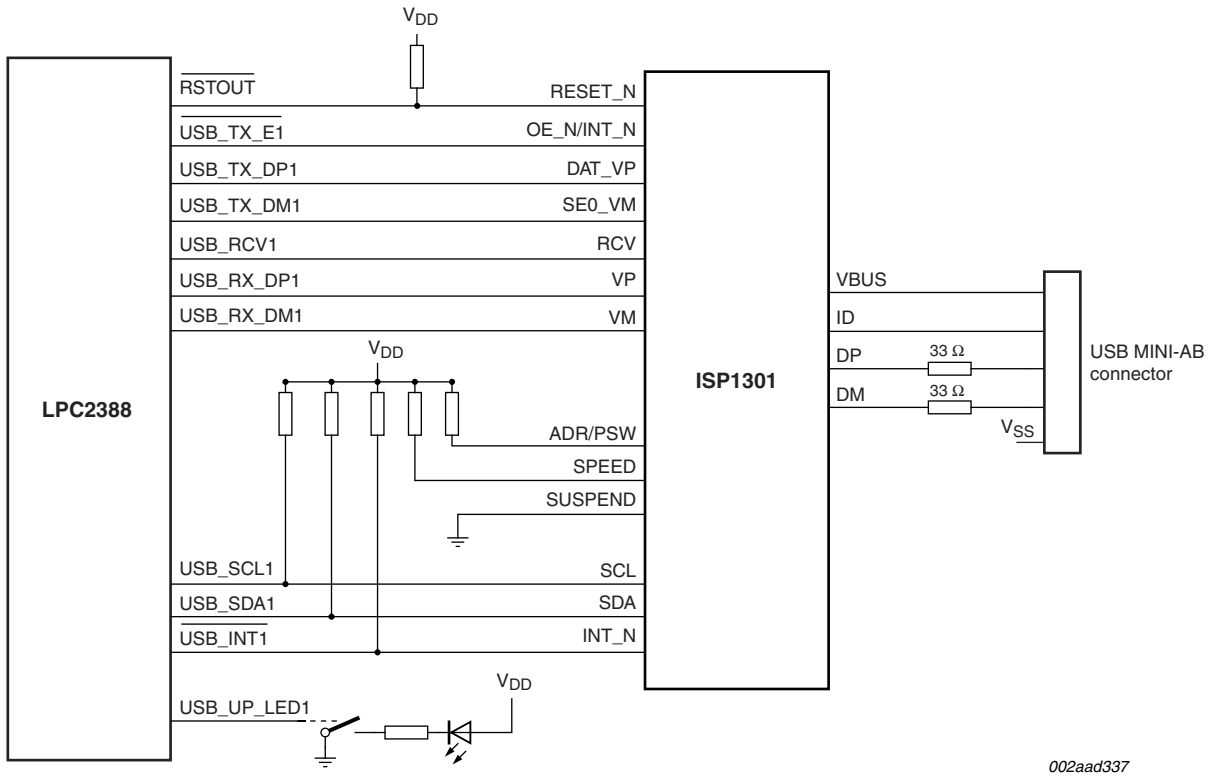


Fig 12. LPC2388 USB OTG port configuration: VP_VM mode

13. Abbreviations

Table 9. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BLS	Byte Lane Select
BOD	BrownOut Detection
CAN	Controller Area Network
CTS	Clear To Send
DAC	Digital-to-Analog Converter
DCC	Debug Communication Channel
DMA	Direct Memory Access
DSP	Digital Signal Processing
EOP	End Of Packet
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MII	Media Independent Interface
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
RTS	Request To Send
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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