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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 35x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mk20dx64vmc7

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$	-5	—	mA	1
I_{ICAIO}	Analog ² , EXTAL, and XTAL pin DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection) $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection)	-5	—	mA	3
		—	+5		
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins - Negative current injection - Positive current injection	-25	—	mA	
		—	+25		
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{DIO_MIN} ($=V_{SS}-0.3\text{V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO_MIN}-V_{IN})/|I_{IC}|$.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
3. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} ($=V_{SS}-0.3\text{V}$) and V_{IN} is less than V_{AIO_MAX} ($=V_{DD}+0.3\text{V}$) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{IC}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{IC}|$. Select the larger of these two calculated resistances.

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -9\text{mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{mA}$	$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2\text{mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{mA}$	$V_{DD} - 0.5$	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 9\text{mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{mA}$	—	0.5	V	
	Output low voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{mA}$	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	1
I_{IN}	Input leakage current (per pin) at 25°C	—	0.025	μA	1
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R_{PU}	Internal pullup resistors	20	50	k Ω	2
R_{PD}	Internal pulldown resistors	20	50	k Ω	3

1. Measured at $V_{DD}=3.6\text{V}$

2. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$

3. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{DD}$

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $V_{LLSx} \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- FlexBus clock = 36 MHz
- Flash clock = 24 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	1
	• VLLS1 → RUN	—	112	μs	
	• VLLS2 → RUN	—	74	μs	
	• VLLS3 → RUN	—	73	μs	
	• LLS → RUN	—	5.9	μs	
	• VLPS → RUN	—	5.8	μs	
	• STOP → RUN	—	4.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash	—	21.5	25	mA	2
		—	21.5	30	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash	—	31	34	mA	3, 4
		—	31	34	mA	
		—	32	39	mA	
		—	32	39	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	12.5	—	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	7.2	—	mA	5
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.996	—	mA	6
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.46	—	mA	7

Table continues on the next page...

5.4.2 Thermal attributes

Board type	Symbol	Description	121 MAPBGA	100 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	74	52	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	42	40	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	62	42	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	38	34	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	23	25	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	19	12	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	4	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal. For the LQFP, the board meets the JESD51-7 specification.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.

6.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	—	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	± 0.3	$\%f_{\text{dco}}$	1
$f_{\text{intf_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$f_{\text{intf_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$f_{\text{loc_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints_t}}$	—	—	kHz	
$f_{\text{loc_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints_t}}$	—	—	kHz	
FLL						
$f_{\text{fll_ref}}$	FLL reference frequency range		31.25	—	39.0625	kHz
f_{dco}	DCO output frequency range	Low range (DRS=00) $640 \times f_{\text{fll_ref}}$	20	20.97	25	MHz
		Mid range (DRS=01) $1280 \times f_{\text{fll_ref}}$	40	41.94	50	MHz
		Mid-high range (DRS=10) $1920 \times f_{\text{fll_ref}}$	60	62.91	75	MHz
		High range (DRS=11) $2560 \times f_{\text{fll_ref}}$	80	83.89	100	MHz
$f_{\text{dco_t_DMX32}}$	DCO output frequency	Low range (DRS=00) $732 \times f_{\text{fll_ref}}$	—	23.99	—	MHz
		Mid range (DRS=01) $1464 \times f_{\text{fll_ref}}$	—	47.97	—	MHz
		Mid-high range (DRS=10) $2197 \times f_{\text{fll_ref}}$	—	71.99	—	MHz
		High range (DRS=11) $2929 \times f_{\text{fll_ref}}$	—	95.98	—	MHz

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_fll}	FLL period jitter $f_{VCO} = 48 \text{ MHz}$ $f_{VCO} = 98 \text{ MHz}$	—	180	—	ps	
$t_{fll_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
PLL						
f_{vco}	VCO operating frequency	48.0	—	100	MHz	
I_{pll}	PLL operating current PLL @ 96 MHz ($f_{osc_hi_1} = 8 \text{ MHz}$, $f_{pll_ref} = 2 \text{ MHz}$, VDIV multiplier = 48)	—	1060	—	μA	7
I_{pll}	PLL operating current PLL @ 48 MHz ($f_{osc_hi_1} = 8 \text{ MHz}$, $f_{pll_ref} = 2 \text{ MHz}$, VDIV multiplier = 24)	—	600	—	μA	7
f_{pll_ref}	PLL reference frequency range	2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) $f_{vco} = 48 \text{ MHz}$ $f_{vco} = 100 \text{ MHz}$	—	120	—	ps	8
J_{acc_pll}	PLL accumulated jitter over 1 μs (RMS) $f_{vco} = 48 \text{ MHz}$ $f_{vco} = 100 \text{ MHz}$	—	1350	—	ps	8
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

Table 15. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}^5	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. $V_{DD}=3.3$ V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.

Table 20. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
t_{swapx01}	Swap Control execution time	—	200	—	μs	
t_{swapx02}	• control code 0x02	—	70	150	μs	
t_{swapx04}	• control code 0x04	—	70	150	μs	
t_{swapx08}	• control code 0x08	—	—	30	μs	
$t_{\text{pgmpart32k}}$	Program Partition for EEPROM execution time • 32 KB FlexNVM	—	70	—	ms	
t_{setramff}	Set FlexRAM Function execution time: • Control Code 0xFF	—	50	—	μs	
t_{setram8k}	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{\text{setram32k}}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{\text{eewr8bers}}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
t_{eewr8b8k}	Byte-write to FlexRAM execution time: • 8 KB EEPROM backup	—	340	1700	μs	
$t_{\text{eewr8b16k}}$	• 16 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr8b32k}}$	• 32 KB EEPROM backup	—	475	2000	μs	
Word-write to FlexRAM for EEPROM operation						
$t_{\text{eewr16bers}}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
$t_{\text{eewr16b8k}}$	Word-write to FlexRAM execution time: • 8 KB EEPROM backup	—	340	1700	μs	
$t_{\text{eewr16b16k}}$	• 16 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr16b32k}}$	• 32 KB EEPROM backup	—	475	2000	μs	
Longword-write to FlexRAM for EEPROM operation						
$t_{\text{eewr32bers}}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
$t_{\text{eewr32b8k}}$	Longword-write to FlexRAM execution time: • 8 KB EEPROM backup	—	545	1950	μs	
$t_{\text{eewr32b16k}}$	• 16 KB EEPROM backup	—	630	2050	μs	
$t_{\text{eewr32b32k}}$	• 32 KB EEPROM backup	—	810	2250	μs	

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash high voltage current behaviors

Table 21. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	—	years	
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	—	years	
n _{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
t _{nvmretd10k}	Data retention after up to 10 K cycles	5	50	—	years	
t _{nvmretd1k}	Data retention after up to 1 K cycles	20	100	—	years	
n _{nvmcycd}	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
t _{nvmreteee100}	Data retention up to 100% of write endurance	5	50	—	years	
t _{nvmreteee10}	Data retention up to 10% of write endurance	20	100	—	years	
n _{nvmwree16}	Write endurance					3
n _{nvmwree128}	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
n _{nvmwree512}	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
n _{nvmwree4k}	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
n _{nvmwree8k}	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$.
3. Write endurance represents the number of writes to each FlexRAM location at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

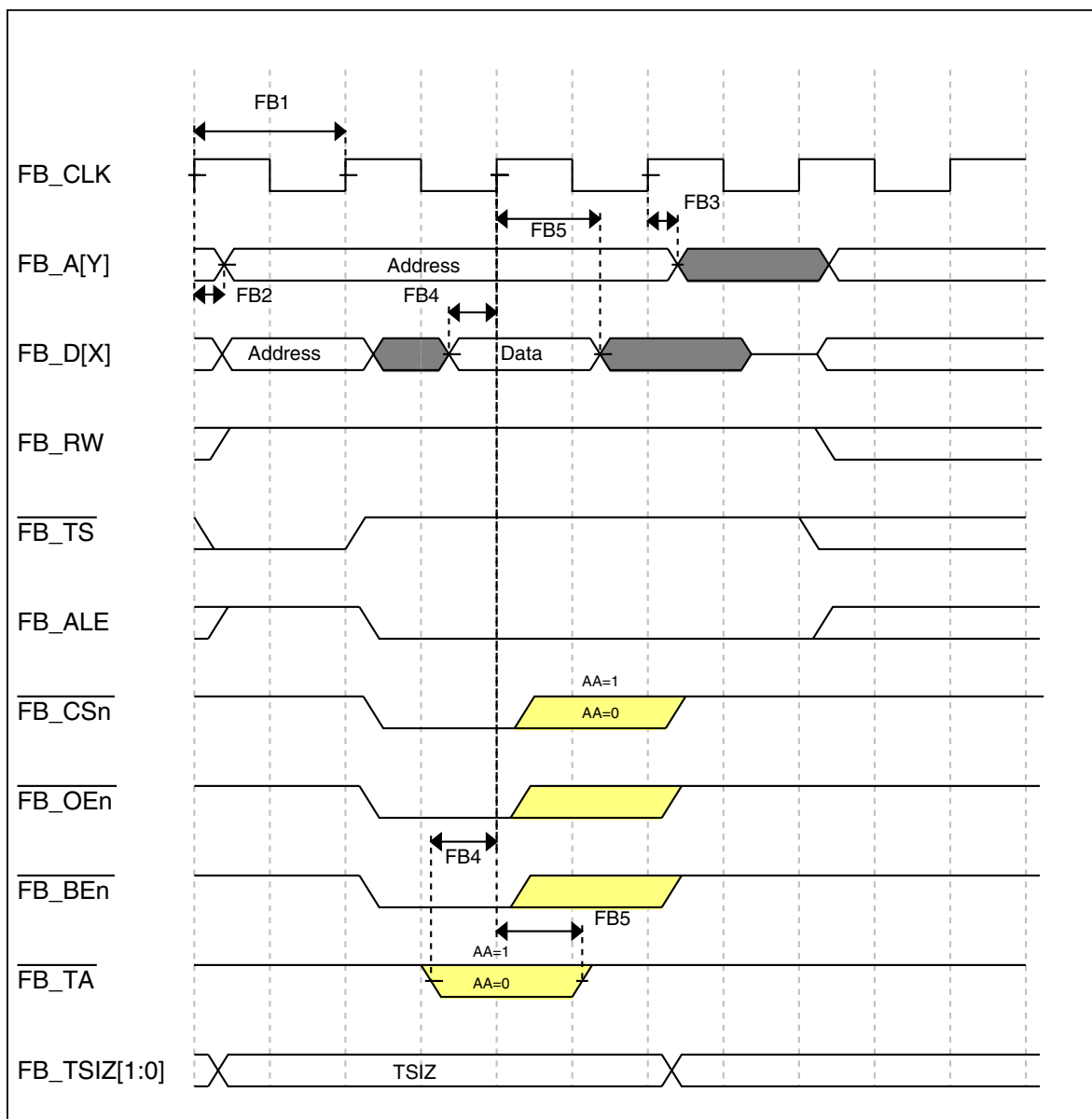


Figure 12. FlexBus read timing diagram

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 26](#) and [Table 27](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 28](#) and [Table 29](#).

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 26. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} - V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} - V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	16-bit differential mode - All other modes	V _{REFL} V _{REFL}	— —	31/32 * V _{REFH} V _{REFH}	V	
C _{ADIN}	Input capacitance	16-bit mode 8-/10-/12-bit modes	— —	8 4	10 5	pF	
R _{ADIN}	Input resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance	13-/12-bit modes f _{ADCK} < 4 MHz	—	—	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C _{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5

Table continues on the next page...

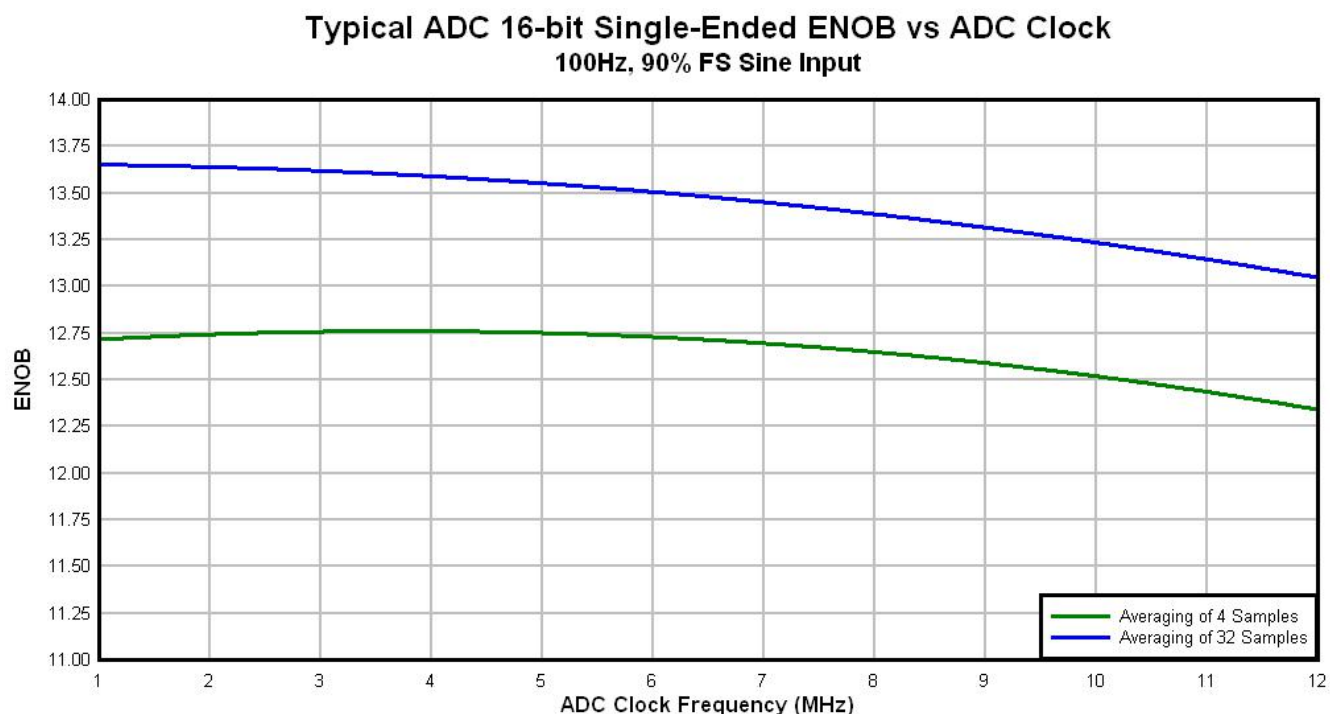


Figure 16. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.1.3 16-bit ADC with PGA operating conditions

Table 28. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V _{REFPGA}	PGA ref voltage		V _{REF_OU} T	V _{REF_OU} T	V _{REF_OU} T	V	2, 3
V _{ADIN}	Input voltage		V _{SSA}	—	V _{DDA}	V	
V _{CM}	Input Common Mode range		V _{SSA}	—	V _{DDA}	V	
R _{PGAD}	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	— — —	128 64 32	— — —	kΩ	IN+ to IN- ⁴
R _{AS}	Analog source resistance		—	100	—	Ω	5
T _S	ADC sampling time		1.25	—	—	μs	6

Table continues on the next page...

Table 29. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
SFDR	Spurious free dynamic range	- Gain=1 - Gain=64	85 53	105 88	— —	dB dB	16-bit differential mode, Average=32, $f_{in}=100\text{Hz}$
ENOB	Effective number of bits	- Gain=1, Average=4 - Gain=64, Average=4 - Gain=1, Average=32 - Gain=2, Average=32 - Gain=4, Average=32 - Gain=8, Average=32 - Gain=16, Average=32 - Gain=32, Average=32 - Gain=64, Average=32	11.6 7.2 12.8 11.0 7.9 7.3 6.8 6.8 7.5	13.4 9.6 14.5 14.3 13.8 13.1 12.5 11.5 10.6	— — — — — — — — —	bits bits bits bits bits bits bits bits bits	16-bit differential mode, $f_{in}=100\text{Hz}$
SINAD	Signal-to-noise plus distortion ratio	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	

- Typical values assume $V_{DDA}=3.0\text{V}$, $\text{Temp}=25^{\circ}\text{C}$, $f_{\text{ADCK}}=6\text{MHz}$ unless otherwise stated.
- This current is a PGA module adder, in addition to ADC conversion currents.
- Between $\text{IN}+$ and $\text{IN}-$. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V_{CM}) and the PGA gain.
- Gain = 2^{PGAG}
- After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
- Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

6.6.2 CMP and 6-bit DAC electrical specifications

Table 30. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
$I_{\text{DDL S}}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V_{AIN}	Analog input voltage	$V_{\text{SS}} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_{H}	Analog comparator hysteresis ¹ - CR0[HYSTCTR] = 00 - CR0[HYSTCTR] = 01 - CR0[HYSTCTR] = 10 - CR0[HYSTCTR] = 11	— — — —	5 10 20 30	— — — —	mV mV mV mV

Table continues on the next page...

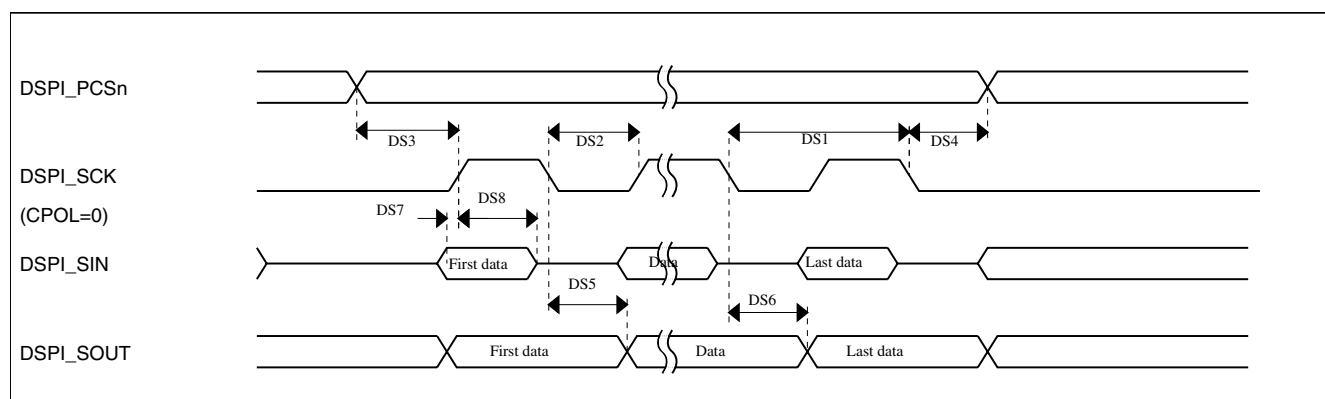


Figure 21. DSPI classic SPI timing — master mode

Table 40. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns </td
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns

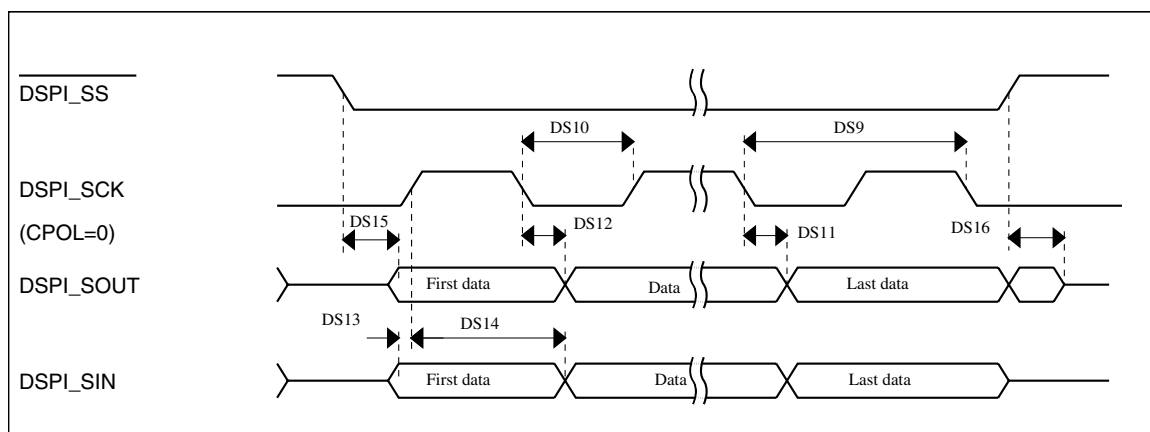


Figure 22. DSPI classic SPI timing — slave mode

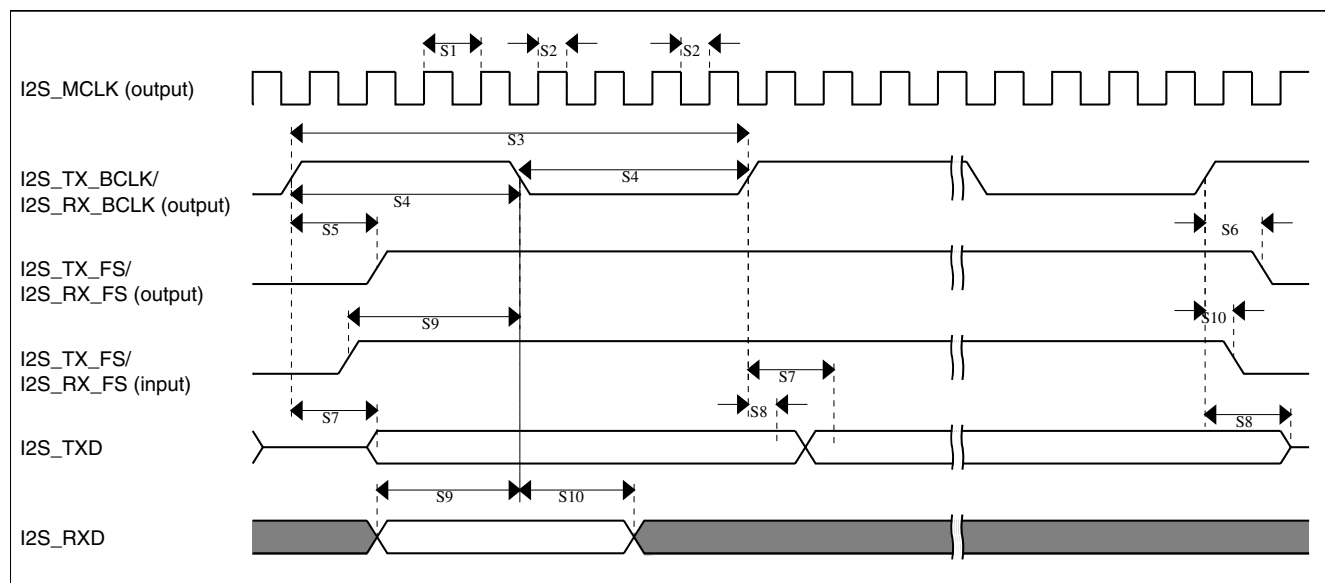


Figure 25. I2S/SAI timing — master modes

Table 44. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

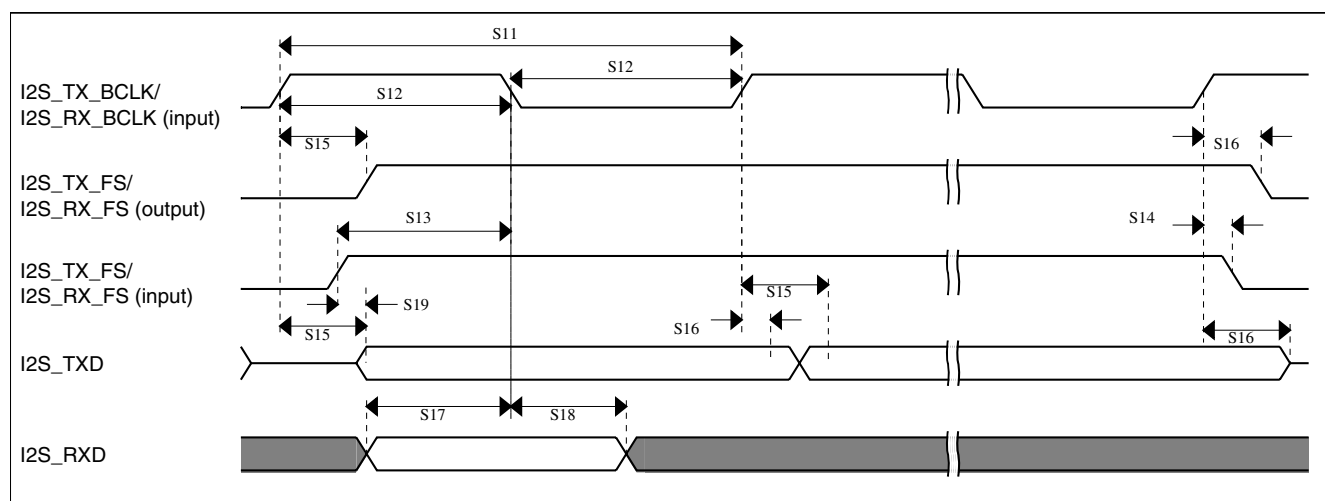


Figure 26. I2S/SAI timing — slave modes

6.8.9.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 45. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	53	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

Pinout

121 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C8	72	PTC2	ADC0_SE4b/ CMP1_IN0/ TS10_CH15	ADC0_SE4b/ CMP1_IN0/ TS10_CH15	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1	FB_AD12	I2S0_TX_FS		
B8	73	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK		
—	74	VSS	VSS	VSS								
—	75	VDD	VDD	VDD								
A8	76	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
D7	77	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0	FB_AD10	CMP0_OUT		
C7	78	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_ BCLK	FB_AD9	I2S0_MCLK		
B7	79	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS	FB_AD8			
A7	80	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8			I2S0_MCLK	FB_AD7			
D6	81	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_ BCLK	FB_AD6	FTM2_FLT0		
C6	82	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL		I2S0_RX_FS	FB_AD5			
C5	83	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD1	FB_RW_b			
B6	84	PTC12	DISABLED		PTC12		UART4_RTS_ b		FB_AD27			
A6	85	PTC13	DISABLED		PTC13		UART4_CTS_ b		FB_AD26			
A5	86	PTC14	DISABLED		PTC14		UART4_RX		FB_AD25			
B5	87	PTC15	DISABLED		PTC15		UART4_TX		FB_AD24			
—	88	VSS	VSS	VSS								
—	89	VDD	VDD	VDD								
D5	90	PTC16	DISABLED		PTC16		UART3_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_ b			
C4	91	PTC17	DISABLED		PTC17		UART3_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_ b			
B4	92	PTC18	DISABLED		PTC18		UART3_RTS_ b		FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b			
A4	—	PTC19	DISABLED		PTC19		UART3_CTS_ b		FB_CS3_b/ FB_BE7_0_b	FB_TA_b		
D4	93	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_ b		FB_ALE/ FB_CS1_b/ FB_TS_b			

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	PTC19	PTC14	PTC13	PTC8	PTC4/ LLWU_P8	NC	NC	NC	A
B	NC	PTD6/ LLWU_P15	PTD3	PTC18	PTC15	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	NC	B
C	NC	NC	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	NC	C
D	NC	NC	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	PTB8	D
E	NC	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	VDD	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	USB0_DP	USB0_DM	PTE6	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	PTB6	F
G	VOOUT33	VREGIN	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	ADC0_DP1	ADC0_DM1	NC	NC	PTE24	PTE26	PTE4/ LLWU_P2	PTA1	PTA3	PTA17	NC	H
J	ADC1_DP	ADC1_DM	NC	NC	PTE25	PTA0	PTA2	PTA4/ LLWU_P3	NC	PTA16	RESET_b	J
K	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	NC	NC	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	XTAL32	EXTAL32	VSS	RTC WAKEUP_B	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 30. K20 121 MAPBGA Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 48. Revision History

Rev. No.	Date	Substantial Changes
1	3/2012	Initial public release

Table continues on the next page...

Table 48. Revision History (continued)

Rev. No.	Date	Substantial Changes
2	4/2012	- Replaced TBDs throughout. - Updated "Power consumption operating behaviors" table. - Updated "ADC electrical specifications" section. - Updated "VREF full-range operating behaviors" table. - Updated "I2S/SAI Switching Specifications" section. - Updated "TSI electrical specifications" table.
3	11/2012	- Updated orderable part numbers. - Updated the maximum input voltage (V_{ADIN}) specification in the "16-bit ADC operating conditions" section. - Updated the maximum I_{DDstby} specification in the "USB VREG electrical specifications" section.

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