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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	·
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f74-e-l

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FIGURE 1-2: PIC16F74 AND PIC16F77 BLOCK DIAGRAM

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1. The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral feature section.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page	
Bank 0												
00h ⁽⁴⁾	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96	
01h	TMR0	Timer0 Mo	odule Registe	er						xxxx xxxx	45, 96	
02h ⁽⁴⁾	PCL	Program 0	Counter (PC)		0000 0000	26, 96						
03h ⁽⁴⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96	
04h ⁽⁴⁾	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27, 96	
05h	PORTA	—	_	PORTA Dat	ta Latch when	written: POF	RTA pins wh	en read		0x 0000	32, 96	
06h	PORTB	PORTB D	ata Latch wh	nen written: F	ORTB pins w	hen read				xxxx xxxx	34, 96	
07h	PORTC	PORTC D	ata Latch wh	nen written: F	PORTC pins w	hen read				xxxx xxxx	35, 96	
08h ⁽⁵⁾	PORTD	PORTD D	ata Latch wh	nen written: F	PORTD pins w	hen read				xxxx xxxx	36, 96	
09h ⁽⁵⁾	PORTE	_	—	_	—	_	RE2	RE1	RE0	xxx	39, 96	
0Ah ^(1,4)	PCLATH	—	_	_	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	26, 96	
0Bh ⁽⁴⁾	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	21, 96	
0Ch	PIR1	PSPIF ⁽³⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	23, 96	
0Dh	PIR2	_	_	_	_	_	_	_	CCP2IF	0	24, 96	
0Eh	TMR1L	Holding R	egister for th	e Least Sign	ificant Byte of	the 16-bit TM	VR1 Registe	er		xxxx xxxx	50, 96	
0Fh	TMR1H	Holding R	egister for th	e Most Signi	ficant Byte of	the 16-bit TN	IR1 Registe	r		xxxx xxxx	50, 96	
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	47, 96	
11h	TMR2	Timer2 Mo	dule Registe	er	•	•	-			0000 0000	52, 96	
12h	T2CON		TOUTPS3	TOUTPS2	TOUTPS	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	52, 96	
13h	SSPBUF	Synchrono	ous Serial Po	ort Receive E	Buffer/Transmi	it Register				xxxx xxxx	64, 68, 96	
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	61,96	
15h	CCPR1L	Capture/C	ompare/PW	M Register1	(LSB)					xxxx xxxx	56, 96	
16h	CCPR1H	Capture/C	ompare/PW	M Register1	(MSB)					XXXX XXXX	56, 96	
17h	CCP1CON		_	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	54, 96	
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	70, 96	
19h	TXREG	USART TI	ransmit Data	Register						0000 0000	74, 96	
1Ah	RCREG	USART R	eceive Data	Register						0000 0000	76, 96	
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	58, 96	
1Ch	CCPR2H	Capture/C	ompare/PW	M Register2	(MSB)					xxxx xxxx	58, 96	
1Dh	CCP2CON		_	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	54, 96	
1Eh	ADRES	A/D Resul	t Register By	/te						xxxx xxxx	88, 96	
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/ DONE	_	ADON	0000 00-0	83, 96	

TABLE 2-1:SPECIAL FUNCTION REGISTER SUMMARY

 $\label{eq:legend: Legend: Legend: u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. \\ Shaded locations are unimplemented, read as '0'.$

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

2: Other (non power-up) RESETS include external RESET through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: This bit always reads as a '1'.

3.3 Reading the FLASH Program Memory

A program memory location may be read by writing two bytes of the address to the PMADR and PMADRH registers and then setting control bit RD (PMCON1<0>). Once the read control bit is set, the microcontroller will use the next two instruction cycles to read the data. The data is available in the PMDATA and PMDATH registers after the second NOP instruction. Therefore, it can be read as two bytes in the following instructions. The PMDATA and PMDATH registers will hold this value until the next read operation.

3.4 Operation During Code Protect

FLASH program memory has its own code protect mechanism. External Read and Write operations by programmers are disabled if this mechanism is enabled.

The microcontroller can read and execute instructions out of the internal FLASH program memory, regardless of the state of the code protect configuration bits.

	BSF	STATUS, RP1	;
	BCF	STATUS, RP0	; Bank 2
	MOVF	ADDRH, W	;
	MOVWF	PMADRH	; MSByte of Program Address to read
	MOVF	ADDRL, W	;
	MOVWF	PMADR	; LSByte of Program Address to read
	BSF	STATUS, RP0	; Bank 3 Required
Required Sequence	BSF NOP NOP	PMCON1, RD	; EEPROM Read Sequence ; memory is read in the next two cycles after BSF PMCON1,RD ;
	BCF	STATUS, RPO	; Bank 2
	MOVF	PMDATA, W	; W = LSByte of Program PMDATA
	MOVF	PMDATH, W	; W = MSByte of Program PMDATA

EXAMPLE 3-1: FLASH PROGRAM READ

TABLE 3-1: REGISTERS ASSOCIATED WITH PROGRAM FLASH

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
10Dh	PMADR	Address I	Register Lo	ow Byte						xxxx xxxx	uuuu uuuu
10Fh	PMADRH	_	_	—	Address I	xxxx xxxx	uuuu uuuu				
10Ch	PMDATA	Data Reg	ister Low I	Byte		xxxx xxxx	uuuu uuuu				
10Eh	PMDATH	_	_	Data Reg	ister High	xxxx xxxx	uuuu uuuu				
18Ch	PMCON1	(1)		_	_		10	10			

Legend: x = unknown, u = unchanged, r = reserved, - = unimplemented read as '0'. Shaded cells are not used during FLASH access. **Note 1:** This bit always reads as a '1'.

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data.

TABLE 4-3: PORTB FUNCTIONS

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

TABLE 4-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB	Data Directio	on Registe	er					1111 1111	1111 1111
81h, 181h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

4.6 Parallel Slave Port

The Parallel Slave Port (PSP) is not implemented on the PIC16F73 or PIC16F76.

PORTD operates as an 8-bit wide Parallel Slave Port, or Microprocessor Port, when control bit PSPMODE (TRISE<4>) is set. In Slave mode, it is asynchronously readable and writable by an external system using the read control input pin RE0/RD, the write control input pin RE1/WR, and the chip select control input pin RE2/CS.

The PSP can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting bit PSPMODE enables port pin RE0/RD to be the RD input, RE1/WR to be the WR input and RE2/CS to be the CS (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (i.e., set). The A/D port configuration bits PCFG3:PCFG0 (ADCON1<3:0>) must be set to configure pins RE2:RE0 as digital I/O.

There are actually two 8-bit latches, one for data output (external reads) and one for data input (external writes). The firmware writes 8-bit data to the PORTD output data latch and reads data from the PORTD input data latch (note that they have the same address). In this mode, the TRISD register is ignored, since the external device is controlling the direction of data flow.

An external write to the PSP occurs when the \overline{CS} and \overline{WR} lines are both detected low. Firmware can read the actual data on the PORTD pins during this time. When either the CS or WR lines become high (level triggered), the data on the PORTD pins is latched, and the Input Buffer Full (IBF) status flag bit (TRISE<7>) and interrupt flag bit PSPIF (PIR1<7>) are set on the Q4 clock cycle, following the next Q2 cycle to signal the write is complete (Figure 4-9). Firmware clears the IBF flag by reading the latched PORTD data, and clears the PSPIF bit.

The Input Buffer Overflow (IBOV) status flag bit (TRISE<5>) is set if an external write to the PSP occurs while the IBF flag is set from a previous external write. The previous PORTD data is overwritten with the new data. IBOV is cleared by reading PORTD and clearing IBOV.

A read from the PSP occurs when both the \overline{CS} and \overline{RD} lines are detected low. The data in the PORTD output latch is output to the PORTD pins. The Output Buffer Full (OBF) status flag bit (TRISE<6>) is cleared immediately (Figure 4-10), indicating that the PORTD latch is being read, or has been read by the external bus. If firmware writes new data to the output latch during this time, it is immediately output to the PORTD pins, but OBF will remain cleared.

When either the \overline{CS} or \overline{RD} pins are detected high, the PORTD outputs are disabled, and the interrupt flag bit PSPIF is set on the Q4 clock cycle following the next Q2 cycle, indicating that the read is complete. OBF remains low until firmware writes new data to PORTD.

When not in PSP mode, the IBF and OBF bits are held clear. Flag bit IBOV remains unchanged. The PSPIF bit must be cleared by the user in firmware; the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).

FIGURE 4-8:

PORTD AND PORTE BLOCK DIAGRAM (PARALLEL SLAVE PORT)



6.1 **Timer1 Operation in Timer Mode**

Timer mode is selected by clearing the TMR1CS (T1CON<1>) bit. In this mode, the input clock to the timer is Fosc/4. The synchronize control bit T1SYNC (T1CON<2>) has no effect, since the internal clock is always in sync.

6.2 **Timer1 Counter Operation**

Timer1 may operate in Asynchronous or Synchronous mode, depending on the setting of the TMR1CS bit.

When Timer1 is being incremented via an external source, increments occur on a rising edge. After Timer1 is enabled in Counter mode, the module must first have a falling edge before the counter begins to increment.



6.3 **Timer1 Operation in Synchronized Counter Mode**

Counter mode is selected by setting bit TMR1CS. In this mode, the timer increments on every rising edge of clock input on pin RC1/T1OSI/CCP2, when bit T1OSCEN is set, or on pin RC0/T1OSO/T1CKI, when bit T1OSCEN is cleared.

If TISYNC is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple counter.

In this configuration, during SLEEP mode, Timer1 will not increment even if the external clock is present, since the synchronization circuit is shut-off. The prescaler, however, will continue to increment.



FIGURE 6-2: TIMER1 BLOCK DIAGRAM

		Fosc = 20 M	lHz		Fosc = 16 M	IHz		Fosc = 10 M	lHz
BAUD RATE	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)
1200	1,221	1.73%	255	1,202	0.16%	207	1,202	0.16%	129
2400	2,404	0.16%	129	2,404	0.16%	103	2,404	0.16%	64
9600	9,470	-1.36%	32	9,615	0.16%	25	9,766	1.73%	15
19,200	19,531	1.73%	15	19,231	0.16%	12	19,531	1.73%	7
38,400	39,063	1.73%	7	35,714	-6.99%	6	39,063	1.73%	3
57,600	62,500	8.51%	4	62,500	8.51%	3	52,083	-9.58%	2
76,800	78,125	1.73%	3	83,333	8.51%	2	78,125	1.73%	1
96,000	104,167	8.51%	2	83,333	-13.19%	2	78,125	-18.62%	1
115,200	104,167	-9.58%	2	125,000	8.51%	1	78,125	-32.18%	1
250,000	312,500	25.00%	0	250,000	0.00%	0	156,250	-37.50%	0

TABLE 10-3:BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

		Fosc = 4 MI	Hz		Fosc = 3.6864	MHz	Fosc = 3.579545 MHz			
BAUD RATE	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	
300	300	0.16%	207	300	0.00%	191	301	0.23%	185	
1200	1,202	0.16%	51	1,200	0.00%	47	1,190	-0.83%	46	
2400	2,404	0.16%	25	2,400	0.00%	23	2,432	1.32%	22	
9600	8,929	-6.99%	6	9,600	0.00%	5	9,322	-2.90%	5	
19,200	20,833	8.51%	2	19,200	0.00%	2	18,643	-2.90%	2	
38,400	31,250	-18.62%	1	28,800	-25.00%	1	27,965	-27.17%	1	
57,600	62,500	8.51%	0	57,600	0.00%	0	55,930	-2.90%	0	
76,800	62,500	-18.62%	0	—	_	_	—	—	—	

TABLE 10-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

		Fosc = 20 M	Hz		Fosc = 16 M	Hz	Fosc = 10 MHz			
BAUD RATE	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	
2400	_	—	_	—	—	_	2,441	1.73%	255	
9600	9,615	0.16%	129	9,615	0.16%	103	9,615	0.16%	64	
19,200	19,231	0.16%	64	19,231	0.16%	51	18,939	-1.36%	32	
38,400	37,879	-1.36%	32	38,462	0.16%	25	39,063	1.73%	15	
57,600	56,818	-1.36%	21	58,824	2.12%	16	56,818	-1.36%	10	
76,800	78,125	1.73%	15	76,923	0.16%	12	78,125	1.73%	7	
96,000	96,154	0.16%	12	100,000	4.17%	9	89,286	-6.99%	6	
115,200	113,636	-1.36%	10	111,111	-3.55%	8	125,000	8.51%	4	
250,000	250,000	0.00%	4	250,000	0.00%	3	208,333	-16.67%	2	
300,000	312,500	4.17%	3	333,333	11.11%	2	312,500	4.17%	1	

BAUD		Fosc = 4 MH	Iz	F	osc = 3.6864	MHz	Fosc = 3.579545 MHz			
RATE (K)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	
1200	1,202	0.16%	207	1,200	0.00%	191	1,203	0.23%	185	
2400	2,404	0.16%	103	2,400	0.00%	95	2,406	0.23%	92	
9600	9,615	0.16%	25	9,600	0.00%	23	9,727	1.32%	22	
19,200	19,231	0.16%	12	19,200	0.00%	11	18,643	-2.90%	11	
38,400	35,714	-6.99%	6	38,400	0.00%	5	37,287	-2.90%	5	
57,600	62,500	8.51%	3	57,600	0.00%	3	55,930	-2.90%	3	
76,800	83,333	8.51%	2	76,800	0.00%	2	74,574	-2.90%	2	
96,000	83,333	-13.19%	2	115,200	20.00%	1	111,861	16.52%	1	
115,200	125,000	8.51%	1	115,200	0.00%	1	111,861	-2.90%	1	
250,000	250,000	0.00%	0	230,400	-7.84%	0	223,722	-10.51%	0	



FIGURE 10-6: SYNCHRONOUS TRANSMISSION

FIGURE 10-7: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



TABLE 10-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tr	ansmit R	egister						0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Generat	or Registe	r					0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous master transmission.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F73/76 devices; always maintain these bits clear.

12.10 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON, has two bits to indicate the type of RESET that last occurred.

Bit0 is Brown-out Reset Status bit, BOR. Bit BOR is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see

TABLE 12-3: TIME-OUT IN VARIOUS SITUATIONS

if bit $\overline{\text{BOR}}$ cleared, indicating a Brown-out Reset occurred. When the Brown-out Reset is disabled, the state of the $\overline{\text{BOR}}$ bit is unpredictable.

Bit1 is POR (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

Oppillator Configuration	Power	-up	Brown out	Wake-up from
Oscillator Configuration	PWRTE = 0	PWRTE = 1	Brown-out	SLEEP
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	72 ms + 1024 Tosc	1024 Tosc
RC	72 ms	_	72 ms	_

TABLE 12-4: STATUS BITS AND THEIR SIGNIFICANCE

POR (PCON<1>)	BOR (PCON<0>)	TO (STATUS<4>)	PD (STATUS<3>)	Significance	
0	х	1	1	Power-on Reset	
0	x	0	x	Illegal, TO is set on POR	
0	х	x	0	Illegal, PD is set on POR	
1	0	1	1	Brown-out Reset	
1	1	0	1	WDT Reset	
1	1	0	0	WDT Wake-up	
1	1	u	u	MCLR Reset during normal operation	
1	1	1	0	MCLR Reset during SLEEP or interrupt wake-up from SLEEP	

TABLE 12-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	0x
MCLR Reset during normal operation	000h	000u uuuu	uu
MCLR Reset during SLEEP	000h	0001 0uuu	uu
WDT Reset	000h	0000 luuu	uu
WDT Wake-up	PC + 1	uuu0 0uuu	uu
Brown-out Reset	000h	0001 luuu	u0
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuul 0uuu	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

14.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PICmicro MCUs and can be used to develop for this and other PICmicro microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming[™] protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in realtime.

14.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode, the PRO MATE II device programmer can read, verify, or program PICmicro devices. It can also set code protection in this mode.

14.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PICmicro devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

14.11 PICDEM 1 Low Cost PICmicro Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44, All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE incircuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

14.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I^2C^{TM} bus and separate headers for connection to an LCD module and a keypad.

15.3 Timing Parameter Symbology

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS		3. Tcc:st	(I ² C specifications only)
2. TppS		4. Ts	(I ² C specifications only)
Т			
F	Frequency	Т	Time
Lowercase	e letters (pp) and their meanings:		
рр			
сс	CCP1	OSC	OSC1
ck	CLKOUT	rd	RD
cs	CS	rw	RD or WR
di	SDI	SC	SCK
do	SDO	SS	SS
dt	Data in	tO	ТОСКІ
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR
Uppercase	e letters and their meanings:	-	
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I ² C only			
AA	output access	High	High
BUF	Bus free	Low	Low
TCC:ST (I ²	C specifications only)		
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		









TABLE 15-2:	CLKOUT AND I/O TIMING REQUIREMENTS
-------------	---

Param No.	Symbol	Charact	Min	Тур†	Мах	Units	Conditions	
10*	TosH2ckL	OSC1↑ to CLKOUT↓		_	75	200	ns	(Note 1)
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	(Note 1)
12*	TckR	CLKOUT rise time		—	35	100	ns	(Note 1)
13*	TckF	CLKOUT fall time		—	35	100	ns	(Note 1)
14*	TckL2ioV	CLKOUT↓ to Port out vali	d	—	_	0.5TCY + 20	ns	(Note 1)
15*	TioV2ckH	Port in valid before CLKO	Port in valid before CLKOUT↑			_	ns	(Note 1)
16*	TckH2iol	Port in hold after CLKOUT	0	_	—	ns	(Note 1)	
17*	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port	out valid	—	100	255	ns	
18*	TosH2iol	OSC1 [↑] (Q2 cycle) to	Standard (F)	100	_	_	ns	
		Port input invalid (I/O in hold time)	Extended (LF)	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC11	(I/O in setup time)	0	_	—	ns	
20*	TioR	Port output rise time	Standard (F)	—	10	40	ns	
			Extended (LF)	—	_	145	ns	
21*	TioF	Port output fall time	Standard (F)	—	10	40	ns	
			Extended (LF)	—	—	145	ns	
22††*	Tinp	INT pin high or low time		Тсү	_	—	ns	
23††*	Trbp	RB7:RB4 change INT hig	n or low time	Тсү	_	_	ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

 $\mbox{ ++ } \mbox{ These parameters are asynchronous events, not related to any internal clock edges. } \label{eq:these parameters}$

Note 1: Measurements are taken in RC mode, where CLKOUT output is 4 x Tosc.

*

TABLE 15-12: A/D CONVERTER CHARACTERISTICS: PIC16F7X (INDUSTRIAL, EXTENDED) PIC16LF7X (INDUSTRIAL)

Param No.	Sym	Characteristic		Min	Тур†	Мах	Units	Conditions
A01	NR	Resolution	PIC16F7X		_	8 bits	bit	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$
			PIC16LF7X	—	_	8 bits	bit	VREF = VDD = 2.2V
A02	Eabs	Total absolute e	rror	—	—	< ±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A03	EIL	Integral linearity	error	—	_	< ±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A04	Edl	Differential linearity error		—	-	< ±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A05	Efs	Full scale error		—	_	< ±1	LSb	VREF = VDD = 5.12V, $VSS \le VAIN \le VREF$
A06	Eoff	Offset error		—	—	< ±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A10	—	Monotonicity (Note 3)		—	guaranteed	—	_	$VSS \leq VAIN \leq VREF$
A20	Vref	Reference voltage		2.5 2.2		5.5 5.5	V V	-40°C to +125°C 0°C to +125°C
A25	VAIN	Analog input vol	tage	Vss - 0.3	_	Vref + 0.3	V	
A30	ZAIN	Recommended impedance of analog voltage source		—	—	10.0	kΩ	
A40	IAD	A/D conversion	PIC16F7X	—	180	—	μΑ	Average current
	current (VDD)		PIC16LF7X	—	90	—	μA	consumption when A/D is on (Note 1) .
A50	IREF	VREF input current (Note 2)		N/A 		±5 500	μΑ μΑ	During VAIN acquisition. During A/D Conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from the RA3 pin or the VDD pin, whichever is selected as a reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.









28-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)



	Units	INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.050			1.27	
Overall Height	Α	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	φ	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.013	0.23	0.28	0.33
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013 Drawing No. C04-052

5

44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)



	Units	INCHES			MILLIMETERS*		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	р		.031			0.80	
Pins per Side	n1		11			11	
Overall Height	Α	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039		1.00		
Foot Angle	¢	0	3.5	7	0	3.5	7
Overall Width	Е	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	С	.004	.006	.008	0.09	0.15	0.20
Lead Width	В	.012	.015	.017	0.30	0.38	0.44
Pin 1 Corner Chamfer	СН	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-026 Drawing No. C04-076

PIC16F7X

S

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