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### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f76-e-ss

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 1											
80h <sup>(4)</sup>	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	ot a physica	al register)	0000 0000	27, 96
81h	OPTION_REG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	20, 44, 96
82h <sup>(4)</sup>	PCL	Program C	Counter's (PC	C) Least Sigr	nificant Byte				-	0000 0000	26, 96
83h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
84h <sup>(4)</sup>	FSR	Indirect da	idirect data memory address pointer								27, 96
85h	TRISA	_	PORTA Data Direction Register								32, 96
86h	TRISB	PORTB D	ata Direction	Register						1111 1111	34, 96
87h	TRISC	PORTC D	ata Direction	Register						1111 1111	35, 96
88h <sup>(5)</sup>	TRISD	PORTD D	ata Direction	Register						1111 1111	36, 96
89h <b>(5)</b>	TRISE	IBF	IBF OBF IBOV PSPMODE — PORTE Data Direction Bits								38, 96
8Ah <sup>(1,4)</sup>	PCLATH									0 0000	21, 96
8Bh <sup>(4)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
8Ch	PIE1	PSPIE <sup>(3)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	22, 96
8Dh	PIE2	_		_	_	_	_		CCP2IE	0	24, 97
8Eh	PCON	—		—	—		—	POR	BOR	qq	25, 97
8Fh		Unimplem	ented							_	_
90h	_	Unimplem	ented							_	_
91h	_	Unimplem	ented							_	—
92h	PR2	Timer2 Pe	riod Registe	r						1111 1111	52, 97
93h	SSPADD	Synchrono	ous Serial Po	ort (I <sup>2</sup> C mode	e) Address Re	gister				0000 0000	68, 97
94h	SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	60, 97
95h	—	Unimplem	ented							_	_
96h		Unimplem	ented							_	_
97h	—	Unimplem	ented				_			_	_
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	69, 97
99h	SPBRG	Baud Rate	e Generator I	Register						0000 0000	71, 97
9Ah	—	Unimplem	ented							_	
9Bh	—	Unimplem	ented							_	
9Ch	—	Unimplem	ented							—	
9Dh	—	Unimplem	ented							_	
9Eh	—	Unimplem	ented							_	
9Fh	ADCON1	—	_	—	—	—	PCFG2	PCFG1	PCFG0	000	84, 97

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINU
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 $\label{eq:legend: Legend: Legend: u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.$ Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

2: Other (non power-up) RESETS include external RESET through MCLR and Watchdog Timer Reset. 3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: This bit always reads as a '1'.

TABLE 2-1:	SPECIAL FUNCTION REGISTER SUMMARY	(CONTINUED)
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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 2											
100h <sup>(4)</sup>	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
101h	TMR0	Timer0 Mo	odule Registe	er						xxxx xxxx	45, 96
102h <sup>(4)</sup>	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
103h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
104h <sup>(4)</sup>	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27, 96
105h	_	Unimplem	ented							_	_
106h	PORTB	PORTB D	ata Latch wh	ien written: P	ORTB pins w	hen read				xxxx xxxx	34, 96
107h	_	Unimplem	ented							—	_
108h	_	Unimplem	ented							—	—
109h	_	Unimplem	nimplemented								_
10Ah <sup>(1,4)</sup>	PCLATH	—	— — Write Buffer for the upper 5 bits of the Program Counter							0 0000	21, 96
10Bh <sup>(4)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
10Ch	PMDATA	Data Regi	ster Low Byt	е						xxxx xxxx	29, 97
10Dh	PMADR	Address R	Address Register Low Byte								
10Eh	PMDATH	—	— — Data Register High Byte								29, 97
10Fh	PMADRH	—	— — Address Register High Byte								29, 97
Bank 3											
180h <sup>(4)</sup>	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
181h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	20, 44, 96
182h <sup>(4)</sup>	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
183h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
184h <sup>(4)</sup>	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27, 96
185h	—	Unimplem	ented							_	_
186h	TRISB	PORTB D	ata Direction	Register						1111 1111	34, 96
187h	_	Unimplem	ented							_	_
188h	_	Unimplem	ented							_	_
189h	_	Unimplem	ented							_	—
18Ah <sup>(1,4)</sup>	PCLATH	—	_	—	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	21, 96
18Bh <b><sup>(4)</sup></b>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
18Ch	PMCON1	(6)	—	—	—	—	—	—	RD	10	29, 97
18Dh	—	Unimplem	Unimplemented								
18Eh	—	Reserved	maintain clea	ar						0000 0000	
18Fh	_	Reserved	maintain clea	ar						0000 0000	

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

**Note** 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

2: Other (non power-up) RESETS include external RESET through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: This bit always reads as a '1'.

### 2.2.2.4 PIE1 Register

The PIE1 register contains the individual enable bits for the peripheral interrupts.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

## REGISTER 2-4: PIE1 REGISTER (ADDRESS 8Ch)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE						
	bit 7							bit 0						
bit 7	PSPIE <sup>(1)</sup> : I	PSPIE <sup>(1)</sup> : Parallel Slave Port Read/Write Interrupt Enable bit												
	1 = Enable	s the PSP r	ead/write int	errupt										
	0 = Disable	es the PSP	read/write in	terrupt										
bit 6	ADIE: A/D Converter Interrupt Enable bit													
	1 = Enables the A/D converter interrupt													
	0 = Disables the A/D converter interrupt													
bit 5	RCIE: USA	ART Receive	e Interrupt E	nable bit										
	1 = Enable	s the USAR	T receive in	terrupt										
	0 = Disables the USART receive interrupt													
bit 4	TXIE: USA	RT Transmi	it Interrupt E	nable bit										
	1 = Enable	s the USAR	T transmit ir	nterrupt										
	0 = Disable	es the USAF	RT transmit i	nterrupt										
bit 3	SSPIE: Synchronous Serial Port Interrupt Enable bit													
	1 = Enables the SSP interrupt													
	0 = Disable	es the SSP	interrupt											
bit 2	CCP1IE: C	CP1 Interru	pt Enable bi	t										
	1 = Enable	s the CCP1	interrupt											
	0 = Disable	es the CCP	l interrupt											
bit 1	TMR2IE: T	MR2 to PR2	2 Match Inte	rrupt Enable	e bit									
	1 = Enables the TMR2 to PR2 match interrupt													
	0 = Disable	es the TMR2	2 to PR2 ma	tch interrupt										
bit 0	TMR1IE: T	MR1 Overfl	ow Interrupt	Enable bit										
	1 = Enable	s the TMR1	overflow int	terrupt										
	0 = Disable	es the TMR	l overflow in	terrupt										

Note 1: PSPIE is reserved on 28-pin devices; always maintain this bit clear.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	l bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

### 3.0 **READING PROGRAM MEMORY**

The FLASH Program Memory is readable during normal operation over the entire VDD range. It is indirectly addressed through Special Function Registers (SFR). Up to 14-bit numbers can be stored in memory for use as calibration parameters, serial numbers, packed 7-bit ASCII, etc. Executing a program memory location containing data that forms an invalid instruction results in a NOP.

There are five SFRs used to read the program and memory. These registers are:

- PMCON1
- PMDATA
- PMDATH
- PMADR
- PMADRH

The program memory allows word reads. Program memory access allows for checksum calculation and reading calibration tables.

When interfacing to the program memory block, the PMDATH:PMDATA registers form a two-byte word, which holds the 14-bit data for reads. The PMADRH:PMADR registers form a two-byte word, which holds the 13-bit address of the FLASH location being accessed. These devices can have up to 8K words of program FLASH, with an address range from Oh to 3FFFh. The unused upper bits in both the PMDATH and PMADRH registers are not implemented and read as "0's".

### 3.1 **PMADR**

The address registers can address up to a maximum of 8K words of program FLASH.

When selecting a program address value, the MSByte of the address is written to the PMADRH register and the LSByte is written to the PMADR register. The upper MSbits of PMADRH must always be clear.

#### 3.2 PMCON1 Register

PMCON1 is the control register for memory accesses.

The control bit RD initiates read operations. This bit cannot be cleared, only set, in software. It is cleared in hardware at the completion of the read operation.

#### **REGISTER 3-1:** PMCON1 REGISTER (ADDRESS 18Ch)

	R-1	U-0	U-0	U-0	U-x	U-0	U-0	R/S-0					
	reserved		_	_			_	RD					
	bit 7							bit 0					
bit 7	Reserved: Read as '1'												
bit 6-1	Unimplemented: Read as '0'												
bit 0	RD: Read	Control bit											
	1 = Initiates a FLASH read, RD is cleared in hardware. The RD bit can only be set (not cleared) in software.												
	0 = FLASH	I read comp	leted										
	Legend:												

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

# PIC16F7X

NOTES:

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REGISTER 7-1:	T2CON:	TIMER2 C	ONTROL R	EGISTER (	ADDRESS	12h)							
	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0					
	bit 7							bit 0					
bit 7	Unimple	mented: Rea	ad as '0'										
bit 6-3	TOUTPS	3:TOUTPS0	: Timer2 Out	put Postscale	e Select bits								
	0000 = 1	:1 Postscale											
	0001 = 1	0001 = 1:2 Postscale											
	0010 = 1:3 Postscale												
	•												
	•												
	1111 <b>= 1</b>	:16 Postscal	e										
bit 2	TMR2ON	I: Timer2 On	bit										
	1 = Time	r2 is on											
	0 = Time	r2 is off											
bit 1-0	T2CKPS	1:T2CKPS0:	Timer2 Cloc	k Prescale S	elect bits								
	00 = Pres	scaler is 1											
	01 = Pres	scaler is 4											
	1x = Pres	scaler is 16											
	Legend:												
	R = Reada	able bit	W = W	/ritable bit	U = Unim	plemented l	oit, read as '	0'					

### TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

- n = Value at POR reset

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value PC BC	e on: DR, DR	Valu all c RES	e on other ETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
11h	TMR2	Timer2 M	odule Regis	ster						0000	0000	0000	0000
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000	0000	-000	0000
92h	PR2	Timer2 Pe	eriod Regis	ter						1111	1111	1111	1111

'1' = Bit is set

'0' = Bit is cleared

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F73/76; always maintain these bits clear.

x = Bit is unknown

		Fosc = 20 M	lHz		Fosc = 16 M	IHz		Fosc = 10 M	lHz
BAUD RATE	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)
1200	1,221	1.73%	255	1,202	0.16%	207	1,202	0.16%	129
2400	2,404	0.16%	129	2,404	0.16%	103	2,404	0.16%	64
9600	9,470	-1.36%	32	9,615	0.16%	25	9,766	1.73%	15
19,200	19,531	1.73%	15	19,231	0.16%	12	19,531	1.73%	7
38,400	39,063	1.73%	7	35,714	-6.99%	6	39,063	1.73%	3
57,600	62,500	8.51%	4	62,500	8.51%	3	52,083	-9.58%	2
76,800	78,125	1.73%	3	83,333	8.51%	2	78,125	1.73%	1
96,000	104,167	8.51%	2	83,333	-13.19%	2	78,125	-18.62%	1
115,200	104,167	-9.58%	2	125,000	8.51%	1	78,125	-32.18%	1
250,000	312,500	25.00%	0	250,000	0.00%	0	156,250	-37.50%	0

## TABLE 10-3:BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

	Fosc = 4 MHz			Fosc = 3.6864 MHz			Fosc = 3.579545 MHz		
BAUD RATE	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)
300	300	0.16%	207	300	0.00%	191	301	0.23%	185
1200	1,202	0.16%	51	1,200	0.00%	47	1,190	-0.83%	46
2400	2,404	0.16%	25	2,400	0.00%	23	2,432	1.32%	22
9600	8,929	-6.99%	6	9,600	0.00%	5	9,322	-2.90%	5
19,200	20,833	8.51%	2	19,200	0.00%	2	18,643	-2.90%	2
38,400	31,250	-18.62%	1	28,800	-25.00%	1	27,965	-27.17%	1
57,600	62,500	8.51%	0	57,600	0.00%	0	55,930	-2.90%	0
76,800	62,500	-18.62%	0	—	_	_	—	—	—

## TABLE 10-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

		Fosc = 20 M	Hz		Fosc = 16 M	Hz		Fosc = 10 MI	Hz
BAUD RATE	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)
2400	_	—	_	—	—	_	2,441	1.73%	255
9600	9,615	0.16%	129	9,615	0.16%	103	9,615	0.16%	64
19,200	19,231	0.16%	64	19,231	0.16%	51	18,939	-1.36%	32
38,400	37,879	-1.36%	32	38,462	0.16%	25	39,063	1.73%	15
57,600	56,818	-1.36%	21	58,824	2.12%	16	56,818	-1.36%	10
76,800	78,125	1.73%	15	76,923	0.16%	12	78,125	1.73%	7
96,000	96,154	0.16%	12	100,000	4.17%	9	89,286	-6.99%	6
115,200	113,636	-1.36%	10	111,111	-3.55%	8	125,000	8.51%	4
250,000	250,000	0.00%	4	250,000	0.00%	3	208,333	-16.67%	2
300,000	312,500	4.17%	3	333,333	11.11%	2	312,500	4.17%	1

BAUD	Fosc = 4 MHz			Fosc = 3.6864 MHz			Fosc = 3.579545 MHz		
RATE (K)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)
1200	1,202	0.16%	207	1,200	0.00%	191	1,203	0.23%	185
2400	2,404	0.16%	103	2,400	0.00%	95	2,406	0.23%	92
9600	9,615	0.16%	25	9,600	0.00%	23	9,727	1.32%	22
19,200	19,231	0.16%	12	19,200	0.00%	11	18,643	-2.90%	11
38,400	35,714	-6.99%	6	38,400	0.00%	5	37,287	-2.90%	5
57,600	62,500	8.51%	3	57,600	0.00%	3	55,930	-2.90%	3
76,800	83,333	8.51%	2	76,800	0.00%	2	74,574	-2.90%	2
96,000	83,333	-13.19%	2	115,200	20.00%	1	111,861	16.52%	1
115,200	125,000	8.51%	1	115,200	0.00%	1	111,861	-2.90%	1
250,000	250,000	0.00%	0	230,400	-7.84%	0	223,722	-10.51%	0

### 10.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 10-4. The data is received on the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate, or at FOSC.

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the STOP bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, flag bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/ disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is a double buffered register (i.e., it is a two deep FIFO). It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting to the RSR register. On the detection of the STOP bit of the third byte, if the RCREG register is still full, the overrun error bit OERR (RCSTA<1>) will be set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun bit OERR has to be cleared in software. This is done by resetting the receive logic (CREN is cleared and then set). If bit OERR is set, transfers from the RSR register to the RCREG register are inhibited and no further data will be received, therefore, it is essential to clear error bit OERR if it is set. Framing error bit FERR (RCSTA<2>) is set if a STOP bit is detected as clear. Bit FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG will load bits RX9D and FERR with new values, therefore, it is essential for the user to read the RCSTA register before reading RCREG register, in order not to lose the old FERR and RX9D information.





### 11.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 9.0 TAD per 8-bit conversion. The source of the A/D conversion clock is software selectable. The four possible options for TAD are:

- 2 Tosc (Fosc/2)
- 8 Tosc (Fosc/8)
- 32 Tosc (Fosc/32)
- Internal RC oscillator (2-6 μs)

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time as small as possible, but no less than  $1.6 \,\mu$ s.

### 11.3 Configuring Analog Port Pins

The ADCON1, TRISA and TRISE registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

- Note 1: When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.
  - 2: Analog levels on any pin that is defined as a digital input, but not as an analog input, may cause the digital input buffer to consume current that is out of the device's specification.

## 11.4 A/D Conversions

**Note:** The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

Setting the GO/DONE bit begins an A/D conversion. When the conversion completes, the 8-bit result is placed in the ADRES register, the GO/DONE bit is cleared, and the ADIF flag (PIR<6>) is set.

If both the A/D interrupt bit ADIE (PIE1<6>) and the peripheral interrupt enable bit PEIE (INTCON<6>) are set, the device will wake from SLEEP whenever ADIF is set by hardware. In addition, an interrupt will also occur if the global interrupt bit GIE (INTCON<7>) is set.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The ADRES register will NOT be changed, and the ADIF flag will not be set.

After the GO/DONE bit is cleared at either the end of a conversion, or by firmware, another conversion can be initiated by setting the GO/DONE bit. Users must still take into account the appropriate acquisition time for the application.

## 11.5 A/D Operation During SLEEP

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = '11'). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed, the GO/DONE bit will be cleared, and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an A/D conversion in SLEEP, ensure the SLEEP instruction immediately follows the instruction that sets the GO/DONE bit.

## 11.6 Effects of a RESET

A device RESET forces all registers to their RESET state. The A/D module is disabled and any conversion in progress is aborted. All A/D input pins are configured as analog inputs.

The ADRES register will contain unknown data after a Power-on Reset.

### 12.14 Power-down Mode (SLEEP)

Power-down mode is entered by executing a  $\ensuremath{\mathtt{SLEEP}}$  instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit (STATUS<3>) is cleared, the TO (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or Vss, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and disable external clocks. Pull all I/O pins that are hi-impedance inputs, high or low externally, to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or Vss for lowest current consumption. The contribution from on-chip pull-ups on PORTB should also be considered.

The  $\overline{\text{MCLR}}$  pin must be at a logic high level (VIHMC).

### 12.14.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- 1. External RESET input on MCLR pin.
- 2. Watchdog Timer wake-up (if WDT was enabled).
- 3. Interrupt from INT pin, RB port change or a Peripheral Interrupt.

External MCLR Reset will cause a device RESET. All other events are considered a continuation of program execution and cause a "wake-up". The TO and PD bits in the STATUS register can be used to determine the cause of device RESET. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. The TO bit is cleared if a WDT time-out occurred and caused wake-up.

The following peripheral interrupts can wake the device from SLEEP:

- 1. PSP read or write (PIC16F74/77 only).
- 2. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 3. CCP Capture mode interrupt.
- 4. Special event trigger (Timer1 in Asynchronous mode, using an external clock).
- 5. SSP (START/STOP) bit detect interrupt.
- SSP transmit or receive in Slave mode (SPI/I<sup>2</sup>C).
- 7. USART RX or TX (Synchronous Slave mode).
- 8. A/D conversion (when A/D clock source is RC).

Other peripherals cannot generate interrupts, since during SLEEP, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs, regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

### 12.14.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the TO bit will not be set and PD bits will not be cleared.
- If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake-up from SLEEP. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

; Q1  Q2  Q3  Q4; Q1  Q2  Q3  C	Q4 Q1	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1  Q2  Q3  Q4
0SC1 //////					
CLKOUT <sup>(4)</sup>	Tost <sup>(2)</sup>		\	\/	
INT pin		I I	I I I I	1	1
	×	1 <del> </del>			
(INTCON<1>)		I I	(Note 2)	1 1	
	Processor in	<u> </u> 		1	I
	SLEEP	1	i i	1	1
INSTRUCTION FLOW		i I	i i i i	I I	1
PC X PC X PC+1	X PC+2	χ PC+2	X PC + 2	( <u>0004h</u> )	0005h
Instruction Fetched { Inst(PC) = SLEEP Inst(PC + 1	)	Inst(PC + 2)	1 1 1 1 1 1	Inst(0004h)	Inst(0005h)
Instruction Executed { Inst(PC - 1) SLEEP		Inst(PC + 1)	Dummy cycle	Dummy cycle	Inst(0004h)
Note 1: XT, HS or LP oscillator mode assun	ned.				
2: Tost = 1024 Tosc (drawing not to sc	ale) This delay will not be	there for RC osc m	iode.		
3: GIE = '1' assumed. In this case after '	wake- up, the processor ju	imps to the interrup	ot routine.		
4. CI KOUT is not available in these os	c modes, but shown here f	or timina reference	<b>)</b> .		

### FIGURE 12-12: WAKE-UP FROM SLEEP THROUGH INTERRUPT

12.15 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

### 12.16 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during program/verify. It is recommended that only the 4 Least Significant bits of the ID location are used.

### 12.17 In-Circuit Serial Programming

PIC16F7X microcontrollers can be serially programmed while in the end application circuit. This is simply done, with two lines for clock and data and three other lines for power, ground, and the programming voltage (see Figure 12-13 for an example). This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed. For general information of serial programming, please refer to the In-Circuit Serial Programming (ICSP<sup>™</sup>) Guide (DS30277). For specific details on programming commands and operations for the PIC16F7X devices, please refer to the latest version of the PIC16F7X FLASH Program Memory Programming Specification (DS30324).





# PIC16F7X

CALL	Call Subroutine
Syntax:	[ <i>label</i> ] CALL k
Operands:	$0 \le k \le 2047$
Operation:	(PC)+ 1 $\rightarrow$ TOS, k $\rightarrow$ PC<10:0>, (PCLATH<4:3>) $\rightarrow$ PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven-bit immedi- ate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

CLRWDT	Clear Watchdog Timer
Syntax:	[label] CLRWDT
Operands:	None
Operation: Status Affected:	$\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \\ \overline{TO}, \ \overline{PD} \end{array}$
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.

CLRF	Clear f
Syntax:	[label] CLRF f
Operands:	$0 \le f \le 127$
Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

COMF	Complement f
Syntax:	[ <i>label</i> ] COMF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \ [0,1] \end{array}$
Operation:	$(\overline{f}) \rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow (W) \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

DECF	Decrement f
Syntax:	[label] DECF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \ [0,1] \end{array}$
Operation:	(f) - 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

### 14.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for precompiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

### 14.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multiproject software development tool.

### 14.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft<sup>®</sup> Windows environment were chosen to best make these features available to you, the end user.

## 14.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

## 16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.









## PIC16F7X



FIGURE 16-15: TYPICAL, MINIMUM AND MAXIMUM VOH vs. IOH (VDD = 5V, -40°C TO 125°C)







FIGURE 16-17: TYPICAL, MINIMUM AND MAXIMUM Vol vs. lol (VDD = 5V, -40°C TO 125°C)





## 28-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)



	Units	INCHES		MILLIMETERS*			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.026			0.65	
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	ш	.299	.309	.319	7.59	7.85	8.10
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.396	.402	.407	10.06	10.20	10.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	с	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-150 Drawing No. C04-073

## 40-Lead Plastic Dual In-line (P) - 600 mil (PDIP)



Units		INCHES*		N	<b>IILLIMETERS</b>	6
1 Limits	MIN	NOM	MAX	MIN	NOM	MAX
n		40			40	
р		.100			2.54	
А	.160	.175	.190	4.06	4.45	4.83
A2	.140	.150	.160	3.56	3.81	4.06
A1	.015			0.38		
Е	.595	.600	.625	15.11	15.24	15.88
E1	.530	.545	.560	13.46	13.84	14.22
D	2.045	2.058	2.065	51.94	52.26	52.45
L	.120	.130	.135	3.05	3.30	3.43
С	.008	.012	.015	0.20	0.29	0.38
B1	.030	.050	.070	0.76	1.27	1.78
В	.014	.018	.022	0.36	0.46	0.56
eВ	.620	.650	.680	15.75	16.51	17.27
α	5	10	15	5	10	15
β	5	10	15	5	10	15
	Units    n    P    A    A2    A1    E    D    L    C    B1    B    eB    α    β	Units  MIN    n  P    A  .160    A2  .140    A1  .015    E  .595    E1  .530    D  2.045    L  .120    c  .008    B1  .030    B  .014    eB  .620    α  .5    β  .5	Units  INCHES*    nLimits  MIN  NOM    n  40    P  .100    A  .160  .175    A2  .140  .150    A1  .015	$\begin{tabular}{ c c c c } \hline Units & INCHES* \\ \hline Limits & MIN & NOM & MAX \\ \hline n & 40 \\ \hline P & 100 \\ \hline A & 160 & 175 \\ \hline A & 160 & 160 \\ \hline B & 100 & 160 \\ \hline B & 100 & 160 \\ \hline B & 100 & 150 \\ \hline B & 5 & 100 & 150 \\ \hline B & 5 & 100 & 150 \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c } \hline Vnits & VNCHES* & NN \\ \hline \mbox{n Limits} & MIN & NOM & MAX & MIN \\ \hline \mbox{n } & 40 & & & & & & & & & & & & & & & & & $	$\begin{tabular}{ c c c c c } \hline $\mathbf{V}$ $\mathbf{NCHES}^*$ $\mathbf{MIN}$ $\mathbf{NOM}$ $\mathbf{MAX}$ $\mathbf{MIN}$ $\mathbf{NOM}$ $\mathbf{NOnd}$ $\mathbf{NOM}$ $$

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-011

Drawing No. C04-016

## APPENDIX A: REVISION HISTORY

Version	Date	Revision Description		
A	2000	This is a new data sheet. How- ever, these devices are similar to the PIC16C7X devices found in the PIC16C7X Data Sheet (DS30390) or the PIC16F87X devices (DS30292).		
В	2001	Final data sheet. Includes device characterization data. Addition of extended temperature devices. Addition of 28-pin MLF package. Minor typographic revisions throughout.		

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices in this data sheet are listed in Table B-1.

### TABLE B-1:DEVICE DIFFERENCES

Difference	PIC16F73	PIC16F74	PIC16F76	PIC16F77
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
I/O Ports	3	5	3	5
A/D	5 channels, 8 bits	8 channels, 8 bits	5 channels, 8 bits	8 channels, 8 bits
Parallel Slave Port	no	yes	no	yes
Interrupt Sources	11	12	11	12
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin MLF	40-pin PDIP 44-pin TQFP 44-pin PLCC	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin MLF	40-pin PDIP 44-pin TQFP 44-pin PLCC



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