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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f77-e-p

Email: info@E-XFL.COM

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4.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PICmicro[™] Mid-Range Reference Manual, (DS33023).

4.1 PORTA and the TRISA Register

PORTA is a 6-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= '1') will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= '0') will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other PORTA pins have TTL input levels and full CMOS output drivers.

Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

Note: On a Power-on Reset, these pins are configured as analog inputs and read as '0'.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set, when using them as analog inputs.

BCF	STATUS,	RP0	;	
BCF	STATUS,	RP1	;	Bank0
CLRF	PORTA		;	Initialize PORTA by
			;	clearing output
			;	data latches
BSF	STATUS,	RP0	;	Select Bank 1
MOVLW	0x06		;	Configure all pins
MOVWF	ADCON1		;	as digital inputs
MOVLW	0xCF		;	Value used to
			;	initialize data
			;	direction
MOVWF	TRISA		;	Set RA<3:0> as inputs
			;	RA<5:4> as outputs
			;	TRISA<7:6>are always
			;	read as '0'.

FIGURE 4-1:

BLOCK DIAGRAM OF RA3:RA0 AND RA5 PINS



FIGURE 4-2:

BLOCK DIAGRAM OF RA4/T0CKI PIN



5.2 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

REGISTER 5-1:	OPTION_REG REGISTER
---------------	----------------------------

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1			
	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0			
	bit 7							bit 0			
bit 7	RBPU: PO	ORTB Pull-up	Enable bit	(see Section	n 2.2.2.2)						
bit 6	INTEDG : Interrupt Edge Select bit (see Section 2.2.2.2)										
bit 5	T0CS: TMR0 Clock Source Select bit										
	1 = Transition on T0CKI pin										
	0 = Intern	al instruction	cycle clock	(CLKOUT)							
bit 4	TOSE: TM	IR0 Source E	dge Select	bit							
	1 = Increr	nent on high-	to-low trans	ition on TOC	KI pin						
	0 = Increr	nent on low-t	o-high trans	ition on 10C	KI pin						
bit 3	PSA: Pre	scaler Assign	ment bit								
	1 = Presc 0 = Presc	aler is assign aler is assign	ied to the W ied to the Ti	DT mer0 modul	e						
bit 2-0	PS2:PS0:	Prescaler Ra	ate Select b	its							
	Bit Value	TMR0 Rate	WDT Rate								
	000	1:2	1:1								
	001	1:4	1:2								
	010	1:8	1:4								
	011	1:16	1:8								
	100	1:64	1:32								
	110	1 : 128	1:64								
	111	1 : 256	1 : 128								
	Logondi]			
	Legena.							(0)			
	R = Read	able bit	VV = V	Vritable bit	U = Unii	nplemented	bit, read as	.0,			
	- n = Valu	e at POR res	et '1' = E	Bit is set	'0' = Bit	is cleared	x = Bit is ι	unknown			
	Note:	To avoid ar	n unintende	d device F	RESET the	instruction	sequences	shown in			
		Example 5-1	and Examp	le 5-2 (page	45) must be	e executed w	hen changir	ng the pres-			
		caler assignr	nent betwe	en Timer0 a	and the WD	T. This sequ	ence must l	be followed			
	even if the WDT is disabled.										

NOTES:

6.4 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 6.4.1).

In Asynchronous Counter mode, Timer1 cannot be used as a time-base for capture or compare operations.

6.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. The example code provided in Example 6-1 and Example 6-2 demonstrates how to write to and read Timer1 while it is running in Asynchronous mode.

EXAMPLE 6-1: WRITING A 16-BIT FREE-RUNNING TIMER

; All	interrupts	are disabled	
CLRF	TMR1L	; Clear Low byte, Ensures no rollover into TMR1H	
MOVLW	HI_BYTE	; Value to load into TMR1H	
MOVWF	TMR1H, F	; Write High byte	
MOVLW	LO_BYTE	; Value to load into TMR1L	
MOVWF	TMR1H, F	; Write Low byte	
; Re-	enable the i	nterrupt (if required)	
CONTI	NUE	; Continue with your code	

EXAMPLE 6-2: READING A 16-BIT FREE-RUNNING TIMER

; All int	errupts a	re	disabled
MOVF TN	R1H, W	;	Read high byte
MOVWF TN	PH		
MOVF TN	R1L, W	;	Read low byte
MOVWF TN	PL		
MOVF TN	R1H, W	;	Read high byte
SUBWF TN	PH, W	;	Sub 1st read with 2nd read
BTFSC ST	ATUS,Z	;	Is result = 0
GOTO CO	NTINUE	;	Good 16-bit read
; TMR1L m	y have r	01	led over between the read of the high and low bytes.
; Reading	the high	a	nd low bytes now will read a good value.
MOVF TN	R1H, W	;	Read high byte
MOVWF TN	PH		
MOVF TN	R1L, W	;	Read low byte
MOVWF TN	PL	;	Re-enable the Interrupt (if required)
CONTINUE		;	Continue with your code

6.5 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for use with a 32 kHz crystal. Table 6-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must provide a software time delay to ensure proper oscillator start-up.

6.6 Resetting Timer1 using a CCP Trigger Output

If the CCP1 or CCP2 module is configured in Compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = '1011'), this signal will reset Timer1.

Note:	The special event triggers from the CCP1
	and CCP2 modules will not set interrupt
	flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either Timer or Synchronized Counter mode, to take advantage of this feature. If Timer1 is running in Asynchronous Counter mode, this RESET operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL register pair effectively becomes the period register for Timer1.

6.7 Resetting of Timer1 Register Pair (TMR1H, TMR1L)

TMR1H and TMR1L registers are not reset to 00h on a POR, or any other RESET, except by the CCP1 and CCP2 special event triggers.

TABLE 6-1:CAPACITOR SELECTION FOR
THE TIMER1 OSCILLATOR

	Frequency	Capacitors Used:					
Osc Type	Frequency	OSC1	OSC2				
LP	32 kHz	47 pF	47 pF				
	100 kHz	33 pF	33 pF				
	200 kHz	15 pF	15 pF				
			-				

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. These values were not optimized.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

Commonly Used Crystals:							
32.768 kHz	Epson C-001R32.768K-A						
100 kHz	Epson C-2 100.00 KC-P						
200 kHz	STD XTL 200.000 kHz						
Note 1: Hig of t sta 2: Sir cha res pria	wher capacitance increases the stability the oscillator, but also increases the rt-up time. Ince each resonator/crystal has its own aracteristics, the user should consult the conator/crystal manufacturer for appro- tate values of external components.						

T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other RESETS, the register is unaffected.

6.8 Timer1 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR		Value on all other RESETS	
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding re	gister for	the Most S	Significant I	Byte of the	16-bit TMR	1 Register		xxxx	xxxx	uuuu	uuuu
10h	T1CON	—	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu

TABLE 6-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F73/76; always maintain these bits clear.

8.5 PWM Mode (PWM)

In Pulse Width Modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force
	the CCP1 PWM output latch to the default
	low level. This is not the PORTC I/O data
	latch.

Figure 8-3 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see Section 8.5.3.

FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 8-4) has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).



8.5.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

 $PWM period = [(PR2) + 1] \cdot 4 \cdot Tosc \cdot (TMR2 prescale value)$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscaler (see Section 8.3) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

8.5.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

```
PWM duty cycle = (CCPR1L:CCP1CON<5:4>)•
TOSC • (TMR2 prescale value)
```

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the formula:

Resolution =
$$\frac{\log(\frac{FOSC}{FPWM})}{\log(2)}$$
 bits

Note: If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

10.1 USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In Asynchronous mode, bit BRGH (TXSTA<2>) also controls the baud rate. In Synchronous mode, bit BRGH is ignored. Table 10-1 shows the formula for computation of the baud rate for different USART modes which only apply in Master mode (internal clock).

Given the desired baud rate and FOSC, the nearest integer value for the SPBRG register can be calculated using the formula in Table 10-1. From this, the error in baud rate can be determined. It may be advantageous to use the high baud rate (BRGH = 1), even for slower baud clocks. This is because the FOSC/(16(X + 1)) equation can reduce the baud rate error in some cases.

Writing a new value to the SPBRG register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

10.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin.

TABLE 10-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate = Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	N/A

X = value in SPBRG (0 to 255)

TABLE 10-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	x00-000x
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

10.3 USART Synchronous Master Mode

In Synchronous Master mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition, enable bit SPEN (RCSTA<7>) is set in order to configure the RC6/TX/CK and RC7/RX/DT I/O pins to CK (clock) and DT (data) lines, respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

10.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 10-1. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer register TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCYCLE), the TXREG is empty and interrupt bit TXIF (PIR1<4>) is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. TRMT is a read only bit, which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory, so it is not available to the user.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 10-6). The transmission can also be started by first loading the TXREG register and then setting bit TXEN (Figure 10-7). This is advantageous when slow baud rates are selected, since the BRG is kept in RESET when bits TXEN, CREN and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally, when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR, resulting in an empty TXREG. Back-to-back transfers are possible.

Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to hiimpedance. If either bit CREN or bit SREN is set during a transmission, the transmission is aborted and the DT pin reverts to a hi-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic, however, is not reset, although it is disconnected from the pins. In order to reset the transmitter, the user has to clear bit TXEN. If bit SREN is set (to interrupt an on-going transmission and receive a single word), then after the single word is received, bit SREN will be cleared and the serial port will revert back to transmitting, since bit TXEN is still set. The DT line will immediately switch from Hiimpedance Receive mode to transmit and start driving. To avoid this, bit TXEN should be cleared.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR was empty and the TXREG was written before writing the "new" TX9D, the "present" value of bit TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 10.1).
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.
- 8. If using interrupts, ensure that GIE and PEIE in the INTCON register are set.

11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The 8-bit analog-to-digital (A/D) converter module has five inputs for the PIC16F73/76 and eight for the PIC16F74/77.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD), or the voltage level on the RA3/AN3/VREF pin.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the A/D conversion clock must be derived from the A/D's internal RC oscillator. The A/D module has three registers. These registers are:

- A/D Result Register ((ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 ((ADCON1)

The ADCON0 register, shown in Register 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference), or as digital I/O.

Additional information on using the A/D module can be found in the PICmicro[™] Mid-Range MCU Family Reference Manual (DS33023) and in Application Note, AN546 (DS00546).

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0			
	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON			
	bit 7			-				bit 0			
bit 7-6	ADCS1:ADCS0: A/D Conversion Clock Select bits										
	00 = Fosc	:/2									
	01 = FOSC	/8 \/20									
	10 = F030 11 = FRC (/o∠ Iclock derive	d from the ir	nternal A/D n	nodule RC c	oscillator)					
bit 5-3	CHS2:CH	SO: Analog C	Channel Sele	ect bits		,					
	000 = Ch a	annel 0 (RA0	/AN0)								
	001 = Cha	annel 1 (RA1	/AN1)								
	010 = Cha	annel 2 (RA2	./AN2)								
	011 = Cha	INNEL 3 (KAJ	/AN3) :/ana)								
	101 = Ch a	annel 5 (RE0	/AN5) ⁽¹⁾								
	110 = Cha	annel 6 (RE1	/AN6) ⁽¹⁾								
	111 = Cha	innel 7 (RE2	/AN7)(''								
bit 2	GO/DONE	: A/D Conve	rsion Status	; bit							
	$\frac{\text{If ADON} = 1}{1 - \sqrt{D}}$										
	1 = A/D conversion in progress (setting this bit starts the A/D conversion) 0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the										
	A/D conversion is complete)										
bit 1	Unimplem	nented: Read	d as '0'								
bit 0	ADON: A/I	D On bit									
	1 = A/D converter module is operating										
	0 = A/D co	0 = A/D converter module is shut-off and consumes no operating current									
	Note 1:	A/D channe	els 5, 6 and	7 are implem	nented on th	ie PIC16F74/7	7 only.				
	Legend:										
	R = Reada	able bit	W = V	Vritable bit	U = Unir	nplemented bit	t, read as '(0'			

'1' = Bit is set

'0' = Bit is cleared

REGISTER 11-1: ADCON0 REGISTER (ADDRESS 1Fh)

- n = Value at POR reset

x = Bit is unknown

The following steps should be followed for doing an $\ensuremath{\mathsf{A}}\xspace/\ensuremath{\mathsf{D}}\xspace$ conversion:

- 1. Configure the A/D module:
 - Configure analog pins, voltage reference, and digital I/O (ADCON1)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
- 2. Configure the A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set PEIE bit
 - Set GIE bit
- 3. Select an A/D input channel (ADCON0).

- 4. Wait for at least an appropriate acquisition period.
- 5. Start conversion:Set GO/DONE bit (ADCON0)
- 6. Wait for the A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared (interrupts disabled)

OR

- Waiting for the A/D interrupt
- 7. Read A/D result register (ADRES), and clear bit ADIF if required.
- 8. For next conversion, go to step 3 or step 4, as required.



FIGURE 11-1: A/D BLOCK DIAGRAM

11.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 11-2. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), see Figure 11-2. The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is 10 k Ω . After the analog input channel is selected (changed), the acquisition period must pass before the conversion can be started.

To calculate the minimum acquisition time, TACQ, see the PICmicroTM Mid-Range MCU Family Reference Manual (DS33023). In general, however, given a maximum source impedance of 10 k Ω and at a temperature of 100°C, TACQ will be no more than 16 µsec.



TABLE 11-1: TAD vs. MAXIMUM DEVICE OPERATING FREQUENCIES (STANDARD DEVICES (C))

AD Clo	Maximum Device Frequency		
Operation	ADCS1:ADCS0	Max.	
2Tosc	00	1.25 MHz	
8Tosc	01	5 MHz	
32Tosc	10	20 MHz	
RC ^(1, 2, 3)	11	(Note 1)	

Note 1: The RC source has a typical TAD time of 4 µs but can vary between 2-6 µs.

2: When the device frequencies are greater than 1 MHz, the RC A/D conversion clock source is only recommended for SLEEP operation.

3: For extended voltage devices (LC), please refer to the Electrical Specifications section.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/P-1	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
_	_	_					BOREN	_	CP0	PWRTEN	WDTEN	FOSC1	FOSC0
bit13													bit0
bit 13-7		Unimplemented: Read as '1'											
bit 6		BOREN	: Browr	n-out Re	set Enal	ble bit							
		1 = BO	R enable	ed									
		0 = BO	R disabl	ed									
bit 5		Unimpl	emente	d: Read	l as '1'								
bit 4		CP0: FI	LASH P	rogram l	Vemory	Code P	rotection b	oit					
		1 = Coo	de prote	ction off									
		0 = All ı	memory	location	s code	protecte	d						
bit 3		PWRTE	EN: Pow	er-up Ti	mer Ena	able bit							
		1 = PW	RT disa	bled									
		0 = PW	RT enat	bled									
bit 2		WDTEN	: Watch	ndog Tim	ner Enat	ole bit							
		1 = WD	T enabl	ed									
		0 = WD	I disabi	ed									
bit 1-0		FOSC1	:FOSCO	: Oscilla	tor Sele	ection bit	ts						
		11 = R(C oscilla	tor									
		$10 = H_{1}^{2}$	S OSCIIIA	tor									
		$01 = \mathbf{A}$	oscillat	or									
		00 – Li	ocomat										
		Nata	4. The				-1)	41	<i></i>				

REGISTER 12-1: CONFIGURATION WORD (ADDRESS 2007h)⁽¹⁾

Note 1: The erased (unprogrammed) value of the configuration word is 3FFFh.

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
- n = Value when device is un	programmed	u = Unchanged from programmed state

TABLE 12-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR (FOR DESIGN GUIDANCE ONLY)

Osc Type	Crystal	Typical Capacitor Values Tested:					
	печ	C1	C2				
LP	32 kHz	33 pF	33 pF				
	200 kHz	15 pF	15 pF				
XT	200 kHz	56 pF	56 pF				
	1 MHz	15 pF	15 pF				
	4 MHz	15 pF	15 pF				
HS	4 MHz	15 pF	15 pF				
	8 MHz	15 pF	15 pF				
	20 MHz	15 pF	15 pF				

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. These values were not optimized.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following this table for additional information.

Crystals Used:							
32 kHz	Epson C-001R32.768K-A						
200 kHz	STD XTL 200.000KHz						
1 MHz	ECS ECS-10-13-1						
4 MHz	ECS ECS-40-20-1						
8 MHz	EPSON CA-301 8.000M-C						
20 MHz	EPSON CA-301 20.000M-C						

- **Note 1:** Higher capacitance increases the stability of oscillator, but also increases the start-up time.
 - 2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - 3: Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.
 - **4:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

12.2.3 RC OSCILLATOR

For timing insensitive applications, the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 12-3 shows how the R/C combination is connected to the PIC16F7X.





14.0 DEVELOPMENT SUPPORT

The PICmicro[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD
- Device Programmers
 - PRO MATE[®] II Universal Device Programmer
- PICSTART[®] Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
 - PICDEM[™]1 Demonstration Board
 - PICDEM 2 Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - KEELOQ® Demonstration Board

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows[®]-based application that contains:

- · An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- · A full-featured editor
- · A project manager
- Customizable toolbar and key mapping
- · A status bar
- · On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the costeffective simulator to a full-featured emulator with minimal retraining.

14.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PICmicro MCU's.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

14.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

15.2 **DC Characteristics:** PIC16F73/74/76/77 (Industrial, Extended) PIC16LF73/74/76/77 (Industrial)

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions	
	VIL	Input Low Voltage						
		I/O ports:						
D030		with TTL buffer	Vss	—	0.15Vdd	V	For entire VDD range	
D030A			Vss	—	0.8V	V	$4.5V \le VDD \le 5.5V$	
D031		with Schmitt Trigger buffer	Vss	_	0.2Vdd	V		
D032		MCLR, OSC1 (in RC mode)	Vss	_	0.2Vdd	V	(Note 1)	
D033		OSC1 (in XT and LP mode)	Vss	_	0.3V	V		
		OSC1 (in HS mode)	Vss		0.3Vdd	V		
	Viн	Input High Voltage						
		I/O ports:						
D040		with TTL buffer	2.0	_	Vdd	V	$4.5V \le VDD \le 5.5V$	
D040A			0.25Vdd + 0.8V	—	Vdd	V	For entire VDD range	
D041		with Schmitt Trigger buffer	0.8Vdd	_	Vdd	V	For entire VDD range	
D042		MCLR	0.8Vdd	_	Vdd	V		
D042A		OSC1 (in XT and LP mode)	1.6V	_	Vdd	V		
		OSC1 (in HS mode)	0.7Vdd	—	Vdd	V		
D043		OSC1 (in RC mode)	0.9Vdd	_	Vdd	V	(Note 1)	
D070	Ipurb	PORTB Weak Pull-up Current	50	250	400	μΑ	VDD = 5V, VPIN = VSS	
	lı∟	Input Leakage Current (Notes 2	2, 3)					
D060		I/O ports	—	—	±1	μA	Vss ≤ VPIN ≤ VDD, pin at hi-impedance	
D061		MCLR, RA4/T0CKI	—	—	±5	μΑ	$Vss \le VPIN \le VDD$	
D063		OSC1	—		±5	μA	Vss \leq VPIN \leq VDD, XT, HS and LP osc configuration	

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance † only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.







FIGURE 15-14: SPI SLAVE MODE TIMING (CKE = 1)



FIGURE 16-3: TYPICAL IDD vs. Fosc OVER VDD (XT MODE)







FIGURE 16-13: TYPICAL, MINIMUM AND MAXIMUM WDT PERIOD vs. VDD (-40°C TO 125°C)





Package Marking Information (Cont'd)



44-Lead TQFP





Example

Ο

PIC16F77-I/P

0210017

44-Lead PLCC



Example





28-Lead Plastic Micro Leadframe Package (MF) 6x6 mm Body (MLF) (Continued)

	Units		INCHES		MILLIMETERS*			
Dim	MIN	NOM	MAX	MIN	NOM	MAX		
Pitch	р		.026 BSC		0.65 BSC			
Pad Width	В	.009	.011	.014	0.23	0.28	0.35	
Pad Length	L	.020	.024	.030	0.50	0.60	0.75	
Pad to Solder Mask	М	.005		.006	0.13		0.15	

*Controlling Parameter

Drawing No. C04-2114