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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f77t-i-l

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PIC16F7X





TABLE 1-3:PIC16F74 AND PIC16F77 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI	13	14	30		ST/CMOS(4)	Oscillator crystal or external clock input.
OSC1				I		Oscillator crystal input or external clock source input.
						ST buffer when configured in RC mode. Otherwise
CLKI				I		CMOS.
						function OSC1 (see OSC1/CLKL OSC2/CLKO pins)
OSC2/CLKO	14	15	31			Oscillator crystal or clock output.
OSC2				0		Oscillator crystal output.
						Connects to crystal or resonator in Crystal Oscillator
						mode.
CLKO				0		In RC mode, OSC2 pin outputs CLKO, which has 1/4
						the frequency of OSC1 and denotes the instruction
			40		07	
	1	2	18		51	Master Clear (Input) or programming voltage (output).
WIGER				1		RESET to the device
Vpp				Р		Programming voltage input.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19		TTL	
RA0		_	_	I/O		Digital I/O.
AN0				I		Analog input 0.
RA1/AN1	3	4	20		TTL	
RA1				I/O		Digital I/O.
AN1				I		Analog input 1.
RA2/AN2	4	5	21		TTL	
RA2				1/0		Digital I/O.
	_			1		Analog Input 2.
RA3/AN3/VREF	5	6	22	1/0	116	Digital I/O
AN3				1/0		Analog input 3
VREF				i		A/D reference voltage input.
RA4/T0CKI	6	7	23		ST	
RA4				I/O		Digital I/O – Open drain when configured as output.
TOCKI				I		Timer0 external clock input.
RA5/SS/AN4	7	8	24		TTL	
RA5				I/O		Digital I/O.
SS						SPI slave select input.
AN4						Analog input 4.
Legend: I = input		0 = 0	utput	1/0	D = input/outpu	It P = power

— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 2-1:	SPECIAL FUNCTION REGISTER SUMMARY	(CONTINUED)
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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 2											
100h ⁽⁴⁾	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
101h	TMR0	Timer0 Mo	odule Registe	er						xxxx xxxx	45, 96
102h ⁽⁴⁾	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
103h ⁽⁴⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
104h ⁽⁴⁾	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27, 96
105h	_	Unimplem	Inimplemented								_
106h	PORTB	PORTB D	ata Latch wh	ien written: P	ORTB pins w	hen read				xxxx xxxx	34, 96
107h	_	Unimplem	ented							—	_
108h	—	Unimplem	Jnimplemented								—
109h	_	Unimplem	ented							_	_
10Ah ^(1,4)	PCLATH	—	—	—	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	21, 96
10Bh ⁽⁴⁾	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
10Ch	PMDATA	Data Regi	Data Register Low Byte								
10Dh	PMADR	Address Register Low Byte								xxxx xxxx	29, 97
10Eh	PMDATH	— — Data Register High Byte							xxxx xxxx	29, 97	
10Fh	PMADRH	—	—	—	Address Reg	gister High By	/te			XXXX XXXX	29, 97
Bank 3											
180h ⁽⁴⁾	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
181h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	20, 44, 96
182h ⁽⁴⁾	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
183h ⁽⁴⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
184h ⁽⁴⁾	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27, 96
185h	—	Unimplem	ented							_	_
186h	TRISB	PORTB D	ata Direction	Register						1111 1111	34, 96
187h	_	Unimplem	ented							_	_
188h	_	Unimplem	ented							_	_
189h	_	Unimplem	ented							_	—
18Ah ^(1,4)	PCLATH	—	_	—	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	21, 96
18Bh ⁽⁴⁾	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
18Ch	PMCON1	(6)	—	—	—	—	—	—	RD	10	29, 97
18Dh	—	Unimplem	Unimplemented								
18Eh	—	Reserved	maintain clea	ar						0000 0000	
18Fh	_	Reserved	maintain clea	ar						0000 0000	

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

2: Other (non power-up) RESETS include external RESET through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: This bit always reads as a '1'.

4.2 PORTB and the TRISB Register

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= '1') will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISB bit (= '0') will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.





Four of the PORTB pins (RB7:RB4) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>). This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

This interrupt on mismatch feature, together with software configureable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression. Refer to the Embedded Control Handbook, "Implementing Wake-up on Key Stroke" (AN552).

RB0/INT is an external interrupt input pin and is configured using the INTEDG bit (OPTION_REG<6>).

RB0/INT is discussed in detail in Section 12.11.1.

FIGURE 4-4: BLOCK DIAGRAM OF RB7:RB4 PINS



4.3 PORTC and the TRISC Register

PORTC is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (= '1') will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISC bit (= '0') will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin).

PORTC is multiplexed with several peripheral functions (Table 4-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (BSF, BCF, XORWF) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings, and to Section 13.1 for additional information on read-modify-write operations.

FIGURE 4-5:

PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)



3: Peripheral OE (output enable) is only activated if peripheral select is active.

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or Data I/O (I ² C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output.
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchronous Data.

TABLE 4-5: PORTC FUNCTIONS

Legend: ST = Schmitt Trigger input

TABLE 4-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	PORTC	Data Dire	ection Re	egister					1111 1111	1111 1111

Legend: x = unknown, u = unchanged

FIGURE 9-1: SSP BLOCK DIAGRAM (SPI MODE)



To enable the serial port, SSP enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON register, and then set bit SSPEN. This configures the SDI, SDO, SCK, and SS pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set and ADCON must be configured such that RA5 is a digital I/O

Note 1: When the SPI is in Slave mode with SS pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the SS pin is set to VDD.

- 2: If the SPI is used in Slave mode with CKE = '1', then the SS pin control must be enabled.
- 3: When the SPI is in Slave mode with \overline{SS} pin control enabled (SSPCON<3:0> = '0100'), the state of the \overline{SS} pin can affect the state read back from the TRISC<5> bit. The Peripheral OE signal from the SSP module into PORTC controls the state that is read back from the TRISC<5> bit (see Section 4.3 for information on PORTC). If Read-Modify-Write instructions, such as BSF are performed on the TRISC register while the \overline{SS} pin is high, this will cause the TRISC<5> bit to be set, thus disabling the SDO output.

9.3 SSP I²C Operation

The SSP module in l^2C mode, fully implements all slave functions, except general call support, and provides interrupts on START and STOP bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer. These are the RC3/ SCK/SCL pin, which is the clock (SCL), and the RC4/ SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

The SSP module functions are enabled by setting SSP enable bit SSPEN (SSPCON<5>).

FIGURE 9-5: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for $\mathsf{I}^2\mathsf{C}$ operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I^2C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I^2C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with START and STOP bit interrupts enabled to support Firmware Master mode
- I²C Slave mode (10-bit address), with START and STOP bit interrupts enabled to support Firmware Master mode
- I²C START and STOP bit interrupts enabled to support Firmware Master mode, Slave is IDLE

Selection of any I^2C mode with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I^2C module.

Additional information on SSP I²C operation can be found in the PICmicro[™] Mid-Range MCU Family Reference Manual (DS33023A).

9.3.1 SLAVE MODE

In Slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge (\overline{ACK}) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this ACK pulse. They include (either or both):

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. Table 9-2 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I^2C specification, as well as the requirements of the SSP module, are shown in timing parameter #100 and parameter #101.

10.2 USART Asynchronous Mode

In this mode, the USART uses standard non-return-tozero (NRZ) format (one START bit, eight or nine data bits, and one STOP bit). The most common data format is 8-bits. An on-chip, dedicated, 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART transmits and receives the LSb first. The USART's transmitter and receiver are functionally independent, but use the same data format and baud rate. The baud rate generator produces a clock, either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- · Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

10.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 10-1. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREG. The TXREG register is loaded with data by firmware. The TSR register is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register, the TXREG register is empty. One instruction cycle later, flag bit TXIF (PIR1<4>) and flag bit TRMT (TXSTA<1>)

are set. The TXIF interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. Status bit TRMT is a read only bit, which is set one instruction cycle after the TSR register becomes empty, and is cleared one instruction cycle after the TSR register is loaded. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

Note 1:	The TSR register is not mapped in data
	memory, so it is not available to the user.
2.	Flag bit TXIE is set when enable bit TXEN

is set. TXIF is cleared by loading TXREG.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 10-2). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN. Normally, when transmission is first started, the TSR register is empty. At that point, transfer to the TXREG register will result in an immediate transfer to TSR, resulting in an empty TXREG. A back-to-back transfer is thus possible (Figure 10-3). Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. As a result, the RC6/TX/CK pin will revert to hi-impedance.

In order to select 9-bit transmission, transmit bit TX9 (TXSTA<6>) should be set and the ninth bit should be written to TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). In such a case, an incorrect ninth data bit may be loaded in the TSR register.



FIGURE 10-1: USART TRANSMIT BLOCK DIAGRAM

11.7 Use of the CCP Trigger

An A/D conversion can be started by the "special event trigger" of the CCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as 1011 and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D conversion, and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving the ADRES to the desired location). The appropriate analog input channel must be selected and an appropriate acquisition time should pass before the "special event trigger" sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the "special event trigger" will be ignored by the A/D module, but will still reset the Timer1 counter.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 1 Bit 0		Value on: POR, BOR		e on ther ETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
0Dh	PIR2	_	_	—	—		—		CCP2IF		0		0
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
8Dh	PIE2	—	—	—	—	—	—	_	CCP2IE		0		0
1Eh	ADRES	A/D Resu	ılt Registe	ər						xxxx	xxxx	uuuu	uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000	00-0	0000	00-0
9Fh	ADCON1	_	_	_	—	_	PCFG2	PCFG1	PCFG0		-000		-000
05h	PORTA	_		RA5	RA4	RA3	RA2	RA1	RA0	0x	0000	0u	0000
85h	TRISA	_		PORTA I	Data Directio	n Regist	er			11	1111	11	1111
09h	PORTE ⁽²⁾			_	_		RE2	RE1	RE0		-xxx		-uuu
89h	TRISE ⁽²⁾	IBF	OBF	IBOV	PSPMODE	_	PORTE Da	ta Directio	on Bits	0000	-111	0000	-111

TABLE 11-2: SUMMARY OF A/D REGISTERS

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F73/76; always maintain these bits clear.

2: These registers are reserved on the PIC16F73/76.

12.4 MCLR

PIC16F7X devices have a noise filter in the $\overline{\text{MCLR}}$ Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

The behavior of the ESD protection on the $\overline{\text{MCLR}}$ pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both $\overline{\text{MCLR}}$ Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the $\overline{\text{MCLR}}$ pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 12-5, is suggested.





12.5 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V - 1.7V). To take advantage of the POR, tie the MCLR pin to VDD as described in Section 12.4. A maximum rise time for VDD is specified. See the Electrical Specifications for details.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. For additional information, refer to Application Note, AN607, "Power-up Trouble Shooting" (DS00607).

12.6 Power-up Timer (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an accept-able level. A configuration bit is provided to enable/ disable the PWRT.

The power-up time delay will vary from chip to chip, due to VDD, temperature and process variation. See DC parameters for details (TPWRT, parameter #33).

12.7 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycles (from OSC1 input) delay after the PWRT delay is over (if enabled). This helps to ensure that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset, or wake-up from SLEEP.

12.8 Brown-out Reset (BOR)

The configuration bit, BODEN, can enable or disable the Brown-out Reset circuit. If VDD falls below VBOR (parameter D005, about 4V) for longer than TBOR (parameter #35, about 100 μ S), the brown-out situation will reset the device. If VDD falls below VBOR for less than TBOR, a RESET may not occur.

Once the brown-out occurs, the device will remain in Brown-out Reset until VDD rises above VBOR. The Power-up Timer then keeps the device in RESET for TPWRT (parameter #33, about 72 mS). If VDD should fall below VBOR during TPWRT, the Brown-out Reset process will restart when VDD rises above VBOR, with the Power-up Timer Reset. The Power-up Timer is always enabled when the Brown-out Reset circuit is enabled, regardless of the state of the PWRT configuration bit.

12.9 Time-out Sequence

On power-up, the time-out sequence is as follows: the PWRT delay starts (if enabled) when a POR Reset occurs. Then, OST starts counting 1024 oscillator cycles when PWRT ends (LP, XT, HS). When the OST ends, the device comes out of RESET.

If MCLR is kept low long enough, all delays will expire. Bringing MCLR high will begin execution immediately. This is useful for testing purposes or to synchronize more than one PIC16F7X device operating in parallel.

Table 12-5 shows the RESET conditions for the STATUS, PCON and PC registers, while Table 12-6 shows the RESET conditions for all the registers.

NOTES:

FIGURE 15-9: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



TABLE 15-5: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param No.	Symbol	(Characteristic		Min	Тур†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2	No Prescaler		0.5Tcy + 20	—	—	ns	
		input low time		Standard(F)	10	_	_	ns	
		With Prescaler	Extended(LF)	20	_	_	ns		
51*	ТссН	CCP1 and CCP2	No Prescaler		0.5Tcy + 20	_	_	ns	
	input high time		Standard(F)	10			ns		
		With Prescaler	Extended(LF)	20			ns		
52*	TccP	CCP1 and CCP2 in	CP1 and CCP2 input period					ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 and CCP2 c	utput rise time	Standard(F)	—	10	25	ns	
				Extended(LF)	—	25	50	ns	
54*	TccF	CCP1 and CCP2 c	output fall time	Standard(F)	—	10	25	ns	
				Extended(LF)	—	25	45	ns	
*	These	narameters are cha	racterized but no	nt tested					

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.







FIGURE 15-14: SPI SLAVE MODE TIMING (CKE = 1)

TABLE 15-12: A/D CONVERTER CHARACTERISTICS: PIC16F7X (INDUSTRIAL, EXTENDED) PIC16LF7X (INDUSTRIAL)

Param No.	Sym	Charact	eristic	Min	Тур†	Мах	Units	Conditions
A01	NR	Resolution	PIC16F7X		_	8 bits	bit	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$
			PIC16LF7X		_	8 bits	bit	VREF = VDD = 2.2V
A02	Eabs	Total absolute e	rror	—	—	< ±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A03	EIL	Integral linearity	error	—	_	< ±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A04	Edl	Differential linea	rity error	—	-	< ±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A05	Efs	Full scale error		—	_	< ±1	LSb	VREF = VDD = 5.12V, $VSS \le VAIN \le VREF$
A06	Eoff	Offset error		—	—	< ±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A10	—	Monotonicity (No	ote 3)	—	guaranteed	—	_	$VSS \leq VAIN \leq VREF$
A20	Vref	Reference volta	ge	2.5 2.2		5.5 5.5	V V	-40°C to +125°C 0°C to +125°C
A25	VAIN	Analog input vol	tage	Vss - 0.3	_	Vref + 0.3	V	
A30	ZAIN	Recommended analog voltage s	impedance of source	—	—	10.0	kΩ	
A40	IAD	A/D conversion	PIC16F7X	—	180	—	μΑ	Average current
		current (VDD)	PIC16LF7X	—	90	—	μA consumption whe is on (Note 1) .	consumption when A/D is on (Note 1) .
A50	IREF	VREF input curre	ent (Note 2)	N/A 	_	±5 500	μΑ μΑ	During VAIN acquisition. During A/D Conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from the RA3 pin or the VDD pin, whichever is selected as a reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.









PIC16F7X



FIGURE 16-15: TYPICAL, MINIMUM AND MAXIMUM VOH vs. IOH (VDD = 5V, -40°C TO 125°C)







FIGURE 16-19: MINIMUM AND MAXIMUM VIN vs. VDD, (TTL INPUT, -40°C TO 125°C)





40-Lead Plastic Dual In-line (P) - 600 mil (PDIP)



Units		INCHES*		N	IILLIMETERS	6
1 Limits	MIN	NOM	MAX	MIN	NOM	MAX
n		40			40	
р		.100			2.54	
А	.160	.175	.190	4.06	4.45	4.83
A2	.140	.150	.160	3.56	3.81	4.06
A1	.015			0.38		
Е	.595	.600	.625	15.11	15.24	15.88
E1	.530	.545	.560	13.46	13.84	14.22
D	2.045	2.058	2.065	51.94	52.26	52.45
L	.120	.130	.135	3.05	3.30	3.43
С	.008	.012	.015	0.20	0.29	0.38
B1	.030	.050	.070	0.76	1.27	1.78
В	.014	.018	.022	0.36	0.46	0.56
eВ	.620	.650	.680	15.75	16.51	17.27
α	5	10	15	5	10	15
β	5	10	15	5	10	15
	Units n P A A2 A1 E D L C B1 B eB α β	Units MIN n P A .160 A2 .140 A1 .015 E .595 E1 .530 D 2.045 L .120 c .008 B1 .030 B .014 eB .620 α .5 β .5	Units INCHES* nLimits MIN NOM n 40 P .100 A .160 .175 A2 .140 .150 A1 .015	$\begin{tabular}{ c c c c } \hline Units & INCHES* \\ \hline Limits & MIN & NOM & MAX \\ \hline n & 40 \\ \hline P & 100 \\ \hline A & 160 & 175 \\ \hline A & 160 & 160 \\ \hline B & 100 & 160 \\ \hline B & 100 & 160 \\ \hline B & 100 & 150 \\ \hline B & 5 & 100 & 150 \\ \hline B & 5 & 100 & 150 \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c } \hline Vnits & VNCHES* & NN \\ \hline \mbox{n Limits} & MIN & NOM & MAX & MIN \\ \hline \mbox{n } & 40 & & & & & & & & & & & & & & & & & $	$\begin{tabular}{ c c c c c } \hline \mathbf{V} \mathbf{NCHES}^* \mathbf{MIN} \mathbf{NOM} \mathbf{MAX} \mathbf{MIN} \mathbf{NOM} \mathbf{NOnd} \mathbf{NOM} $$

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-011

Drawing No. C04-016

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RC7/RX/DT Pin	9,	11

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