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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf74-i-pt

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PIC16F73 AND PIC16F76 PINOUT DESCRIPTION **TABLE 1-2:**

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	l/O/P Type	Buffer Type	Description
OSC1/CLKI OSC1	9	6	I	ST/CMOS ⁽³⁾	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST
CLKI			I		buffer when configured in RC mode. Otherwise CMOS. External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO OSC2	10	7	0	-	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator
CLKO			0		mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP MCLR	1	26	I	ST	Master Clear (input) or programming voltage (output). Master Clear (Reset) input. This pin is an active low RESET to the device.
Vpp			Р		Programming voltage input.
					PORTA is a bi-directional I/O port.
RA0/AN0	2	27		TTL	
			1/0		Digital I/O. Analog input 0
	з	28	1	тті	
RA1	5	20	I/O		Digital I/O.
AN1			1		Analog input 1.
RA2/AN2	4	1		TTL	
RA2			I/O		Digital I/O.
AN2			I		Analog input 2.
RA3/AN3/VREF	5	2		TTL	
RA3			I/O		Digital I/O.
AN3			I		Analog input 3.
VREF			I		A/D reference voltage input.
RA4/T0CKI	6	4		ST	
RA4			1/0		Digital I/O – Open drain when configured as output.
	_	_	I		limero external clock input.
RA5/SS/AN4	(5	1/0	IIL	Disting 1/O
			1/0		SPI slove select input
AN4					Analog input 4
Legend: L= inpu	l I	$\Omega = 0.01$	iout	I/O = inpu	P = power

— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

This buffer is a Schmitt Trigger input when used in Serial Programming mode.
 This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

2.2.2.1 STATUS Register

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC, or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable, therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as $000u \ u1uu$ (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, or DC bits from the STATUS register. For other instructions not affecting any status bits, see the "Instruction Set Summary."

Note 1: The <u>C</u> and <u>DC</u> bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the <u>SUBLW</u> and <u>SUBWF</u> instructions for examples.

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
	IRP	RP1	RP0	TO	PD	Z	DC	С
	bit 7							bit 0
bit 7	IRP: Regis 1 = Bank 2 0 = Bank 0	ster Bank Sele 2, 3 (100h - 1F 0, 1 (00h - FFt	ect bit (used f Fh) n)	or indirect ac	ldressing)			
bit 6-5	RP1:RP0 : Register Bank Select bits (used for direct addressing) 11 = Bank 3 (180h - 1FFh) 10 = Bank 2 (100h - 17Fh) 01 = Bank 1 (80h - FFh) 00 = Bank 0 (00h - 7Fh) Each bank is 128 bytes							
bit 4	TO: Time-out bit 1 = After power-up, CLRWDT instruction, or SLEEP instruction 0 = A WDT time-out occurred							
bit 3	PD : Power-down bit 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction							
bit 2	 z: Zero bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero 							
bit 1	 DC: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) 1 = A carry-out from the 4th low order bit of the result occurred 0 = No carry-out from the 4th low order bit of the result 							
bit 0	C : Carry/b 1 = A carry 0 = No car	orrow bit (ADE y-out from the ry-out from th	WF, ADDLW Most Signific e Most Signif	cant bit of the ficant bit of the	SUBWF instru e result occu ne result occ	uctions) irred curred	ad by addin	a the two's
	Legend:	complement loaded with e	of the secon	d operand. F h or low orde	For rotate (R r bit of the s	RF, RLF)	instructions	s, this bit is

- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
Legend:			

3.0 **READING PROGRAM MEMORY**

The FLASH Program Memory is readable during normal operation over the entire VDD range. It is indirectly addressed through Special Function Registers (SFR). Up to 14-bit numbers can be stored in memory for use as calibration parameters, serial numbers, packed 7-bit ASCII, etc. Executing a program memory location containing data that forms an invalid instruction results in a NOP.

There are five SFRs used to read the program and memory. These registers are:

- PMCON1
- PMDATA
- PMDATH
- PMADR
- PMADRH

The program memory allows word reads. Program memory access allows for checksum calculation and reading calibration tables.

When interfacing to the program memory block, the PMDATH:PMDATA registers form a two-byte word, which holds the 14-bit data for reads. The PMADRH:PMADR registers form a two-byte word, which holds the 13-bit address of the FLASH location being accessed. These devices can have up to 8K words of program FLASH, with an address range from Oh to 3FFFh. The unused upper bits in both the PMDATH and PMADRH registers are not implemented and read as "0's".

3.1 **PMADR**

The address registers can address up to a maximum of 8K words of program FLASH.

When selecting a program address value, the MSByte of the address is written to the PMADRH register and the LSByte is written to the PMADR register. The upper MSbits of PMADRH must always be clear.

3.2 PMCON1 Register

PMCON1 is the control register for memory accesses.

The control bit RD initiates read operations. This bit cannot be cleared, only set, in software. It is cleared in hardware at the completion of the read operation.

REGISTER 3-1: PMCON1 REGISTER (ADDRESS 18Ch)

	R-1	U-0	U-0	U-0	U-x	U-0	U-0	R/S-0
	reserved		_	_			_	RD
	bit 7							bit 0
bit 7	Reserved:	Read as '1'						
bit 6-1	Unimplemented: Read as '0'							
bit 0	RD: Read Control bit							
	1 = Initiates a FLASH read, RD is cleared in hardware. The RD bit can only be set (not cleared) in software.							
	0 = FLASH	I read comp	leted					
	Legend:							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PICmicro[™] Mid-Range Reference Manual, (DS33023).

4.1 PORTA and the TRISA Register

PORTA is a 6-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= '1') will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= '0') will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other PORTA pins have TTL input levels and full CMOS output drivers.

Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

Note: On a Power-on Reset, these pins are configured as analog inputs and read as '0'.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set, when using them as analog inputs.

BCF	STATUS,	RP0	;	
BCF	STATUS,	RP1	;	Bank0
CLRF	PORTA		;	Initialize PORTA by
			;	clearing output
			;	data latches
BSF	STATUS,	RP0	;	Select Bank 1
MOVLW	0x06		;	Configure all pins
MOVWF	ADCON1		;	as digital inputs
MOVLW	0xCF		;	Value used to
			;	initialize data
			;	direction
MOVWF	TRISA		;	Set RA<3:0> as inputs
			;	RA<5:4> as outputs
			;	TRISA<7:6>are always
			;	read as '0'.

FIGURE 4-1:

BLOCK DIAGRAM OF RA3:RA0 AND RA5 PINS



FIGURE 4-2:

BLOCK DIAGRAM OF RA4/T0CKI PIN



6.5 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for use with a 32 kHz crystal. Table 6-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must provide a software time delay to ensure proper oscillator start-up.

6.6 Resetting Timer1 using a CCP Trigger Output

If the CCP1 or CCP2 module is configured in Compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = '1011'), this signal will reset Timer1.

Note:	The special event triggers from the CCP1
	and CCP2 modules will not set interrupt
	flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either Timer or Synchronized Counter mode, to take advantage of this feature. If Timer1 is running in Asynchronous Counter mode, this RESET operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL register pair effectively becomes the period register for Timer1.

6.7 Resetting of Timer1 Register Pair (TMR1H, TMR1L)

TMR1H and TMR1L registers are not reset to 00h on a POR, or any other RESET, except by the CCP1 and CCP2 special event triggers.

TABLE 6-1:CAPACITOR SELECTION FOR
THE TIMER1 OSCILLATOR

	Frequency	Capacitors Used:			
Osc Type	Frequency	OSC1	OSC2		
LP	32 kHz	47 pF	47 pF		
	100 kHz	33 pF	33 pF		
	200 kHz	15 pF	15 pF		
			-		

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. These values were not optimized.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

Commonly Used Crystals:						
32.768 kHz Epson C-001R32.768K-A						
100 kHz	100 kHz Epson C-2 100.00 KC-P					
200 kHz	STD XTL 200.000 kHz					
Note 1: Hig of t sta 2: Sir cha res pria	wher capacitance increases the stability the oscillator, but also increases the rt-up time. The each resonator/crystal has its own aracteristics, the user should consult the conator/crystal manufacturer for appro- tate values of external components.					

T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other RESETS, the register is unaffected.

6.8 Timer1 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value PC BC	e on:)R,)R	Valu all o RES	e on other ETS
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
0Eh	TMR1L	Holding re	Holding register for the Least Significant Byte of the 16-bit TMR1 Register					r	xxxx	xxxx	uuuu	uuuu	
0Fh	TMR1H	Holding re	gister for	the Most S	Significant I	Byte of the	16-bit TMR	1 Register		xxxx	xxxx	uuuu	uuuu
10h	T1CON	—	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu

TABLE 6-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F73/76; always maintain these bits clear.

REGISTER 7-1:	T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)									
	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0		
	bit 7							bit 0		
bit 7	Unimple	mented: Rea	ad as '0'							
bit 6-3	bit 6-3 TOUTPS3:TOUTPS0: Timer2 Output Postscale Select bits									
	0000 = 1	:1 Postscale								
	0001 = 1	:2 Postscale								
	0010 = 1:3 Postscale									
	•									
	1111 = 1	:16 Postscal	e							
bit 2	TMR2ON	I: Timer2 On	bit							
	1 = Time	r2 is on								
	0 = Time	r2 is off								
bit 1-0	T2CKPS	1:T2CKPS0:	Timer2 Cloc	k Prescale S	elect bits					
	00 = Pres	scaler is 1								
	01 = Pres	scaler is 4								
	1x = Pres	scaler is 16								
	Legend:									
	R = Reada	able bit	W = W	/ritable bit	U = Unim	plemented l	oit, read as '	0'		

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

- n = Value at POR reset

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value PC BC	e on: DR, DR	Valu all c RES	e on other ETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
11h	TMR2	Timer2 M	Timer2 Module Register						0000	0000	0000	0000	
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000	0000	-000	0000
92h	PR2	Timer2 Pe	eriod Regis	ter						1111	1111	1111	1111

'1' = Bit is set

'0' = Bit is cleared

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F73/76; always maintain these bits clear.

x = Bit is unknown

REGISTER 9-2:	EGISTER 9-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h))	
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	
	bit 7							bit 0	
bit 7	WCOL: W	rite Collisior	n Detect bit						
	1 = The SS (must I 0 = No col	 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software) 0 = No collision 							
bit 6	SSPOV: R	eceive Ove	rflow Indicate	or bit					
	In SPI mod	de:							
 1 = A new byte is received while the SSPBUF register is still holding the previous data of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The must read the SSPBUF, even if only transmitting data, to avoid setting overflow. I Master mode, the overflow bit is not set since each new reception (and transmiss initiated by writing to the SSPBUF register. 0 = No overflow 							ta. In case The user 7. In ssion) is		
	In I ² C mod	<u>de:</u>							
	 1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPO is a "don't care" in Transmit mode. SSPOV must be cleared in software in either mod 0 = No overflow 						SSPOV er mode.		
bit 5	SSPEN: S	ynchronous	Serial Port	Enable bit					
	In SPI mode: 1 = Enables serial port and configures SCK, SDO, and SDI as serial port pins 0 = Disables serial port and configures these pins as I/O port pins In I ² C mode:								
	 1 = Enables the serial port and configures the SDA and SCL pins as serial port pins 0 = Disables serial port and configures these pins as I/O port pins 								
	In both mo	des, when e	enabled, thes	se pins must b	e properly o	configured a	is input or o	utput.	
bit 4	CKP: Cloc	k Polaritv S	elect bit		,	0	•	•	
	In SPI mode: 1 = IDLE state for clock is a high level (Microwire [®] default) 0 = IDLE state for clock is a low level (Microwire [®] alternate)								
	$\frac{\ln I^2 C \mod}{SCK \text{ releases}}$	<u>te:</u> se control e clock							
	0 = Holds	clock low (c	lock stretch).	(Used to ensu	ure data set	up time.)			
bit 3-0	SSPM3:SS	SPM0: Sync	hronous Ser	ial Port Mode	Select bits				
	$\begin{array}{l} 0000 = SPI \text{ Master mode, clock} = Fosc/4 \\ 0001 = SPI \text{ Master mode, clock} = Fosc/16 \\ 0010 = SPI \text{ Master mode, clock} = Fosc/64 \\ 0011 = SPI \text{ Master mode, clock} = TMR2 \text{ output/2} \\ 0100 = SPI \text{ Slave mode, clock} = SCK pin. SS pin control enabled. \\ 0101 = SPI \text{ Slave mode, clock} = SCK pin. SS pin control disabled. SS can be used as I/O pin. \\ 0110 = I^2C \text{ Slave mode, 7-bit address} \\ 0111 = I^2C \text{ Slave mode, 10-bit address} \\ 1011 = I^2C \text{ Slave mode, 7-bit address with START and STOP bit interrupts enabled} \\ \end{array}$								
	Legend:		107 10		11 11	nlomentad	hit rocd	·0'	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
 n = Value at POR reset 	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 9-1: SSP BLOCK DIAGRAM (SPI MODE)



To enable the serial port, SSP enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON register, and then set bit SSPEN. This configures the SDI, SDO, SCK, and SS pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set and ADCON must be configured such that RA5 is a digital I/O

Note 1: When the SPI is in Slave mode with SS pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the SS pin is set to VDD.

- 2: If the SPI is used in Slave mode with CKE = '1', then the SS pin control must be enabled.
- 3: When the SPI is in Slave mode with \overline{SS} pin control enabled (SSPCON<3:0> = '0100'), the state of the \overline{SS} pin can affect the state read back from the TRISC<5> bit. The Peripheral OE signal from the SSP module into PORTC controls the state that is read back from the TRISC<5> bit (see Section 4.3 for information on PORTC). If Read-Modify-Write instructions, such as BSF are performed on the TRISC register while the \overline{SS} pin is high, this will cause the TRISC<5> bit to be set, thus disabling the SDO output.

9.3 SSP I²C Operation

The SSP module in l^2C mode, fully implements all slave functions, except general call support, and provides interrupts on START and STOP bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer. These are the RC3/ SCK/SCL pin, which is the clock (SCL), and the RC4/ SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

The SSP module functions are enabled by setting SSP enable bit SSPEN (SSPCON<5>).

FIGURE 9-5: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for $\mathsf{I}^2\mathsf{C}$ operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I^2C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I^2C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with START and STOP bit interrupts enabled to support Firmware Master mode
- I²C Slave mode (10-bit address), with START and STOP bit interrupts enabled to support Firmware Master mode
- I²C START and STOP bit interrupts enabled to support Firmware Master mode, Slave is IDLE

Selection of any I^2C mode with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I^2C module.

Additional information on SSP I²C operation can be found in the PICmicro[™] Mid-Range MCU Family Reference Manual (DS33023A).

9.3.1 SLAVE MODE

In Slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge (\overline{ACK}) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this ACK pulse. They include (either or both):

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. Table 9-2 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I^2C specification, as well as the requirements of the SSP module, are shown in timing parameter #100 and parameter #101.

9.3.1.1 Addressing

Once the SSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- a) The SSPSR register value is loaded into the SSPBUF register.
- b) The buffer full bit, BF is set.
- c) An ACK pulse is generated.
- d) SSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on the falling edge of the ninth SCL pulse.

In 10-bit Address mode, two address bytes need to be received by the slave (Figure 9-7). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address.

The sequence of events for 10-bit address is as follows, with steps 7 - 9 for slave-transmitter:

- 1. Receive first (high) byte of address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
- Update the SSPADD register with second (low) byte of address (clears bit UA and releases the SCL line).
- 3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 4. Receive second (low) byte of address (bits SSPIF, BF, and UA are set).
- 5. Update the SSPADD register with the first (high) byte of address, if match releases SCL line, this will clear bit UA.
- 6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 7. Receive Repeated START condition.
- 8. Receive first (high) byte of address (bits SSPIF and BF are set).
- 9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

Status Bits as DataTransfer is ReceivedBFSSPOV		$SSPSR \to SSPBUF$	Generate ACK	Set bit SSPIF (SSP Interrupt occurs
			r uise	if enabled)
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

TABLE 9-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Note: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

9.3.1.2 Reception

When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set, or bit SSPOV (SSPCON<6>) is set. This is an error condition due to the user's firmware. An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

10.1 USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In Asynchronous mode, bit BRGH (TXSTA<2>) also controls the baud rate. In Synchronous mode, bit BRGH is ignored. Table 10-1 shows the formula for computation of the baud rate for different USART modes which only apply in Master mode (internal clock).

Given the desired baud rate and FOSC, the nearest integer value for the SPBRG register can be calculated using the formula in Table 10-1. From this, the error in baud rate can be determined. It may be advantageous to use the high baud rate (BRGH = 1), even for slower baud clocks. This is because the FOSC/(16(X + 1)) equation can reduce the baud rate error in some cases.

Writing a new value to the SPBRG register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

10.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin.

TABLE 10-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = FOSC/(64(X+1))	Baud Rate = Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	N/A

X = value in SPBRG (0 to 255)

TABLE 10-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	x00-000x
99h	SPBRG	Baud Ra	ate Gene	erator Re	gister					0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

13.2 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[<i>label</i>] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	$(W) + k \to (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[label] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) \rightarrow (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[<i>label</i>] BCF f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	$0 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[<i>label</i>] BSF f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	$1 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

ANDLW	AND Literal with W			
Syntax:	[label] ANDLW k			
Operands:	$0 \le k \le 255$			
Operation:	(W) .AND. (k) \rightarrow (W)			
Status Affected:	Z			
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.			

BTFSS	Bit Test f, Skip if Set
Syntax:	[label] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if (f) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruc- tion is discarded and a NOP is executed instead, making this a 2TCY instruction.

ANDWF	AND W with f				
Syntax:	[label] ANDWF f,d				
Operands:	$0 \le f \le 127$ $d \in [0,1]$				
Operation:	(W) .AND. (f) \rightarrow (destination)				
Status Affected:	Z				
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.				

BTFSC	Bit Test, Skip if Clear
Syntax:	[label] BTFSC f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	skip if (f) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2TCY instruction.

PIC16F7X

SWAPF	Swap Nibbles in f					
Syntax:	[label] SWAPF f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$					
Operation:	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$					
Status Affected:	None					
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in register 'f'.					

XORWF	Exclusive OR W with f						
Syntax:	[label] XORWF f,d						
Operands:	$0 \le f \le 127$ $d \in [0,1]$						
Operation:	(W) .XOR. (f) \rightarrow (destination)						
Status Affected:	Z						
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.						

XORLW	Exclusive OR Literal with W						
Syntax:	[<i>label</i>] XORLW k						
Operands:	$0 \le k \le 255$						
Operation:	(W) .XOR. $k \rightarrow (W)$						
Status Affected:	Z						
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.						

PIC16F7X





FIGURE 15-2: PIC16LF7X VOLTAGE-FREQUENCY GRAPH



15.2 DC Characteristics: PIC16F73/74/76/77 (Industrial, Extended) PIC16LF73/74/76/77 (Industrial) (Continued)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le Ta \le +85^{\circ}C$ for industrial $-40^{\circ}C \le Ta \le +125^{\circ}C$ for extendedOperating voltage VDD range as described in DC Specification, Section 15.1.								
Param No.	Sym	Characteristic Min Typ† Max Units Conditions								
	Vol	Output Low Voltage								
D080		I/O ports	—	_	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +125°C			
D083		OSC2/CLKOUT (RC osc config)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +125°C			
			—	—	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C			
	Vон	Output High Voltage				•				
D090		I/O ports (Note 3)	Vdd - 0.7	—	_	V	IOH = -3.0 mA, VDD = 4.5V, -40°С to +125°С			
D092		OSC2/CLKOUT (RC osc config)	Vdd - 0.7	—	—	V	ІОН = -1.3 mA, VDD = 4.5V, -40°С to +125°С			
			Vdd - 0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, -40°С to +125°С			
D150*	Vod	Open Drain High Voltage			12	V	RA4 pin			
		Capacitive Loading Specs on C	Output Pir	IS						
D100	Cosc2	OSC2 pin	—		15	pF	In XT, HS and LP modes when external clock is used to drive OSC1			
D101	Сю	All I/O pins and OSC2 (in RC mode)	—	—	50	pF				
D102	Св	SCL, SDA in I ² C mode	—	—	400	pF				
		Program FLASH Memory								
D130	Ер	Endurance	100	1000	—	E/W	25°C at 5V			
D131	Vpr	VDD for Read	2.0	_	5.5	V				

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.





TABLE 15-6: PARALLEL SLAVE PORT REQUIREMENTS (PIC16F74/77 DEVICES ONLY)

Parameter No.	Symbol	Characteristic			Тур†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before WR↑ or CS´	`(setup time)	20 25	_		ns ns	Extended range only
63*	TwrH2dtl	WR↑ or CS↑ to data in invalid (hold time)	Standard(F)	20 35	_		ns ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data out valid				80 90	ns ns	Extended range only
65	TrdH2dtl	\overline{RD} for \overline{CS} to data out invalid		10		30	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 16-5: TYPICAL IDD vs. Fosc OVER VDD (LP MODE)





28-Lead Plastic Micro Leadframe Package (MF) 6x6 mm Body (MLF)



	Units	INCHES		М			
Dimension L	imits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.026 BSC		0.65 BSC		
Overall Height	А		.033	.039		0.85	1.00
Molded Package Thickness	A2		.026	.031		0.65	0.80
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3		.008 REF.		0.20 REF.		
Overall Width	Е		.236 BSC		6.00 BSC		
Molded Package Width	E1		.226 BSC		5.75 BSC		
Exposed Pad Width	E2	.140	.146	.152	3.55	3.70	3.85
Overall Length	D		.236 BSC		6.00 BSC		
Molded Package Length	D1		.226 BSC			5.75 BSC	
Exposed Pad Length	D2	.140	.146	.152	3.55	3.70	3.85
Lead Width	В	.009	.011	.014	0.23	0.28	0.35
Lead Length	L	.020	.024	.030	0.50	0.60	0.75
Tie Bar Width	R	.005	.007	.010	0.13	0.17	0.23
Tie Bar Length	Q	.012	.016	.026	0.30	0.40	0.65
Chamfer	СН	.009	.017	.024	0.24	0.42	0.60
Mold Draft Angle Top	α			12°			12°

A3

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC equivalent: pending

Drawing No. C04-114



28-Lead Plastic Micro Leadframe Package (MF) 6x6 mm Body (MLF) (Continued)

	Units	INCHES			MILLIMETERS*		
Dim	ension Limits	MIN	NOM	MAX	MIN	NOM	MAX
Pitch	р		.026 BSC			0.65 BSC	
Pad Width	В	.009	.011	.014	0.23	0.28	0.35
Pad Length	L	.020	.024	.030	0.50	0.60	0.75
Pad to Solder Mask	М	.005		.006	0.13		0.15

*Controlling Parameter

Drawing No. C04-2114

APPENDIX C: CONVERSION CONSIDERATIONS

Considerations for converting from previous versions of devices to the ones listed in this data sheet are listed in Table C-1.

TABLE C-1: CONVERSION CONSIDERATIONS

Characteristic	PIC16C7X	PIC16F87X	PIC16F7X
Pins	28/40	28/40	28/40
Timers	3	3	3
Interrupts	11 or 12	13 or 14	11 or 12
Communication	PSP, USART, SSP (SPI, I ² C Slave)	PSP, USART, SSP (SPI, I ² C Master/Slave)	PSP, USART, SSP (SPI, I ² C Slave)
Frequency	20 MHz	20 MHz	20 MHz
A/D	8-bit	10-bit	8-bit
ССР	2	2	2
Program Memory	4K, 8K EPROM	4K, 8K FLASH (1,000 E/W cycles)	4K, 8K FLASH (100 E/W cycles typical)
RAM	192, 368 bytes	192, 368 bytes	192, 368 bytes
EEPROM Data	None	128, 256 bytes	None
Other	_	In-Circuit Debugger, Low Voltage Programming	_