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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
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TABLE 2-1:	SPECIAL FUNCTION REGISTER SUMMARY	(CONTINUED)
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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 2											
100h ⁽⁴⁾	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
101h	TMR0	Timer0 Mo	odule Registe	er						xxxx xxxx	45, 96
102h ⁽⁴⁾	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
103h ⁽⁴⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
104h ⁽⁴⁾	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27, 96
105h	_	Unimplem	ented							_	_
106h	PORTB	PORTB D	ata Latch wh	ien written: P	ORTB pins w	hen read				xxxx xxxx	34, 96
107h	_	Unimplem	ented							—	_
108h	_	Unimplem	mented							—	—
109h	_	Unimplem	ented							_	_
10Ah ^(1,4)	PCLATH	—	—	—	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	21, 96
10Bh ⁽⁴⁾	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
10Ch	PMDATA	Data Regi	ta Register Low Byte								29, 97
10Dh	PMADR	Address R	ddress Register Low Byte							xxxx xxxx	29, 97
10Eh	PMDATH	—	— — Data Register High Byte							xxxx xxxx	29, 97
10Fh	PMADRH	—	—	—	Address Reg	gister High By	/te			XXXX XXXX	29, 97
Bank 3											
180h ⁽⁴⁾	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
181h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	20, 44, 96
182h ⁽⁴⁾	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
183h ⁽⁴⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
184h ⁽⁴⁾	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27, 96
185h	—	Unimplem	ented							_	_
186h	TRISB	PORTB D	ata Direction	Register						1111 1111	34, 96
187h	_	Unimplem	ented							_	_
188h	_	Unimplem	ented							_	_
189h	_	Unimplem	ented							_	—
18Ah ^(1,4)	PCLATH	—	_	—	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	21, 96
18Bh ⁽⁴⁾	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
18Ch	PMCON1	(6)	—	—	—	—	—	—	RD	10	29, 97
18Dh	—	Unimplem	implemented								
18Eh	—	Reserved	maintain clea	ar						0000 0000	
18Fh	_	Reserved	maintain clea	ar						0000 0000	

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

2: Other (non power-up) RESETS include external RESET through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: This bit always reads as a '1'.

6.0 TIMER1 MODULE

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L), which are readable and writable. The TMR1 Register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow, which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit TMR1IE (PIE1<0>).

Timer1 can operate in one of two modes:

- As a timer
- · As a counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Timer1 also has an internal "RESET input". This RESET can be generated by either of the two CCP modules as the special event trigger (see Sections 8.1 and 8.2). Register 6-1 shows the Timer1 Control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI/CCP2 and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored and these pins read as '0'.

Additional information on timer modules is available in the PICmicro[™] Mid-Range MCU Family Reference Manual (DS33023).

REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	_	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N
	bit 7							bit 0
bit 7-6	Unimplem	nented: Rea	ad as '0'					
bit 5-4	T1CKPS1	:T1CKPS0:	Timer1 Inpu	ut Clock Pres	scale Select I	bits		
	11 = 1:8 P	rescale valu	he					
	10 = 1:4 P	rescale valu	Je					
	01 = 1:2 P 00 = 1:1 P	rescale vali rescale vali	re Te					
bit 3	T10SCEN	I: Timer1 Os	scillator Ena	ble Control k	oit			
	1 = Oscilla	ator is enabl	ed					
	0 = Oscilla	ator is shut-o	off (the oscill	ator inverter	is turned off	to eliminate	power draii	ר)
bit 2	T1SYNC:	Timer1 Exte	ernal Clock I	nput Synchr	onization Co	ntrol bit		
	TMR1CS :	<u>= 1:</u>						
	1 = Do not	t synchroniz	e external c	lock input				
	0 = Synch	ronize exter	nal clock inp	out				
	TMR1CS :	<u>= 0:</u>			I I 			
1 ** 4		ignorea. Tin	neri uses th		JCK when TW	$ \mathbf{R} ^{1}\mathbf{CS}=0.$		
Dit 1	IMR1CS:	Timer1 Clo	ck Source S	elect bit				
	1 = Extern 0 = Interna	al clock from	m pin RC0/T sc/4)	1050/110	(I (on the risi	ng edge)		
bit 0	TMR10N:	Timer1 On	bit					
	1 = Enable	es Timer1						
	0 = Stops	Timer1						
	Legend:							
	R = Reada	able bit	W = V	Nritable bit	U = Unin	nplemented	bit, read as	'0'
	- n = Value	e at POR re	set '1' = l	Bit is set	'0' = Bit i	s cleared	x = Bit is ι	Inknown

9.3.1.1 Addressing

Once the SSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- a) The SSPSR register value is loaded into the SSPBUF register.
- b) The buffer full bit, BF is set.
- c) An ACK pulse is generated.
- d) SSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on the falling edge of the ninth SCL pulse.

In 10-bit Address mode, two address bytes need to be received by the slave (Figure 9-7). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address.

The sequence of events for 10-bit address is as follows, with steps 7 - 9 for slave-transmitter:

- 1. Receive first (high) byte of address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
- Update the SSPADD register with second (low) byte of address (clears bit UA and releases the SCL line).
- 3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 4. Receive second (low) byte of address (bits SSPIF, BF, and UA are set).
- 5. Update the SSPADD register with the first (high) byte of address, if match releases SCL line, this will clear bit UA.
- 6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 7. Receive Repeated START condition.
- 8. Receive first (high) byte of address (bits SSPIF and BF are set).
- 9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

Status Bits as Data Transfer is Received		$SSPSR \to SSPBUF$	Generate ACK	Set bit SSPIF (SSP Interrupt occurs			
BF	SSPOV		r uise	if enabled)			
0	0	Yes	Yes	Yes			
1	0	No	No	Yes			
1	1	No	No	Yes			
0	1	No	No	Yes			

TABLE 9-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Note: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

9.3.1.2 Reception

When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set, or bit SSPOV (SSPCON<6>) is set. This is an error condition due to the user's firmware. An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

9.3.2 MASTER MODE

Master mode of operation is supported in firmware using interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a RESET or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I²C bus may be taken when the P bit is set, or the bus is IDLE and both the S and P bits are clear.

In Master mode, the SCL and SDA lines are manipulated by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I²C module.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt will occur if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the Slave mode IDLE (SSPM3:SSPM0 = 1011), or with the Slave active. When both Master and Slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

9.3.3 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the START and STOP conditions, allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a RESET or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I^2C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is IDLE and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In Multi-Master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to retransfer the data at a later time.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS					
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u					
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000					
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000					
13h	SSPBUF	Synchrono	us Serial	Port Rece	eive Buff	er/Transr	nit Registe	er		xxxx xxxx	uuuu uuuu					
93h	SSPADD	Synchrono	us Serial	Port (I ² C	mode) A	ddress R	egister			0000 0000	0000 0000					
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000					
94h	SSPSTAT	SMP ⁽²⁾	CKE ⁽²⁾	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000					
87h	TRISC	PORTC Da	ata Direct	ion Regist	ter	•	ORTC Data Direction Register									

 TABLE 9-3:
 REGISTERS ASSOCIATED WITH I²C OPERATION

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by SSP module in I²C mode. **Note 1:** PSPIF and PSPIE are reserved on the PIC16F73/76; always maintain these bits clear.

2: Maintain these bits clear in I²C mode.

10.1 USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In Asynchronous mode, bit BRGH (TXSTA<2>) also controls the baud rate. In Synchronous mode, bit BRGH is ignored. Table 10-1 shows the formula for computation of the baud rate for different USART modes which only apply in Master mode (internal clock).

Given the desired baud rate and FOSC, the nearest integer value for the SPBRG register can be calculated using the formula in Table 10-1. From this, the error in baud rate can be determined. It may be advantageous to use the high baud rate (BRGH = 1), even for slower baud clocks. This is because the FOSC/(16(X + 1)) equation can reduce the baud rate error in some cases.

Writing a new value to the SPBRG register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

10.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin.

TABLE 10-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = FOSC/(64(X+1))	Baud Rate = Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	N/A

X = value in SPBRG (0 to 255)

TABLE 10-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	x00-000x
99h	SPBRG	Baud Ra	3aud Rate Generator Register							0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

		Fosc = 20 M	lHz		Fosc = 16 M	IHz		Fosc = 10 M	lHz
BAUD RATE	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)
1200	1,221	1.73%	255	1,202	0.16%	207	1,202	0.16%	129
2400	2,404	0.16%	129	2,404	0.16%	103	2,404	0.16%	64
9600	9,470	-1.36%	32	9,615	0.16%	25	9,766	1.73%	15
19,200	19,531	1.73%	15	19,231	0.16%	12	19,531	1.73%	7
38,400	39,063	1.73%	7	35,714	-6.99%	6	39,063	1.73%	3
57,600	62,500	8.51%	4	62,500	8.51%	3	52,083	-9.58%	2
76,800	78,125	1.73%	3	83,333	8.51%	2	78,125	1.73%	1
96,000	104,167	8.51%	2	83,333	-13.19%	2	78,125	-18.62%	1
115,200	104,167	-9.58%	2	125,000	8.51%	1	78,125	-32.18%	1
250,000	312,500	25.00%	0	250,000	0.00%	0	156,250	-37.50%	0

TABLE 10-3:BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

		Fosc = 4 MI	Hz		Fosc = 3.6864	MHz	Fosc = 3.579545 MHz			
BAUD RATE	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	
300	300	0.16%	207	300	0.00%	191	301	0.23%	185	
1200	1,202	0.16%	51	1,200	0.00%	47	1,190	-0.83%	46	
2400	2,404	0.16%	25	2,400	0.00%	23	2,432	1.32%	22	
9600	8,929	-6.99%	6	9,600	0.00%	5	9,322	-2.90%	5	
19,200	20,833	8.51%	2	19,200	0.00%	2	18,643	-2.90%	2	
38,400	31,250	-18.62%	1	28,800	-25.00%	1	27,965	-27.17%	1	
57,600	62,500	8.51%	0	57,600	0.00%	0	55,930	-2.90%	0	
76,800	62,500	-18.62%	0	—	_	_	—	—	—	

TABLE 10-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

		Fosc = 20 M	Hz		Fosc = 16 M	Hz		Fosc = 10 MI	Hz
BAUD RATE	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)
2400	_	—	_	—	—	_	2,441	1.73%	255
9600	9,615	0.16%	129	9,615	0.16%	103	9,615	0.16%	64
19,200	19,231	0.16%	64	19,231	0.16%	51	18,939	-1.36%	32
38,400	37,879	-1.36%	32	38,462	0.16%	25	39,063	1.73%	15
57,600	56,818	-1.36%	21	58,824	2.12%	16	56,818	-1.36%	10
76,800	78,125	1.73%	15	76,923	0.16%	12	78,125	1.73%	7
96,000	96,154	0.16%	12	100,000	4.17%	9	89,286	-6.99%	6
115,200	113,636	-1.36%	10	111,111	-3.55%	8	125,000	8.51%	4
250,000	250,000	0.00%	4	250,000	0.00%	3	208,333	-16.67%	2
300,000	312,500	4.17%	3	333,333	11.11%	2	312,500	4.17%	1

BAUD		Fosc = 4 MH	Iz	F	osc = 3.6864	MHz	Fosc = 3.579545 MHz			
RATE (K)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	BAUD	% ERROR	SPBRG VALUE (DECIMAL)	
1200	1,202	0.16%	207	1,200	0.00%	191	1,203	0.23%	185	
2400	2,404	0.16%	103	2,400	0.00%	95	2,406	0.23%	92	
9600	9,615	0.16%	25	9,600	0.00%	23	9,727	1.32%	22	
19,200	19,231	0.16%	12	19,200	0.00%	11	18,643	-2.90%	11	
38,400	35,714	-6.99%	6	38,400	0.00%	5	37,287	-2.90%	5	
57,600	62,500	8.51%	3	57,600	0.00%	3	55,930	-2.90%	3	
76,800	83,333	8.51%	2	76,800	0.00%	2	74,574	-2.90%	2	
96,000	83,333	-13.19%	2	115,200	20.00%	1	111,861	16.52%	1	
115,200	125,000	8.51%	1	115,200	0.00%	1	111,861	-2.90%	1	
250,000	250,000	0.00%	0	230,400	-7.84%	0	223,722	-10.51%	0	

10.2 USART Asynchronous Mode

In this mode, the USART uses standard non-return-tozero (NRZ) format (one START bit, eight or nine data bits, and one STOP bit). The most common data format is 8-bits. An on-chip, dedicated, 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART transmits and receives the LSb first. The USART's transmitter and receiver are functionally independent, but use the same data format and baud rate. The baud rate generator produces a clock, either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- · Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

10.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 10-1. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREG. The TXREG register is loaded with data by firmware. The TSR register is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register, the TXREG register is empty. One instruction cycle later, flag bit TXIF (PIR1<4>) and flag bit TRMT (TXSTA<1>)

are set. The TXIF interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. Status bit TRMT is a read only bit, which is set one instruction cycle after the TSR register becomes empty, and is cleared one instruction cycle after the TSR register is loaded. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

Note 1:	The TSR register is not mapped in data
	memory, so it is not available to the user.
2.	Flag bit TXIE is set when enable bit TXEN

is set. TXIF is cleared by loading TXREG.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 10-2). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN. Normally, when transmission is first started, the TSR register is empty. At that point, transfer to the TXREG register will result in an immediate transfer to TSR, resulting in an empty TXREG. A back-to-back transfer is thus possible (Figure 10-3). Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. As a result, the RC6/TX/CK pin will revert to hi-impedance.

In order to select 9-bit transmission, transmit bit TX9 (TXSTA<6>) should be set and the ninth bit should be written to TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). In such a case, an incorrect ninth data bit may be loaded in the TSR register.



FIGURE 10-1: USART TRANSMIT BLOCK DIAGRAM

12.13 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/ CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

The WDT can be permanently disabled by clearing configuration bit, WDTE (Section 12.1).

WDT time-out period values may be found in the Electrical Specifications section under parameter #31. Values for the WDT prescaler (actually a postscaler, but shared with the Timer0 prescaler) may be assigned using the OPTION_REG register.

- Note 1: The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.
 - 2: When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.



FIGURE 12-11: WATCHDOG TIMER BLOCK DIAGRAM

TABLE 12-7: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN ⁽¹⁾		CP0	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0
81h,181h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 12-1 for operation of these bits.

TABLE 13-2: PIC16F7X INSTRUCTION SET

Mnemonic, Operands		Description	Cycles		14-Bit	Opcode	Status	Notes	
		Description		MSb			LSb		Affected
		BYTE-ORIENTED FILE REGIS	TER OPE	RATIC	ONS				
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
		BIT-ORIENTED FILE REGIST		RATIO	NS				
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
		LITERAL AND CONTROL	OPERAT	IONS					
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C.DC.Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Ζ	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO.PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk	- ,	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk	_	
RETFIE	-	Return from interrupt	2	0.0	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	0.0	0000	0110	0011	TO.PD	
SUBLW	k	Subtract W from literal	1	11	110×	kkkk	kkkk	C.DC.Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z,20,2	
Note 1	When on I	O register is modified as a function of itself (e.g.		ם ייים	1) tho ye		ad will b	o that value	procont

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Note: Additional information on the mid-range instruction set is available in the PICmicro[™] Mid-Range MCU Family Reference Manual (DS33023).

13.2 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[<i>label</i>] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	$(W) + k \to (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[label] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) \rightarrow (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[<i>label</i>] BCF f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	$0 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[<i>label</i>] BSF f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	$1 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

ANDLW	AND Literal with W
Syntax:	[label] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) \rightarrow (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

BTFSS	Bit Test f, Skip if Set
Syntax:	[label] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if (f) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruc- tion is discarded and a NOP is executed instead, making this a 2TCY instruction.

ANDWF	AND W with f
Syntax:	[label] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) \rightarrow (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BTFSC	Bit Test, Skip if Clear
Syntax:	[label] BTFSC f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	skip if (f) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2TCY instruction.

RLF	Rotate Left f through Carry
Syntax:	[<i>label</i>] RLF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$
Operation:	See description below
Status Affected:	С
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.

SLEEP

Syntax:	[label] SLEEP
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow WDT, \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO}, \\ 0 \rightarrow \overline{PD} \end{array}$
Status Affected:	TO, PD
Description:	The power-down status bit, \overline{PD} is cleared. Time-out status bit, \overline{TO} is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped.

RETURN	Return from Subroutine						
Syntax:	[label] RETURN						
Operands:	None						
Operation:	$TOS\toPC$						
Status Affected:	None						
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.						

RRF	Rotate Right f through Carry					
Syntax:	[<i>label</i>] RRF f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$					
Operation:	See description below					
Status Affected:	С					
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'					
	C Register f					

SUBLW	Subtract W from Literal							
Syntax:	[<i>label</i>] SUBLW k							
Operands:	$0 \le k \le 255$							
Operation:	$k \text{ - (W)} \to (W)$							
Status Affected:	C, DC, Z							
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.							

SUBWF	Subtract W from f						
Syntax:	[<i>label</i>] SUBWF f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$						
Operation:	(f) - (W) \rightarrow (destination)						
Status Affected:	C, DC, Z						
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.						

PIC16F7X





FIGURE 15-2: PIC16LF7X VOLTAGE-FREQUENCY GRAPH



15.2 **DC Characteristics:** PIC16F73/74/76/77 (Industrial, Extended) PIC16LF73/74/76/77 (Industrial)

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$								
Param No.	Sym	Characteristic	ristic Min Typ† Max Units Conditions								
	VIL	nput Low Voltage									
		I/O ports:									
D030		with TTL buffer	Vss	—	0.15Vdd	V	For entire VDD range				
D030A			Vss	—	0.8V	V	$4.5V \le VDD \le 5.5V$				
D031		with Schmitt Trigger buffer	Vss	—	0.2Vdd	V					
D032		MCLR, OSC1 (in RC mode)	Vss	_	0.2Vdd	V	(Note 1)				
D033		OSC1 (in XT and LP mode)	Vss	—	0.3V	V					
		OSC1 (in HS mode)	Vss	—	0.3Vdd	V					
	Viн	Input High Voltage									
		I/O ports:									
D040		with TTL buffer	2.0	—	Vdd	V	$4.5V \le VDD \le 5.5V$				
D040A			0.25Vdd + 0.8V	—	Vdd	V	For entire VDD range				
D041		with Schmitt Trigger buffer	0.8Vdd	—	Vdd	V	For entire VDD range				
D042		MCLR	0.8Vdd	—	Vdd	V					
D042A		OSC1 (in XT and LP mode)	1.6V	—	Vdd	V					
		OSC1 (in HS mode)	0.7Vdd	_	Vdd	V					
D043		OSC1 (in RC mode)	0.9Vdd	—	Vdd	V	(Note 1)				
D070	Ipurb	PORTB Weak Pull-up Current	50	250	400	μA	VDD = 5V, VPIN = VSS				
	lı∟	Input Leakage Current (Notes 2	2, 3)								
D060		I/O ports	—	—	±1	μA	Vss ≤ VPIN ≤ VDD, pin at hi-impedance				
D061		MCLR, RA4/T0CKI	—	—	±5	μΑ	$Vss \le VPIN \le VDD$				
D063		OSC1			±5	μA	Vss \leq VPIN \leq VDD, XT, HS and LP osc configuration				

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance † only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.



FIGURE 15-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

FIGURE 15-7: BROWN-OUT RESET TIMING



TABLE 15-3:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER,
AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	_		μs	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	_	1024 Tosc	_	_	Tosc = OSC1 period
33*	TPWRT	Power-up Timer Period	28	72	132	ms	$VDD = 5V, -40^{\circ}C \text{ to } +85^{\circ}C$
34	Tioz	I/O Hi-Impedance from MCLR Low or Watchdog Timer Reset	_	_	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	_		μs	$VDD \leq VBOR (D005)$
* Th	no poromi	store are abaractorized but not tooted					

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-9: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



TABLE 15-5: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param No.	Symbol	(Characteristic					Units	Conditions
50*	TccL	CCP1 and CCP2	No Prescaler		0.5Tcy + 20	—	—	ns	
		input low time		Standard(F)	10	_	_	ns	
			With Prescaler	Extended(LF)	20	_	_	ns	
51*	ТссН	CCP1 and CCP2	No Prescaler		0.5Tcy + 20	_	_	ns	
		input high time		Standard(F)	10			ns	
			With Prescaler	Extended(LF)	20			ns	
52*	TccP	CCP1 and CCP2 in	CP1 and CCP2 input period					ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 and CCP2 c	utput rise time	Standard(F)	—	10	25	ns	
				Extended(LF)	—	25	50	ns	
54*	TccF	CCP1 and CCP2 c	P1 and CCP2 output fall time		—	10	25	ns	
				Extended(LF)	—	25	45	ns	
*	These	narameters are cha	racterized but no	nt tested					

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.





TABLE 15-6: PARALLEL SLAVE PORT REQUIREMENTS (PIC16F74/77 DEVICES ONLY)

Parameter No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
62	TdtV2wrH	Data in valid before WR↑ or CS´	`(setup time)	20 25	_		ns ns	Extended range only
63*	TwrH2dtl	WR↑ or CS↑ to data in invalid (hold time)	Standard(F)	20 35	_		ns ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data out valid				80 90	ns ns	Extended range only
65	TrdH2dtl	\overline{RD} for \overline{CS} to data out invalid		10		30	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.









17.2 **Package Details**

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-line (SP) – 300 mil (PDIP)



	Units		INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.100			2.54		
Top to Seating Plane	А	.140	.150	.160	3.56	3.81	4.06	
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43	
Base to Seating Plane	A1	.015			0.38			
Shoulder to Shoulder Width	Е	.300	.310	.325	7.62	7.87	8.26	
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49	
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18	
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43	
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38	
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65	
Lower Lead Width	В	.016	.019	.022	0.41	0.48	0.56	
Overall Row Spacing §	eB	.320	.350	.430	8.13	8.89	10.92	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

* Controlling Parameter

§ Significant Characteristic

Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MO-095

Drawing No. C04-070

Notes:

28-Lead Plastic Micro Leadframe Package (MF) 6x6 mm Body (MLF)



	Units		INCHES		MILLIMETERS*			
Dimension L	imits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.026 BSC			0.65 BSC		
Overall Height	А		.033	.039		0.85	1.00	
Molded Package Thickness	A2		.026	.031		0.65	0.80	
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05	
Base Thickness	A3		.008 REF.		0.20 REF.			
Overall Width	Е		.236 BSC		6.00 BSC			
Molded Package Width	E1		.226 BSC		5.75 BSC			
Exposed Pad Width	E2	.140	.146	.152	3.55	3.70	3.85	
Overall Length	D		.236 BSC			6.00 BSC		
Molded Package Length	D1		.226 BSC		5.75 BSC			
Exposed Pad Length	D2	.140	.146	.152	3.55	3.70	3.85	
Lead Width	В	.009	.011	.014	0.23	0.28	0.35	
Lead Length	L	.020	.024	.030	0.50	0.60	0.75	
Tie Bar Width	R	.005	.007	.010	0.13	0.17	0.23	
Tie Bar Length	Q	.012	.016	.026	0.30	0.40	0.65	
Chamfer	СН	.009	.017	.024	0.24	0.42	0.60	
Mold Draft Angle Top	α			12°			12°	

A3

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC equivalent: pending

Drawing No. C04-114

44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)



		INCHES		MILLIMETERS*			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	р		.031			0.80	
Pins per Side	n1		11			11	
Overall Height	Α	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039		1.00		
Foot Angle	¢	0	3.5	7	0	3.5	7
Overall Width	Е	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	С	.004	.006	.008	0.09	0.15	0.20
Lead Width	В	.012	.015	.017	0.30	0.38	0.44
Pin 1 Corner Chamfer	СН	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-026 Drawing No. C04-076