



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf77t-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# **Table of Contents**

1.0	Device Overview	5
2.0	Memory Organization	3
3.0	Reading Program Memory	9
4.0	I/O Ports	1
5.0	Timer0 Module	3
6.0	Timer1 Module	7
7.0	Timer2 Module	1
8.0	Capture/Compare/PWM Modules	3
9.0	Synchronous Serial Port (SSP) Module	9
10.0	Universal Synchronous Asynchronous Receiver Transmitter (USART)	9
11.0	Analog-to-Digital Converter (A/D) Module	3
12.0	Special Features of the CPU	9
13.0	Instruction Set Summary 109	5
14.0	Development Support	3
15.0	Electrical Characteristics	9
16.0	DC and AC Characteristics Graphs and Tables	1
17.0	Packaging Information 15	1
Apper	ndix A: Revision History	1
Apper	ndix B: Device Differences	1
Apper	ndix C: Conversion Considerations	2
Index		3
On-Li	ne Support	9
Reade	er Response 170	C
PIC16	F7X Product Identification System	1

# TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@mail.microchip.com** or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

# Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

## Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)
- The Microchip Corporate Literature Center; U.S. FAX: (480) 792-7277

When contacting a sales office or the literature center, please specify which device, revision of silicon and data sheet (include literature number) you are using.

# **Customer Notification System**

Register on our web site at www.microchip.com/cn to receive the most current information on all of our products.

#### 1.0 **DEVICE OVERVIEW**

This document contains device specific information about the following devices:

- PIC16F73
- PIC16F74
- PIC16F76
- PIC16F77

PIC16F73/76 devices are available only in 28-pin packages, while PIC16F74/77 devices are available in 40-pin and 44-pin packages. All devices in the PIC16F7X family share common architecture, with the following differences:

- The PIC16F73 and PIC16F76 have one-half of the total on-chip memory of the PIC16F74 and **PIC16F77**
- The 28-pin devices have 3 I/O ports, while the 40/44-pin devices have 5
- · The 28-pin devices have 11 interrupts, while the 40/44-pin devices have 12
- The 28-pin devices have 5 A/D input channels, while the 40/44-pin devices have 8
- The Parallel Slave Port is implemented only on the 40/44-pin devices

PIC16F7X DEVICE FEATURES **PIC16F74 PIC16F76 Key Features PIC16F73 PIC16F77 Operating Frequency** DC - 20 MHz DC - 20 MHz DC - 20 MHz DC - 20 MHz **RESETS** (and Delays) POR, BOR POR. BOR POR. BOR POR, BOR (PWRT, OST) (PWRT, OST) (PWRT, OST) (PWRT, OST) FLASH Program Memory 4K 4K 8K 8K (14-bit words) Data Memory (bytes) 368 192 192 368 Interrupts 11 12 11 12 I/O Ports Ports A,B,C Ports A,B,C Ports A,B,C,D,E Ports A,B,C,D,E Timers 3 3 3 3 Capture/Compare/PWM Modules 2 2 2 2 SSP, USART Serial Communications SSP, USART SSP. USART SSP, USART Parallel Communications PSP PSP 8-bit Analog-to-Digital Module **5 Input Channels** 8 Input Channels 5 Input Channels 8 Input Channels Instruction Set **35 Instructions 35 Instructions** 35 Instructions **35 Instructions** Packaging 28-pin DIP 40-pin PDIP 28-pin DIP 40-pin PDIP 28-pin SOIC 44-pin PLCC 28-pin SOIC 44-pin PLCC 28-pin SSOP 44-pin TQFP 28-pin SSOP 44-pin TQFP 28-pin MLF 28-pin MLF

## **TABLE 1-1:**

The available features are summarized in Table 1-1. Block diagrams of the PIC16F73/76 and PIC16F74/77 devices are provided in Figure 1-1 and Figure 1-2, respectively. The pinouts for these device families are listed in Table 1-2 and Table 1-3.

Additional information may be found in the PICmicro™ Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

TABLE 2-1:	SPECIAL FUNCTION REGISTER SUMMARY	(CONTINUED)
------------	-----------------------------------	-------------

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 2											
100h <sup>(4)</sup>	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
101h	TMR0	Timer0 Mo	odule Registe	er						xxxx xxxx	45, 96
102h <sup>(4)</sup>	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
103h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
104h <sup>(4)</sup>	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27, 96
105h	_	Unimplem	ented							_	_
106h	PORTB	PORTB D	ata Latch wh	ien written: P	ORTB pins w	hen read				xxxx xxxx	34, 96
107h	_	Unimplem	nimplemented								_
108h	_	Unimplem	ented							—	—
109h	_	Unimplem	ented							_	_
10Ah <sup>(1,4)</sup>	PCLATH	—	—	—	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	21, 96
10Bh <sup>(4)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
10Ch	PMDATA	Data Regi	Data Register Low Byte								29, 97
10Dh	PMADR	Address R	Address Register Low Byte								29, 97
10Eh	PMDATH	— — Data Register High Byte							xxxx xxxx	29, 97	
10Fh	PMADRH	—	—	—	Address Reg	gister High By	/te			XXXX XXXX	29, 97
Bank 3											
180h <sup>(4)</sup>	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
181h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	20, 44, 96
182h <sup>(4)</sup>	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
183h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
184h <sup>(4)</sup>	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27, 96
185h	—	Unimplem	ented							_	_
186h	TRISB	PORTB D	ata Direction	Register						1111 1111	34, 96
187h	_	Unimplem	ented							_	_
188h	_	Unimplem	ented							_	_
189h	_	Unimplem	ented							_	—
18Ah <sup>(1,4)</sup>	PCLATH	—	_	—	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	21, 96
18Bh <b><sup>(4)</sup></b>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
18Ch	PMCON1	(6)	—	—	—	—	—	—	RD	10	29, 97
18Dh	—	Unimplem	ented							_	
18Eh	—	Reserved	maintain clea	ar						0000 0000	
18Fh	_	Reserved	maintain clea	ar						0000 0000	

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

**Note** 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

2: Other (non power-up) RESETS include external RESET through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: This bit always reads as a '1'.

#### 2.2.2.1 STATUS Register

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC, or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable, therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as  $000u \ u1uu$  (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, or DC bits from the STATUS register. For other instructions not affecting any status bits, see the "Instruction Set Summary."

Note 1: The <u>C</u> and <u>DC</u> bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the <u>SUBLW</u> and <u>SUBWF</u> instructions for examples.

## REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x				
	IRP	RP1	RP0	TO	PD	Z	DC	С				
	bit 7							bit 0				
bit 7	<b>IRP:</b> Regis 1 = Bank 2 0 = Bank 0	ster Bank Sele 2, 3 (100h - 1F 0, 1 (00h - FFt	ect bit (used f Fh) n)	or indirect ac	ldressing)							
bit 6-5	<b>RP1:RP0</b> : 11 = Bank 10 = Bank 01 = Bank 00 = Bank Each bank	Register Banl 3 (180h - 1FF 2 (100h - 17F 1 (80h - FFh) 0 (00h - 7Fh) s is 128 bytes	k Select bits ⁻h) ⁻h)	(used for dire	ect addressi	ng)						
bit 4	<b>TO</b> : Time-0 1 = After p 0 = A WD	O: Time-out bit         = After power-up, CLRWDT instruction, or SLEEP instruction         = A WDT time-out occurred										
bit 3	<b>PD</b> : Power 1 = After p 0 = By exe	PD: Power-down bit 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction										
bit 2	z: Zero bit 1 = The re 0 = The re	sult of an arith sult of an arith	nmetic or logi nmetic or logi	c operation is	s zero s not zero							
bit 1	<b>DC</b> : Digit o 1 = A carry 0 = No car	carry/borrow b y-out from the ry-out from th	it (ADDWF, AD 4th low orde e 4th low ord	DLW,SUBL r bit of the re ler bit of the r	w,SUBWF( sult occurre esult	instructions d	3)					
bit 0	<b>C</b> : Carry/b 1 = A carry 0 = No car	<ul> <li>D = No carry-out from the 4th low order bit of the result</li> <li>C: Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)</li> <li>1 = A carry-out from the Most Significant bit of the result occurred</li> <li>0 = No carry-out from the Most Significant bit of the result occurred</li> </ul>										
	Legend:	complement loaded with e	of the secon	d operand. F h or low orde	For rotate (R r bit of the s	RF, RLF)	instructions	s, this bit is				

- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
Legend:			

## 3.3 Reading the FLASH Program Memory

A program memory location may be read by writing two bytes of the address to the PMADR and PMADRH registers and then setting control bit RD (PMCON1<0>). Once the read control bit is set, the microcontroller will use the next two instruction cycles to read the data. The data is available in the PMDATA and PMDATH registers after the second NOP instruction. Therefore, it can be read as two bytes in the following instructions. The PMDATA and PMDATH registers will hold this value until the next read operation.

# 3.4 Operation During Code Protect

FLASH program memory has its own code protect mechanism. External Read and Write operations by programmers are disabled if this mechanism is enabled.

The microcontroller can read and execute instructions out of the internal FLASH program memory, regardless of the state of the code protect configuration bits.

	BSF	STATUS, RP1	;
	BCF	STATUS, RP0	; Bank 2
	MOVF	ADDRH, W	;
	MOVWF	PMADRH	; MSByte of Program Address to read
	MOVF	ADDRL, W	;
	MOVWF	PMADR	; LSByte of Program Address to read
	BSF	STATUS, RP0	; Bank 3 Required
Required Sequence	BSF NOP NOP	PMCON1, RD	; EEPROM Read Sequence ; memory is read in the next two cycles after BSF PMCON1,RD ;
	BCF	STATUS, RPO	; Bank 2
	MOVF	PMDATA, W	; W = LSByte of Program PMDATA
	MOVF	PMDATH, W	; W = MSByte of Program PMDATA

#### EXAMPLE 3-1: FLASH PROGRAM READ

## TABLE 3-1: REGISTERS ASSOCIATED WITH PROGRAM FLASH

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
10Dh	PMADR	Address I	ddress Register Low Byte							xxxx xxxx	uuuu uuuu
10Fh	PMADRH	_	_	—	Address Register High Byte						uuuu uuuu
10Ch	PMDATA	Data Reg	ata Register Low Byte							xxxx xxxx	uuuu uuuu
10Eh	PMDATH	_	_	Data Reg	ata Register High Byte					xxxx xxxx	uuuu uuuu
18Ch	PMCON1	(1)		_	_			_	RD	10	10

Legend: x = unknown, u = unchanged, r = reserved, - = unimplemented read as '0'. Shaded cells are not used during FLASH access. **Note 1:** This bit always reads as a '1'.

## 4.5 PORTE and TRISE Register

This section is not applicable to the PIC16F73 or PIC16F76.

PORTE has three pins, RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7, which are individually configureable as inputs or outputs. These pins have Schmitt Trigger input buffers.

I/O PORTE becomes control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). Ensure ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

Register 4-1 shows the TRISE register, which also controls the parallel slave port operation.

PORTE pins are multiplexed with analog inputs. When selected as an analog input, these pins will read as '0's.

TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Note: On a Power-on Reset, these pins are configured as analog inputs and read as '0'.

#### FIGURE 4-7: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



# 6.0 TIMER1 MODULE

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L), which are readable and writable. The TMR1 Register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow, which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit TMR1IE (PIE1<0>).

Timer1 can operate in one of two modes:

- As a timer
- · As a counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Timer1 also has an internal "RESET input". This RESET can be generated by either of the two CCP modules as the special event trigger (see Sections 8.1 and 8.2). Register 6-1 shows the Timer1 Control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI/CCP2 and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored and these pins read as '0'.

Additional information on timer modules is available in the PICmicro<sup>™</sup> Mid-Range MCU Family Reference Manual (DS33023).

## REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	_	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N				
	bit 7							bit 0				
bit 7-6	Unimplemented: Read as '0'											
bit 5-4	T1CKPS1	:T1CKPS0:	Timer1 Inpu	ut Clock Pres	scale Select I	bits						
	11 = 1:8 Prescale value											
	10 = 1:4 Prescale value											
	01 = 1:2 P 00 = 1:1 P	rescale vali rescale vali	re Te									
bit 3	T1OSCEN: Timer1 Oscillator Enable Control bit											
	1 = Oscilla	ator is enabl	ed									
	0 = Oscilla	ator is shut-o	off (the oscill	ator inverter	is turned off	to eliminate	power draii	ר)				
bit 2	T1SYNC:	Timer1 Exte	ernal Clock I	nput Synchr	onization Co	ntrol bit						
	TMR1CS :	<u>= 1:</u>										
	1 = Do not	t synchroniz	e external c	lock input								
	0 = Synch	ronize exter	nal clock inp	out								
	TMR1CS :	<u>= 0:</u>			I I <b> </b>							
1 ** 4		ignorea. Tin	neri uses th	e internal ci	JCK when TW	$ \mathbf{R} ^{1}\mathbf{CS}=0.$						
Dit 1	IMR1CS:	Timer1 Clo	ck Source S	elect bit								
	1 = Extern 0 = Interna	al clock from	m pin RC0/T sc/4)	1050/110	(I (on the risi	ng edge)						
bit 0	TMR10N:	Timer1 On	bit									
	1 = Enable	es Timer1										
	0 = Stops	Timer1										
	Legend:											
	R = Reada	able bit	W = V	Nritable bit	U = Unin	nplemented	bit, read as	'0'				
	- n = Value	e at POR re	set '1' = l	Bit is set	'0' = Bit i	s cleared	x = Bit is ι	Inknown				

# 8.3 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1. An event is defined as one of the following and is configured by CCPxCON<3:0>:

- · Every falling edge
- · Every rising edge
- Every 4th rising edge
- Every 16th rising edge

An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. The interrupt flag must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value is overwritten by the new captured value.

## 8.3.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

**Note:** If the RC2/CCP1 pin is configured as an output, a write to the port can cause a capture condition.

#### FIGURE 8-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



## 8.3.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

## 8.3.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF following any such change in operating mode.

## 8.3.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any RESET will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore, the first capture may be from a non-zero prescaler. Example 8-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

#### EXAMPLE 8-1: CHANGING BETWEEN CAPTURE PRESCALERS

CLRF	CCP1CON	;Turn CCP module off
MOVLW	NEW_CAPT_PS	;Load the W reg with
		;the new prescaler
		;move value and CCP ON
MOVWF	CCP1CON	;Load CCP1CON with this
		;value

# 8.4 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- Driven high
- Driven low
- Remains unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.



#### COMPARE MODE OPERATION BLOCK DIAGRAM



Special Event Trigger will:

- clear TMR1H and TMR1L registers
- NOT set interrupt flag bit TMR1F (PIR1<0>)
- (for CCP2 only) set the GO/DONE bit (ADCON0<2>)

REGISTER 9-1:	SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)										
	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0			
	SMP	CKE	D/A	Р	S	R/W	UA	BF			
	bit 7	1 1						bit 0			
bit 7	SMP: SPI [	SMP: SPI Data Input Sample Phase bit									
	SPI Master	SPI Master mode:									
	1 = Input d	1 = Input data sampled at end of data output time									
	SPI Slave r	ala sampieu a mode:		uala oulpu		wile <sup>*</sup> )					
	SMP must	be cleared wh	nen SPI is u	used in Slav	ve mode						
	I <sup>2</sup> C mode:										
	This bit mu	st be maintair	ned clear								
bit 6	CKE: SPI (	Clock Edge Se	elect bit (Fig	gure 9-2, Fig	gure 9-3, and	d Figure 9-4	)				
	<u>SPI mode, CKP = 0:</u>										
	1 = Data tra	ansmitted on I	ising edge	of SCK (Mi	crowire <sup>®</sup> alte	ernate)					
	SPI mode	CKP = 1	annig euge								
	1 = Data tra	ansmitted on 1	alling edge	of SCK (M	icrowire <sup>®</sup> de	fault)					
	0 = Data tra	0 = Data transmitted on rising edge of SCK (Microwne * default)									
	I <sup>2</sup> C mode:										
	This bit must be maintained clear $\mathbf{P}(\mathbf{A}, \mathbf{P})$										
bit 5	<b>D/A:</b> Data/Address bit (I <sup>c</sup> C mode only)										
	1 = Indicate	0 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was address									
bit 4	<b>P</b> : STOP bit (I <sup>2</sup> C mode only)										
	This bit is cleared when the SSP module is disabled, or when the START bit is detected last. SSPEN is cleared.										
	<ul> <li>1 = Indicates that a STOP bit has been detected last (this bit is '0' on RESET)</li> <li>0 = STOP bit was not detected last</li> </ul>										
bit 3	S: START bit (I <sup>2</sup> C mode only) This bit is cleared when the SSP module is disabled, or when the STOP bit is detected last. SSPEN is cleared.										
	1 = Indicate 0 = START	es that a STAI bit was not d	RT bit has l etected las	been detect t	ed last (this l	bit is '0' on F	RESET)				
bit 2	<b>R/W</b> : Read/Write bit Information (I <sup>2</sup> C mode only)										
	This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next START bit. STOP bit or ACK bit										
	the address match to the next START bit, STOP bit, or AUK bit.										
	0 = Write										
bit 1	UA: Update	<b>UA</b> : Update Address bit (10-bit I <sup>2</sup> C mode only)									
	1 = Indicate 0 = Addres	es that the use is does not ne	er needs to ed to be up	update the dated	address in t	he SSPADD	) register				
bit 0	BF: Buffer	Full Status bit									
	<u>Receive (S</u>	Receive (SPI and I <sup>2</sup> C modes):									
	1 = Receive	1 = Receive complete, SSPBUF is full									
		0 = Receive not complete, SSPBUF is empty									
	<u>1 ransmit (i</u>	-C mode only	<u>):</u> 	io full							
	1 = Transfr 0 = Transfr	<ul> <li>1 = Transmit in progress, SSPBUF is full</li> <li>0 = Transmit complete, SSPBUF is empty</li> </ul>									
	Legend:										
	R = Readab	ole bit	W = W	ritable bit	U = Unim	plemented	bit, read as '	0'			
	- n = Value	at POR reset	'1' = Bi	t is set	'0' = Bit is	s cleared	x = Bit is u	nknown			

\_

#### FIGURE 9-1: SSP BLOCK DIAGRAM (SPI MODE)



To enable the serial port, SSP enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON register, and then set bit SSPEN. This configures the SDI, SDO, SCK, and SS pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set and ADCON must be configured such that RA5 is a digital I/O

Note 1: When the SPI is in Slave mode with SS pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the SS pin is set to VDD.

- 2: If the SPI is used in Slave mode with CKE = '1', then the SS pin control must be enabled.
- 3: When the SPI is in Slave mode with  $\overline{SS}$  pin control enabled (SSPCON<3:0> = '0100'), the state of the  $\overline{SS}$  pin can affect the state read back from the TRISC<5> bit. The Peripheral OE signal from the SSP module into PORTC controls the state that is read back from the TRISC<5> bit (see Section 4.3 for information on PORTC). If Read-Modify-Write instructions, such as BSF are performed on the TRISC register while the  $\overline{SS}$  pin is high, this will cause the TRISC<5> bit to be set, thus disabling the SDO output.

#### 9.3.2 MASTER MODE

Master mode of operation is supported in firmware using interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a RESET or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I<sup>2</sup>C bus may be taken when the P bit is set, or the bus is IDLE and both the S and P bits are clear.

In Master mode, the SCL and SDA lines are manipulated by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I<sup>2</sup>C module.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt will occur if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the Slave mode IDLE (SSPM3:SSPM0 = 1011), or with the Slave active. When both Master and Slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

#### 9.3.3 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the START and STOP conditions, allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a RESET or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the  $I^2C$  bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is IDLE and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In Multi-Master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to retransfer the data at a later time.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
13h	SSPBUF	Synchrono	us Serial	Port Rece	eive Buff	er/Transr	nit Registe	er		xxxx xxxx	uuuu uuuu
93h	SSPADD	Synchrono	us Serial	Port (I <sup>2</sup> C	mode) A	ddress R	egister			0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP <sup>(2)</sup>	CKE <sup>(2)</sup>	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000
87h	TRISC	PORTC Da	ata Direct	ion Regist	ter	•	•	•		1111 1111	1111 1111

 TABLE 9-3:
 REGISTERS ASSOCIATED WITH I<sup>2</sup>C OPERATION

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by SSP module in I<sup>2</sup>C mode. **Note 1:** PSPIF and PSPIE are reserved on the PIC16F73/76; always maintain these bits clear.

2: Maintain these bits clear in I<sup>2</sup>C mode.

	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R-0	R-x				
	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D				
	bit 7							bit 0				
bit 7	<b>SPEN:</b> Serial Port Enable bit 1 = Serial port enabled (configures RC7/RX/DT and RC6/TX/CK pins as serial port pins) 0 = Serial port disabled											
bit 6	<b>RX9</b> : 9-bit Receive Enable bit 1 = Selects 9-bit reception 0 = Selects 8-bit reception											
bit 5	SREN: Single Receive Enable bit <u>Asynchronous mode:</u> Don't care <u>Synchronous mode - Master:</u> 1 = Enables single receive 0 = Disables single receive This bit is cleared after reception is complete. <u>Synchronous mode - Slave:</u> Don't care											
bit 4	CREN: Continuous Receive Enable bit <u>Asynchronous mode:</u> 1 = Enables continuous receive 0 = Disables continuous receive <u>Synchronous mode:</u> 1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)											
bit 3	Unimplem	nented: Rea	d as '0'									
bit 2	<b>FERR</b> : Framing Error bit 1 = Framing error (can be updated by reading RCREG register and receive next valid byte) 0 = No framing error											
bit 1	<b>OERR</b> : Ov 1 = Overru 0 = No ove	OERR: Overrun Error bit 1 = Overrun error (can be cleared by clearing bit CREN) 0 = No overrun error										
bit 0	<b>RX9D:</b> 9th Can be pa	bit of Recei rity bit (parity	ved Data y to be calcu	lated by firmw	/are)							
	Legend:											
	R = Reada	able bit	W = W	/ritable bit	U = Unim	plemented	bit, read as	s 'O'				

'1' = Bit is set

'0' = Bit is cleared

#### REGISTER 10-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

- n = Value at POR reset

x = Bit is unknown

Steps to follow when setting up an Asynchronous Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 10.1).
- 2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- 3. If interrupts are desired, then set enable bit TXIE.
- 4. If 9-bit transmission is desired, then set transmit bit TX9.

- 5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Load data to the TXREG register (starts transmission).
- 8. If using interrupts, ensure that GIE and PEIE in the INTCON register are set.

## FIGURE 10-2: ASYNCHRONOUS MASTER TRANSMISSION



#### FIGURE 10-3: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)



#### TABLE 10-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	x000 - 0000	x00- 0000
19h	TXREG	USART Tra	ansmit Re	egister						0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Generat	0000 0000	0000 0000						

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission. Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F73/76; always maintain these bits clear.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	USART Tr	ansmit R	egister						0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC		BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	e Generat	0000 0000	0000 0000						

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F73/76 devices; always maintain these bits clear.

#### 10.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of the SLEEP mode. Bit SREN is a "don't care" in Slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Follow these steps when setting up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- 2. If interrupts are desired, set enable bit RCIE.
- 3. If 9-bit reception is desired, set bit RX9.
- 4. To enable reception, set enable bit CREN.
- 5. Flag bit RCIF will be set when reception is complete and an interrupt will be generated, if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 7. Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing bit CREN.
- 9. If using interrupts, ensure that GIE and PEIE in the INTCON register are set.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR		Value on all other RESETS	
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 0	00x	0000	000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0	000	0000	0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 0	00x	0000	000x
1Ah	RCREG	USART R	USART Receive Register									0000	0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0	000	0000	0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -	010	0000	-010
99h	SPBRG	Baud Rate	Baud Rate Generator Register										0000

#### TABLE 10-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous slave reception. **Note 1:** Bits PSPIE and PSPIF are reserved on the PIC16F73/76 devices, always maintain these bits clear.

# 12.3 **RESET**

The PIC16F7X differentiates between various kinds of RESET:

- Power-on Reset (POR)
- MCLR Reset during normal operation
- MCLR Reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)
- Brown-out Reset (BOR)

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset (POR), on the MCLR and WDT Reset, on MCLR Reset during SLEEP, and Brown-out Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The TO and PD bits are set or cleared differently in different RESET situations, as indicated in Table 12-4. These bits are used in software to determine the nature of the RESET. See Table 12-6 for a full description of RESET states of all registers.

A simplified block diagram of the on-chip RESET circuit is shown in Figure 12-4.





# 15.2 DC Characteristics: PIC16F73/74/76/77 (Industrial, Extended) PIC16LF73/74/76/77 (Industrial) (Continued)

DC CHA	ARACT	ERISTICS	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extendedOperating voltage VDD range as described in DC Specification, Section 15.1.								
Param No.	Sym	Characteristic Min Typ† Max Units Conditions									
	Vol	Output Low Voltage									
D080		I/O ports	—	_	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +125°C				
D083		OSC2/CLKOUT (RC osc config)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +125°C				
			—	—	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C				
	Vон	Output High Voltage				•					
D090		I/O ports (Note 3)	Vdd - 0.7	—	_	V	IOH = -3.0 mA, VDD = 4.5V, -40°С to +125°С				
D092		OSC2/CLKOUT (RC osc config)	Vdd - 0.7	—	—	V	ІОН = -1.3 mA, VDD = 4.5V, -40°C to +125°C				
			Vdd - 0.7	—	_	V	IOH = -1.0 mA, VDD = 4.5V, -40°С to +125°С				
D150*	Vod	Open Drain High Voltage		_	12	V	RA4 pin				
		Capacitive Loading Specs on C	Output Pir	IS							
D100	Cosc2	OSC2 pin	—		15	pF	In XT, HS and LP modes when external clock is used to drive OSC1				
D101	Сю	All I/O pins and OSC2 (in RC mode)	—	—	50	pF					
D102	Св	SCL, SDA in I <sup>2</sup> C mode	—	—	400	pF					
		Program FLASH Memory									
D130	Ер	Endurance	100	1000		E/W	25°C at 5V				
D131	Vpr	VDD for Read	2.0	_	5.5	V					

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
70*	TssL2scH, TssL2scL	$\overline{SS}$ ↓ to SCK↓ or SCK↑ input	Тсү		—	ns		
71*	TscH	SCK input high time (Slave mod	e)	TCY + 20	_	—	ns	
72*	TscL	SCK input low time (Slave mode	e)	TCY + 20	_		ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to S	100	_	_	ns		
74*	TscH2diL, TscL2diL	Hold time of SDI data input to S	100	_	_	ns		
75*	TdoR	SDO data output rise time	Standard( <b>F</b> ) Extended( <b>LF</b> )	_	10 25	25 50	ns ns	
76*	TdoF	SDO data output fall time	—	10	25	ns		
77*	TssH2doZ	SS↑ to SDO output hi-impedanc	10	_	50	ns		
78*	TscR	SCK output rise time Standard(F) (Master mode) Extended(LF)		_	10 25	25 50	ns ns	
79*	TscF	SCK output fall time (Master mo	de)	_	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	Standard( <b>F</b> ) Extended( <b>LF</b> )	—		50 145	ns ns	
81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK e	Тсу		_	ns		
82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$	_		50	ns		
83*	TscH2ssH, TscL2ssH	SS ↑ after SCK edge	1.5Tcy + 40		—	ns		

#### TABLE 15-7: SPI MODE REQUIREMENTS

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

#### FIGURE 15-15: I<sup>2</sup>C BUS START/STOP BITS TIMING





# FIGURE 16-3: TYPICAL IDD vs. Fosc OVER VDD (XT MODE)







FIGURE 16-5: TYPICAL IDD vs. Fosc OVER VDD (LP MODE)







#### FIGURE 16-19: MINIMUM AND MAXIMUM VIN vs. VDD, (TTL INPUT, -40°C TO 125°C)



