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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f215ret6tr

Contents

3 Functional overview

3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM® core, the STM32F21x family is compatible with all ARM® tools and software.

Figure 4 shows the general block diagram of the STM32F21x family.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M3 processors. It balances the inherent performance advantage of the ARM® Cortex®-M3 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher operating frequencies.

To release the processor full 150 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache which increases program execution speed from the 128-bit Flash memory. Based on CoreMark® benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The STM32F21x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbyte available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All STM32F21x products embed:

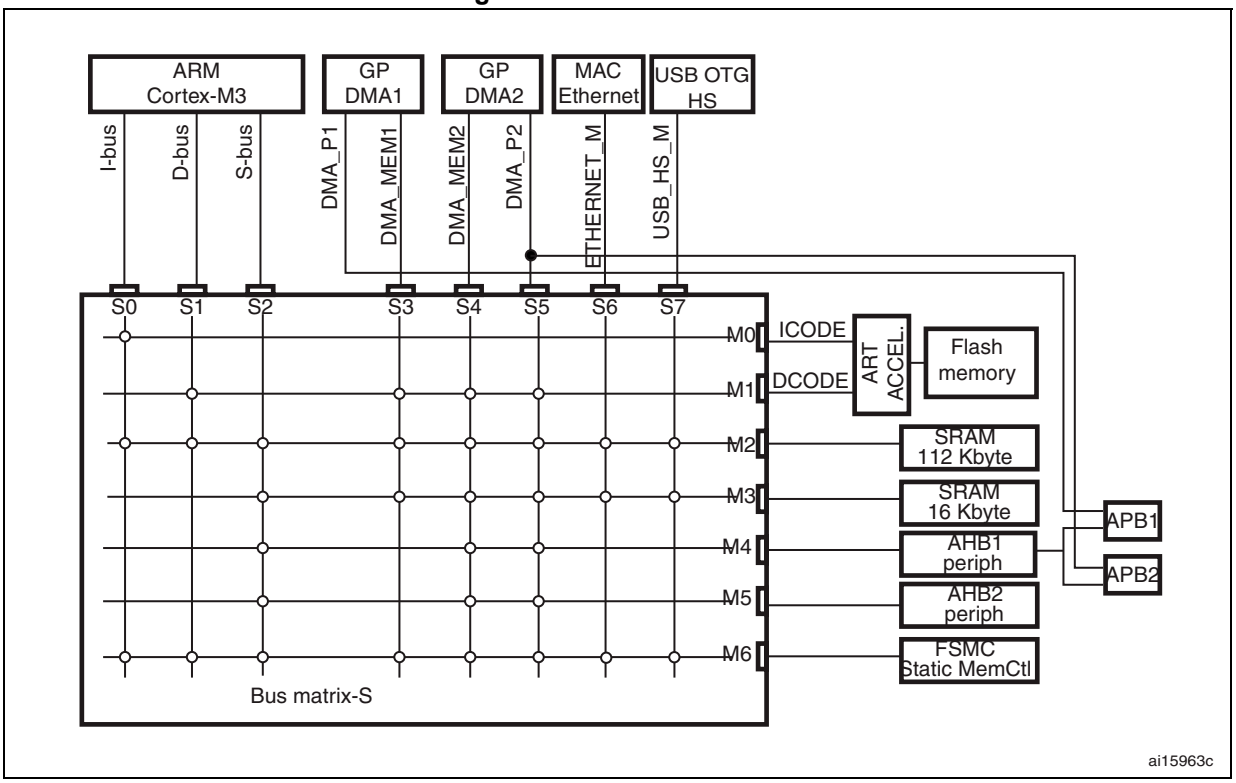
- Up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states
- 4 Kbytes of backup SRAM.

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.26 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F217xx devices.

The STM32F217xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F217xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F217xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F217xx.

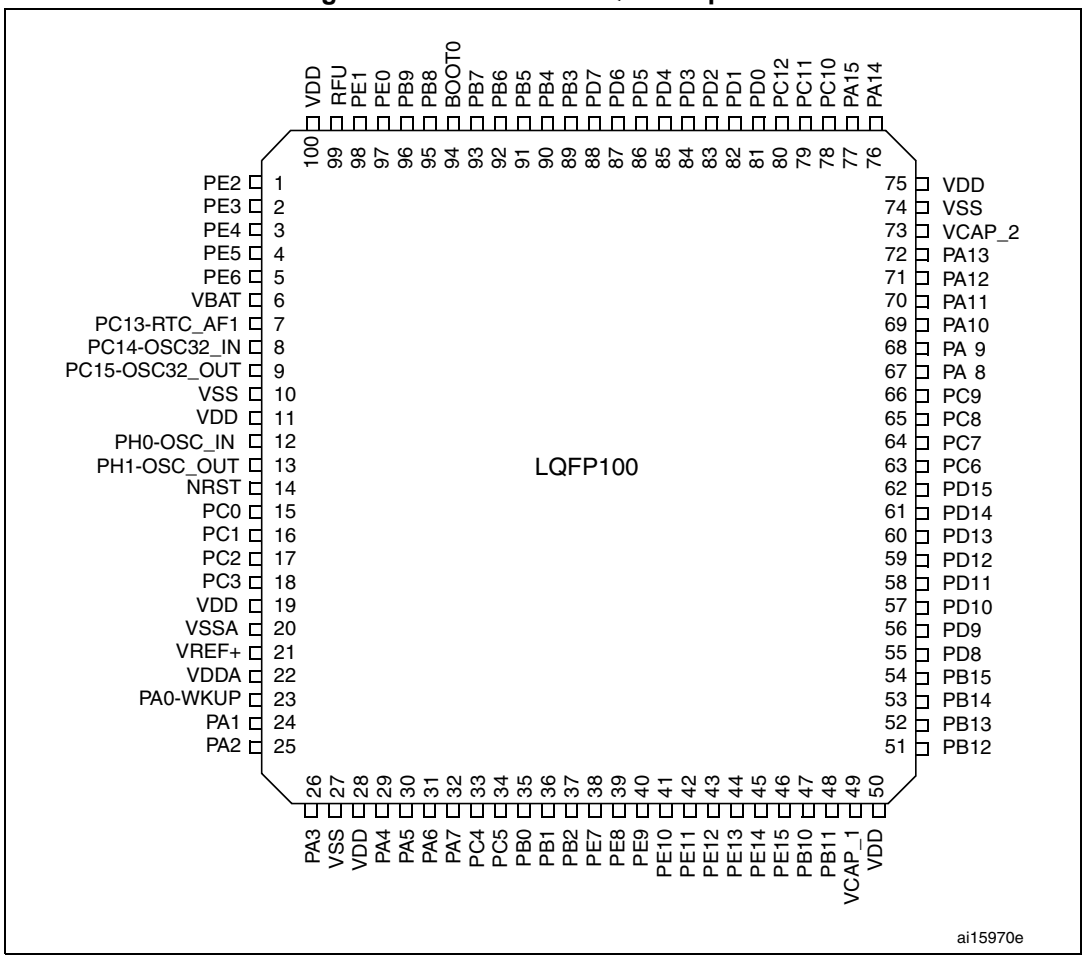
The STM32F217xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F20x and STM32F21x reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.27 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one

Figure 10. STM32F21x LQFP100 pinout



1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 7. STM32F21x pin and ball definitions (continued)

Pins					Pin name (function after reset)[1]	Pin type	I / O structure	Note	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	132	160	B7	PG15	I/O	FT	-	USART6_CTS, DCMI_D13, EVENTOUT	-
55	89	133	161	A10	PB3 (JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, SPI3_SCK, I2S3_SCK, TIM2_CH2, SPI1_SCK, EVENTOUT	-
56	90	134	162	A9	PB4	I/O	FT	-	NJTRST, SPI3_MISO, TIM3_CH1, SPI1_MISO, EVENTOUT	-
57	91	135	163	A6	PB5	I/O	FT	-	I2C1_SMBA, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT,TIM3_CH2, SPI1_MOSI, SPI3_MOSI, DCMI_D10, I2S3_SD, EVENTOUT	-
58	92	136	164	B6	PB6	I/O	FT	-	I2C1_SCL, TIM4_CH1, CAN2_TX, DCMI_D5,USART1_TX, EVENTOUT	-
59	93	137	165	B5	PB7	I/O	FT	-	I2C1_SDA, FSMC_NL[6], DCMI_VSYNC, USART1_RX, TIM4_CH2, EVENTOUT	-
60	94	138	166	D6	BOOT0	I	B	-	-	V_{PP}
61	95	139	167	A5	PB8	I/O	FT	-	TIM4_CH3,SDIO_D4, TIM10_CH1, DCMI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-
62	96	140	168	B4	PB9	I/O	FT	-	SPI2_NSS, I2S2_WS, TIM4_CH4, TIM11_CH1, SDIO_D5, DCMI_D7, I2C1_SDA, CAN1_TX, EVENTOUT	-
-	97	141	169	A4	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, DCMI_D2, EVENTOUT	-
-	98	142	170	A3	PE1	I/O	FT	-	FSMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	D5	V_{SS}	S		-	-	-

Table 8. FSMC pin definition (continued)

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PG3	-	A13	-	-	-
PG4	-	A14	-	-	-
PG5	-	A15	-	-	-
PG6	-	-	-	INT2	-
PG7	-	-	-	INT3	-
PD0	D2	D2	DA2	D2	Yes
PD1	D3	D3	DA3	D3	Yes
PD3	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	NE1	NE1	NCE2	Yes
PG9	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	-	-	-	-
PG12	-	NE4	NE4	-	-
PG13	-	A24	A24	-	-
PG14	-	A25	A25	-	-
PB7	-	NADV	NADV	-	Yes
PE0	-	NBL0	NBL0	-	Yes
PE1	-	NBL1	NBL1	-	Yes

Table 13. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD}(2)	1.8	3.6	
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	
V_{IN}	Input voltage on RST and FT pins	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	5.5	
		1.7 V ≤ V_{DD} ≤ 2 V	–0.3	5.2	
	Input voltage on TTa pins	-	–0.3	V_{DD}+0.3	
	Input voltage on BOOT0 pin	-	0	9	
V_{CAP1}	Internal core voltage to be supplied externally in REGOFF mode	-	1.1	1.3	
V_{CAP2}					
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LQFP64	-	444	mW
		LQFP100	-	434	
		LQFP144	-	500	
		LQFP176	-	526	
		UFBGA176	-	513	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(4)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(4)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 65: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
4. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 36. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode V_{DD} = 3.3 V	-	12	-	

Table 37. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization results, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

Table 45. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design, not tested in production.
2. Guaranteed by tests in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 44: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 44: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 36*.

Table 46. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS ports I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL ports I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL}(2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 37* and *Table 47*, respectively.

Unless otherwise specified, the parameters given in *Table 47* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

Table 47. I/O AC characteristics(1)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	2	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.8 V to 3.6 V	-	-	100	ns

6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 65* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 13*.

Table 65. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8(1)	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	V_{DDA} = 1.8 to 2.4 V	0.6	-	15	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	-	30	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz with 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance	-	1.5	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	4	-	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.5	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.3	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Table 80. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK}$ - 0.5	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK}$- 1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK}$- 3	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK}$+ 1.5	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}$	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK}$+ 1	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	$5T_{HCLK}$– 0.5	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK}$+ 1	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 69 through *Figure 72* represent synchronous waveforms, together with *Table 81* and *Table 82* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 74. SD default mode

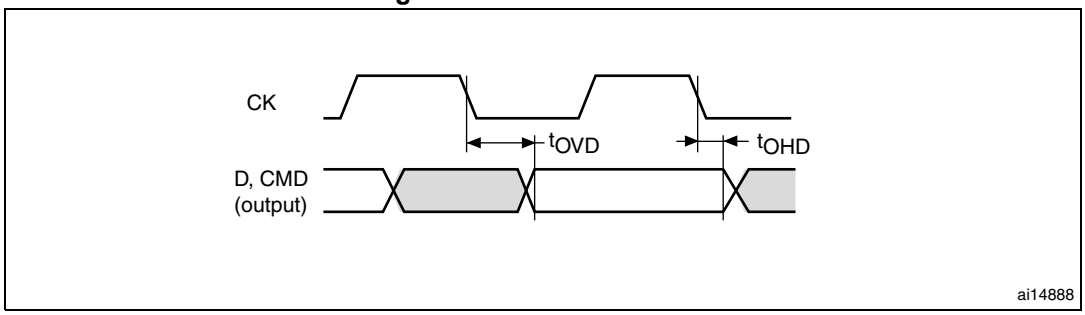


Table 84. SD/MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq 30$ pF	0	48	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	8/3	-
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	32	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	31	-	
t_r	Clock rise time	$C_L \leq 30$ pF	-	3.5	
t_f	Clock fall time	$C_L \leq 30$ pF	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	0.3	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

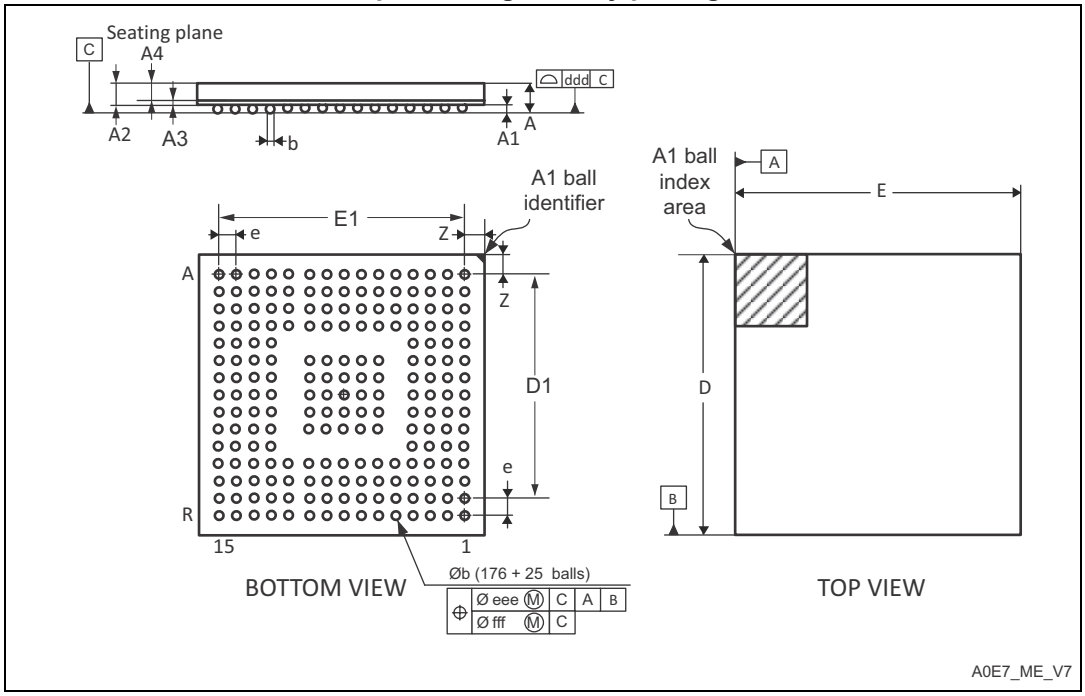
6.3.28 RTC characteristics

Table 85. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

7.5 UFBGA176+25 package information

Figure 85. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 90. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 94. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	4 (continued)	Updated $t_{res(TIM)}$ in *Table 49: Characteristics of TIMx connected to the APB1 domain*. Modified $t_{res(TIM)}$ and f_{EXT} *Table 50: Characteristics of TIMx connected to the APB2 domain*. Changed $t_{w(SCKH)}$ to $t_{w(SCLH)}$, $t_{w(SCKL)}$ to $t_{w(SCLL)}$, $t_{r(SCK)}$ to $t_{r(SCL)}$, and $t_{f(SCK)}$ to $t_{f(SCL)}$ in *Table 51: I2C characteristics* and *Figure 39: I2C bus AC waveforms and measurement circuit*. Added *Table 56: USB OTG FS DC electrical characteristics* and updated *Table 57: USB OTG FS electrical characteristics*. Updated V_{DD} minimum value in *Table 61: Ethernet DC electrical characteristics*. Updated *Table 65: ADC characteristics* and R_{AIN} equation. Updated R_{AIN} equation. Updated *Table 67: DAC characteristics*. Updated t_{START} in *Table 68: Temperature sensor characteristics*. Updated *Table 70: Embedded internal reference voltage*. Modified FSMC_NOE waveform in *Figure 55: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms*. Shifted end of FSMC_NEx/NADV/addresses/NWE/NOE/NWAIT of a half FSMC_CLK period, changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, and $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and updated data latency from 1 to 0 in *Figure 59: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 60: Synchronous multiplexed PSRAM write timings*, *Figure 61: Synchronous non-multiplexed NOR/PSRAM read timings*, and *Figure 62: Synchronous non-multiplexed PSRAM write timings*, Changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and modified $t_{w(CLK)}$ minimum value in *Table 75*, *Table 76*, *Table 77*, and *Table 78*. Updated R typical value in *Table 69: VBAT monitoring characteristics*.Updated note 2 in *Table 71*, *Table 72*, *Table 73*, *Table 74*, *Table 75*, *Table 76*, *Table 77*, and *Table 78*. Modified $t_{h(NIOWR-D)}$ in *Figure 68: PC Card/CompactFlash controller waveforms for I/O space write access*. Modified FSMC_NCEx signal in *Figure 69: NAND controller waveforms for read access*, *Figure 70: NAND controller waveforms for write access*, *Figure 71: NAND controller waveforms for common memory read access*, and *Figure 72: NAND controller waveforms for common memory write access*. Specified Full speed (FS) mode for *Figure 86: USB OTG HS peripheral-only connection in FS mode* and *Figure 87: USB OTG HS host-only connection in FS mode*.

Table 94. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	8 (continued)	Added *Figure 84: LQFP176 recommended footprint*. Added *Note 2* below *Figure 86: Regulator OFF/internal reset ON*. Updated device subfamily in *Table 93: Ordering information scheme*. Remove reference to note 2 for USB IOTG FS in *Table 93: Main applications versus package for STM32F2xxx microcontrollers*.
04-Nov-2013	9	Updated *Section 3.14: Power supply schemes*, *Section 3.15: Power supply supervisor*, *Section 3.16.1: Regulator ON* and *Section 3.16.2: Regulator OFF*. Added *Section 3.16.3: Regulator ON/OFF and internal reset ON/OFF availability*. Restructured RTC features and added reference clock detection in *Section 3.17: Real-time clock (RTC), backup SRAM and backup registers*. Added note indicating the package view below *Figure 9: STM32F21x LQFP64 pinout*, *Figure 10: STM32F21x LQFP100 pinout*, *Figure 11: STM32F21x LQFP144 pinout*, and *Figure 12: STM32F21x LQFP176 pinout*. Added *Table 6: Legend/abbreviations used in the pinout table*. *Table 7: STM32F21x pin and ball definitions*: content reformatted, removed indexes on V_{SS} and V_{DD}, updated PA4, PA5, PA6, PC4, BOOT0; replaced DCMI_12 by DCMI_D12, ETH_MII_RX_D0 by ETH_MII_RXD0, ETH_MII_RX_D1 by ETH_MII_RXD1, ETH_RMII_RX_D0 by ETH_RMII_RXD0, and ETH_RMII_RX_D1 by ETH_RMII_RXD1 in . *Table 9: Alternate function mapping*: replaced FSMC_BLN1 by FSMC_NBL1, added EVENTOUT as AF15 alternated function for PC13, PC14, PC15, PH0, PH1, and PI8. Updated *Figure 15: Pin loading conditions* and *Figure 16: Pin input voltage*. Added V_{IN} in *Table 13: General operating conditions*. Removed note applying to $V_{POR/PDR}$ minimum value in *Table 18: Embedded reset and power control block characteristics*. Updated notes related to C_{L1} and C_{L2} in *Section : Low-speed external clock generated from a crystal/ceramic resonator*. Updated conditions in *Table 40: EMS characteristics*. Updated *Table 41: EMI characteristics*. Updated V_{IL}, V_{IH} and V_{Hys} in *Table 45: I/O static characteristics*. Added *Section : Output driving current* and updated *Figure 37: I/O AC characteristics definition*. Updated $V_{IL(NRST)}$ and $V_{IH(NRST)}$ in *Table 48: NRST pin characteristics*, updated *Figure 37: I/O AC characteristics definition*. Removed tests conditions in *Section : I2C interface characteristics*. Updated *Table 51: I2C characteristics* and *Figure 39: I2C bus AC waveforms and measurement circuit*. Updated I_{VREF+} and I_{VDDA} in *Table 65: ADC characteristics*. Updated Offset comments in *Table 67: DAC characteristics*. Updated minimum $t_{h(CLKH-DV)}$ value in *Table 77: Synchronous non-multiplexed NOR/PSRAM read timings*.

Table 94. Document revision history (continued)

Date	Revision	Changes
04-Nov-2013	9 (continued)	Updated *Figure 75: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 86: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Updated *Figure 77: LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 80: LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline*, *Figure 83: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Updated *Figure 85: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline* and *Figure 85: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*. Removed Appendix A Application block diagrams.
27-Oct-2014	10	Updated V_{BAT} voltage range in *Figure 17: Power supply scheme*. Added caution note in *Section 6.1.6: Power supply scheme*. Updated V_{IN} in *Table 13: General operating conditions*. Removed note 1 in *Table 22: Typical and maximum current consumptions in Stop mode*. Updated *Table 44: I/O current injection susceptibility*, *Section 6.3.16: I/O port characteristics* and *Section 6.3.17: NRST pin characteristics*. Removed note 3 in *Table 68: Temperature sensor characteristics*. Added *Figure 79: LQFP100 marking (package top view)* and *Figure 82: LQFP144 marking (package top view)*.
23-Feb-2016	11	Updated *Section 1: Introduction*. Updated *Table 31: HSI oscillator characteristics* and its footnotes. Updated *Figure 34: PLL output clock waveforms in center spread mode*, *Figure 35: PLL output clock waveforms in down spread mode*, *Figure 52: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 53: Power supply and reference decoupling (VREF+ connected to VDDA)*. Updated *Section 7: Package information* and its subsections.
07-Jul-2016	12	Updated *Features* and *Section 2: Description*. Updated figures *1*, *2* and *3* in *Section 2.1: Full compatibility throughout the family*. Updated *Device marking* and *Figure 79* in *Section 7.2: LQFP100 package information*. Updated *Device marking* and *Figure 82* in *Section 7.3: LQFP144 package information*. Updated *Section 7.5: UFBGA176+25 package information* with introduction of *Device marking* and *Figure 87*. Updated *Table 93: Ordering information scheme*.
16-Aug-2016	13	Updated *Figure 52: Power supply and reference decoupling (VREF+ not connected to VDDA)*. Updated title of *Section 8: Ordering information*.