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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

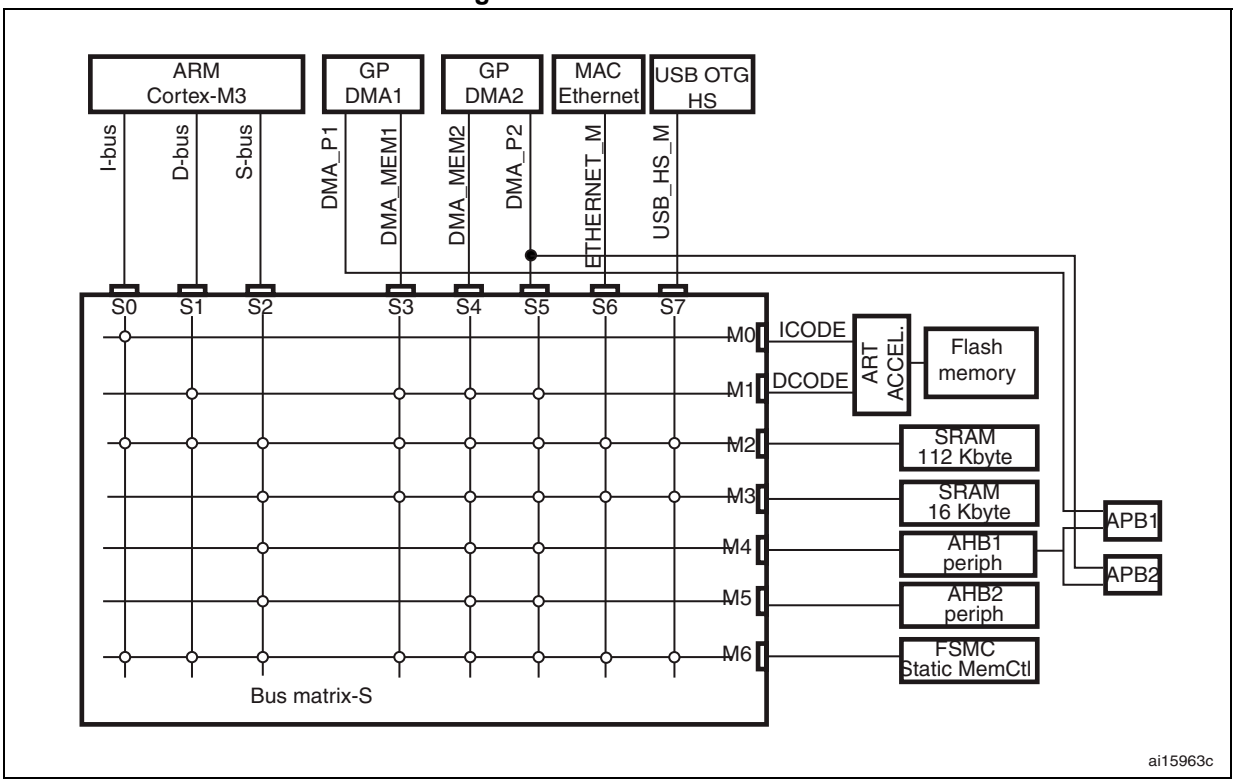
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f215rgt6tr

Table 2. STM32F215xx and STM32F217xx: features and peripheral counts (continued)

Peripherals	STM32F215Rx	STM32F215Vx	STM32F215Zx	STM32F217Vx	STM32F217Zx	STM32F217Ix
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C					
	Junction temperature: –40 to + 125 °C					
Package	LQFP64	LQFP100	LQFP144	LQFP100	LQFP144	UFBGA176, LQFP176

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. Camera interface and Ethernet are available only in STM32F217x devices.
3. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.

Figure 5. Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

3.30 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 kHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

3.31 Digital camera interface (DCMI)

The camera interface is not available in STM32F215xx devices.

STM32F217xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain up to 27 Mbyte/s at 27 MHz or 48 Mbyte/s at 48 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw Bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

Table 7. STM32F21x pin and ball definitions (continued)

Pins					Pin name (function after reset)(1)	Pin type	I / O structure	Note	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	14	20	J3	PF4	I/O	FT	(4)	FSMC_A4, EVENTOUT	ADC3_IN14
-	-	15	21	K3	PF5	I/O	FT	(4)	FSMC_A5, EVENTOUT	ADC3_IN15
-	10	16	22	G2	V_{SS}	S	-	-	-	-
-	11	17	23	G3	V_{DD}	S	-	-	-	-
-	-	18	24	K2	PF6	I/O	FT	(4)	TIM10_CH1, FSMC_NIORD, EVENTOUT	ADC3_IN4
-	-	19	25	K1	PF7	I/O	FT	(4)	TIM11_CH1, FSMC_NREG, EVENTOUT	ADC3_IN5
-	-	20	26	L3	PF8	I/O	FT	(4)	TIM13_CH1, FSMC_NIOWR, EVENTOUT	ADC3_IN6
-	-	21	27	L2	PF9	I/O	FT	(4)	TIM14_CH1, FSMC_CD, EVENTOUT	ADC3_IN7
-	-	22	28	L1	PF10	I/O	FT	(4)	FSMC_INTR, EVENTOUT	ADC3_IN8
5	12	23	29	G1	PH0/OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN(4)
6	13	24	30	H1	PH1/OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT(4)
7	14	25	31	J1	NRST	I/O	RST	-	-	-
8	15	26	32	M2	PC0	I/O	FT	(4)	OTG_HS_ULPI_STP, EVENTOUT	ADC123_ IN10
9	16	27	33	M3	PC1	I/O	FT	(4)	ETH_MDC, EVENTOUT	ADC123_ IN11
10	17	28	34	M4	PC2	I/O	FT	(4)	SPI2_MISO, OTG_HS_ULPI_DIR, ETH_MII_TXD2, EVENTOUT	ADC123_ IN12
11	18	29	35	M5	PC3	I/O	FT	(4)	SPI2_MOSI, I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, EVENTOUT	ADC123_ IN13
-	19	30	36	-	V_{DD}	S	-	-	-	-
12	20	31	37	M1	V_{SSA}	S	-	-	-	-
-	-	-	-	N1	V_{REF-}	S	-	-	-	-
-	21	32	38	P1	V_{REF+}	S	-	-	-	-

Table 7. STM32F21x pin and ball definitions (continued)

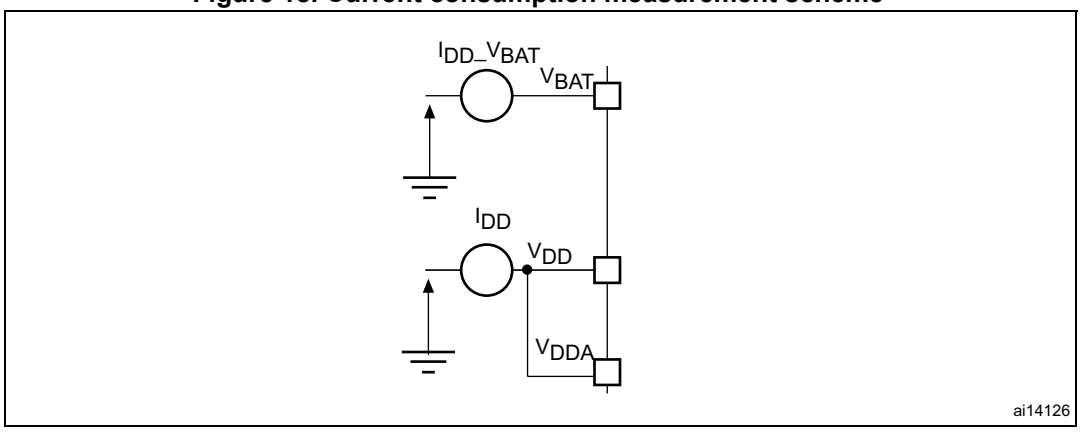
Pins					Pin name (function after reset)[1]	Pin type	I / O structure	Note	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	LQFP176	UFBGA176						
22	31	42	52	P3	PA6	I/O	FT	(4)	SPI1_MISO, TIM8_BKIN, TIM13_CH1, DCMI_PIXCLK, TIM3_CH1, TIM1_BKIN, EVENTOUT	ADC12_IN6
23	32	43	53	R3	PA7	I/O	FT	(4)	SPI1_MOSI, TIM8_CH1N, TIM14_CH1, TIM3_CH2, ETH_MII_RX_DV, TIM1_CH1N, ETH_RMII_CRS_DV, EVENTOUT	ADC12_IN7
24	33	44	54	N5	PC4	I/O	FT	(4)	ETH_RMII_RXD0,/ ETH_MII_RXD0, EVENTOUT	ADC12_IN14
25	34	45	55	P5	PC5	I/O	FT	(4)	ETH_RMII_RXD1, ETH_MII_RXD1, EVENTOUT	ADC12_IN15
26	35	46	56	R5	PB0	I/O	FT	(4)	TIM3_CH3, TIM8_CH2N, OTG_HS_ULPI_D1, ETH_MII_RXD2, TIM1_CH2N, EVENTOUT	ADC12_IN8
27	36	47	57	R4	PB1	I/O	FT	(4)	TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, TIM1_CH3N, EVENTOUT	ADC12_IN9
28	37	48	58	M6	PB2/BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	49	59	R6	PF11	I/O	FT	-	DCMI_D12, EVENTOUT	-
-	-	50	60	P6	PF12	I/O	FT	-	FSMC_A6, EVENTOUT	-
-	-	51	61	M8	V_{SS}	S	-	-	-	-
-	-	52	62	N8	V_{DD}	S	-	-	-	-
-	-	53	63	N6	PF13	I/O	FT	-	FSMC_A7, EVENTOUT	-
-	-	54	64	R7	PF14	I/O	FT	-	FSMC_A8, EVENTOUT	-
-	-	55	65	P7	PF15	I/O	FT	-	FSMC_A9, EVENTOUT	-
-	-	56	66	N7	PG0	I/O	FT	-	FSMC_A10, EVENTOUT	-
-	-	57	67	M7	PG1	I/O	FT	-	FSMC_A11, EVENTOUT	-
-	38	58	68	R8	PE7	I/O	FT	-	FSMC_D4, TIM1_ETR, EVENTOUT	-

Table 8. FSMC pin definition (continued)

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PF2	A2	A2	-	-	-
PF3	A3	A3	-	-	-
PF4	A4	A4	-	-	-
PF5	A5	A5	-	-	-
PF6	NIORD	-	-	-	-
PF7	NREG	-	-	-	-
PF8	NIOWR	-	-	-	-
PF9	CD	-	-	-	-
PF10	INTR	-	-	-	-
PF12	A6	A6	-	-	-
PF13	A7	A7	-	-	-
PF14	A8	A8	-	-	-
PF15	A9	A9	-	-	-
PG0	A10	A10	-	-	-
PG1	-	A11	-	-	-
PE7	D4	D4	DA4	D4	Yes
PE8	D5	D5	DA5	D5	Yes
PE9	D6	D6	DA6	D6	Yes
PE10	D7	D7	DA7	D7	Yes
PE11	D8	D8	DA8	D8	Yes
PE12	D9	D9	DA9	D9	Yes
PE13	D10	D10	DA10	D10	Yes
PE14	D11	D11	DA11	D11	Yes
PE15	D12	D12	DA12	D12	Yes
PD8	D13	D13	DA13	D13	Yes
PD9	D14	D14	DA14	D14	Yes
PD10	D15	D15	DA15	D15	Yes
PD11	-	A16	A16	CLE	Yes
PD12	-	A17	A17	ALE	Yes
PD13	-	A18	A18	-	Yes
PD14	D0	D0	DA0	D0	Yes
PD15	D1	D1	DA1	D1	Yes
PG2	-	A12	-	-	-

6.1.7 Current consumption measurement

Figure 18. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 10: Voltage characteristics*, *Table 11: Current characteristics*, and *Table 12: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five-volt tolerant pin(2)	V_{SS}–0.3	V_{DD}+4	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 11* for the values of the maximum allowed injected current.

Table 14. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency ($f_{Flashmax}$)	Number of wait states at maximum CPU frequency (f_{CPUmax}= 120 MHz)(1)	I/O operation	FSMC_CLK frequency for synchronous accesses	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V	Conversion time up to 1 Msps	16 MHz with no Flash memory wait state	7(2)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1 Msps	18 MHz with no Flash memory wait state	6(2)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2 Msps	24 MHz with no Flash memory wait state	4(2)	– Degraded speed performance – I/O compensation works	Up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(3)	Conversion time up to 2 Msps	30 MHz with no Flash memory wait state	3(2)	– Full-speed operation – I/O compensation works	– Up to 60 MHz when V_{DD} = 3.0 to 3.6 V – Up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 19*).
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

Table 18. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}$(1)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(1)(2)	Reset temporization	-	0.5	1.5	3.0	ms
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed by design, not tested in production.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

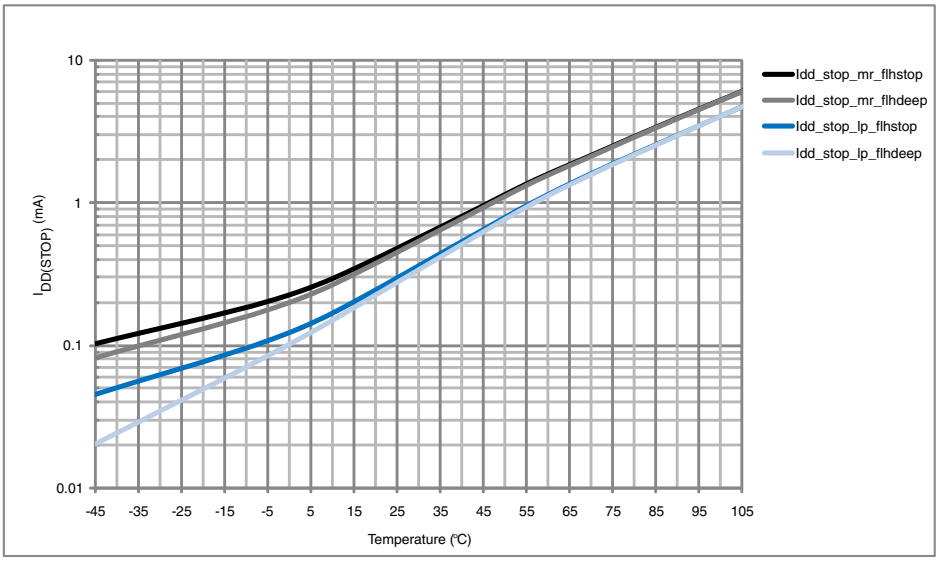
The current consumption is measured as described in *Figure 18: Current consumption measurement scheme*.

All Run mode current consumption measurements given in this section are performed using CoreMark® code.

Table 22. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.55	1.2	11.00	20.00	mA
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.50	1.2	11.00	20.00	
	Supply current in Stop mode with main regulator in Low-power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.35	1.1	8.00	15.00	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.30	1.1	8.00	15.00	

Figure 27. Typical current consumption vs. temperature in Stop mode



1. All typical and maximum values from table 18 and figure 26 will be reduced over time by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes

Table 25. Peripheral current consumption (continued)

Peripheral[1]		Typical consumption at 25 °C	Unit
APB1	TIM2	0.61	mA
	TIM3	0.49	
	TIM4	0.54	
	TIM5	0.62	
	TIM6	0.20	
	TIM7	0.20	
	TIM12	0.36	
	TIM13	0.28	
	TIM14	0.25	
	USART2	0.25	
	USART3	0.25	
	UART4	0.25	
	UART5	0.26	
	I2C1	0.25	
	I2C2	0.25	
	I2C3	0.25	
	SPI2	0.20/0.10	
	SPI3	0.18/0.09	
	CAN1	0.31	
	CAN2	0.30	
	DAC channel 1[2]	1.11	
	DAC channel 1[3]	1.11	
	PWR	0.15	
	WWDG	0.15	

Figure 34 and *Figure 35* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 34. PLL output clock waveforms in center spread mode

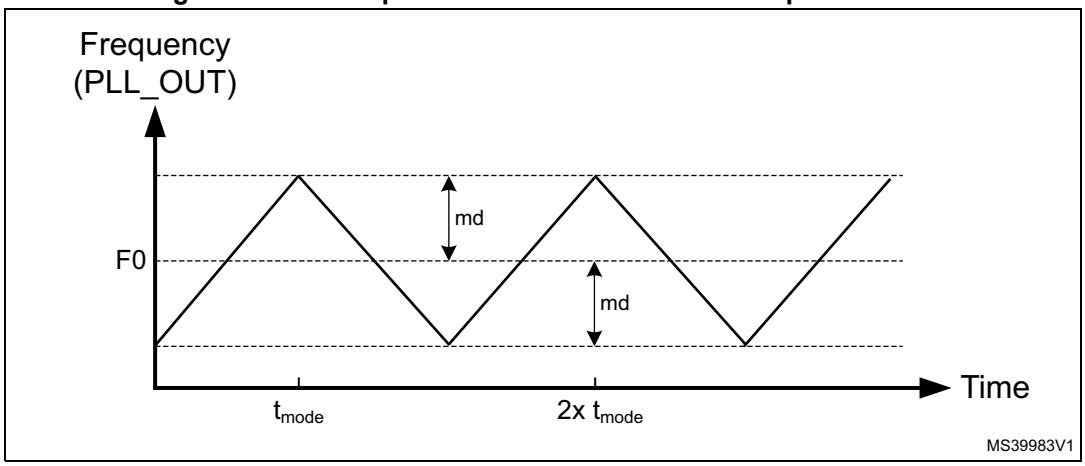
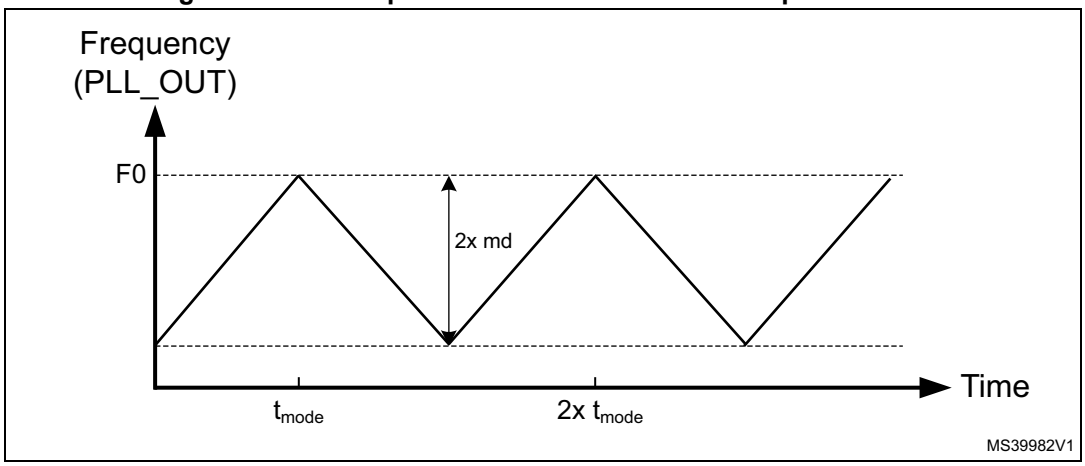


Figure 35. PLL output clock waveforms in down spread mode

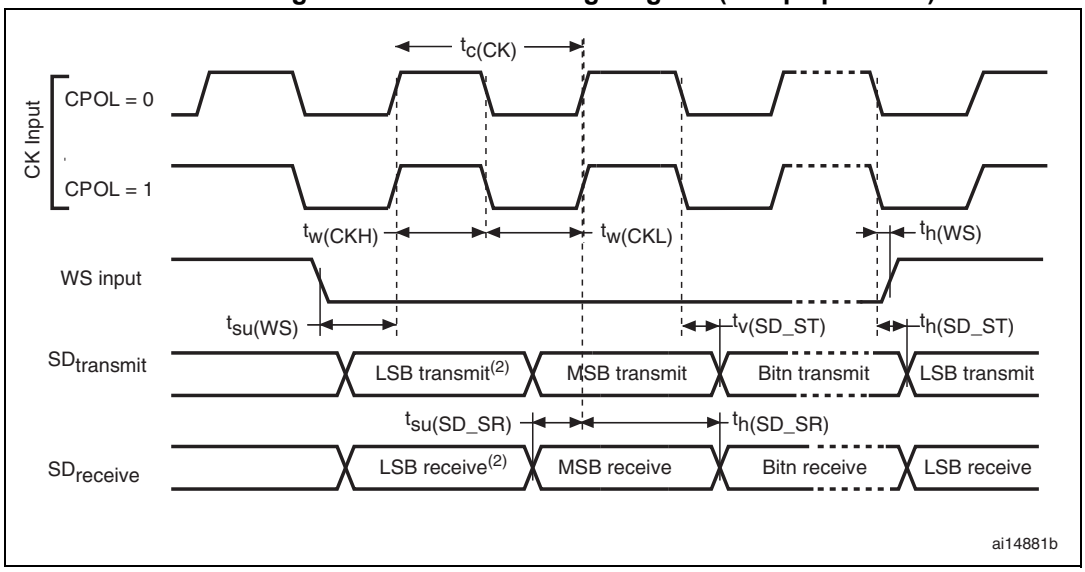


6.3.12 Memory characteristics

Flash memory

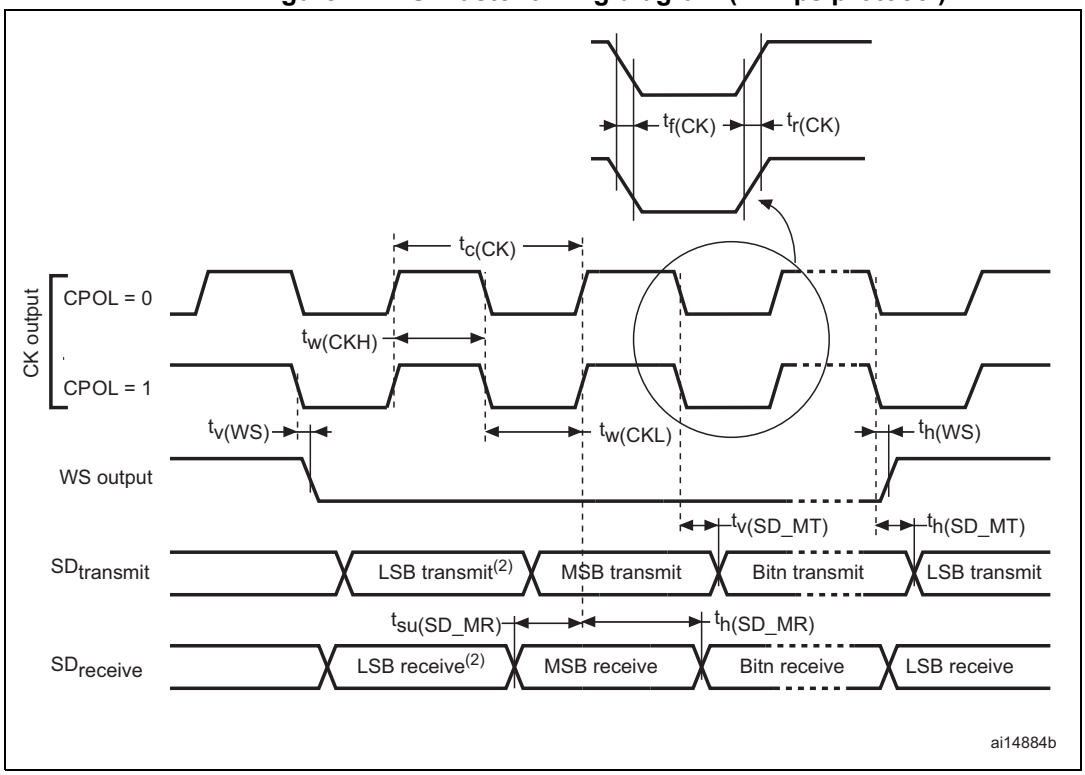
The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Figure 43. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

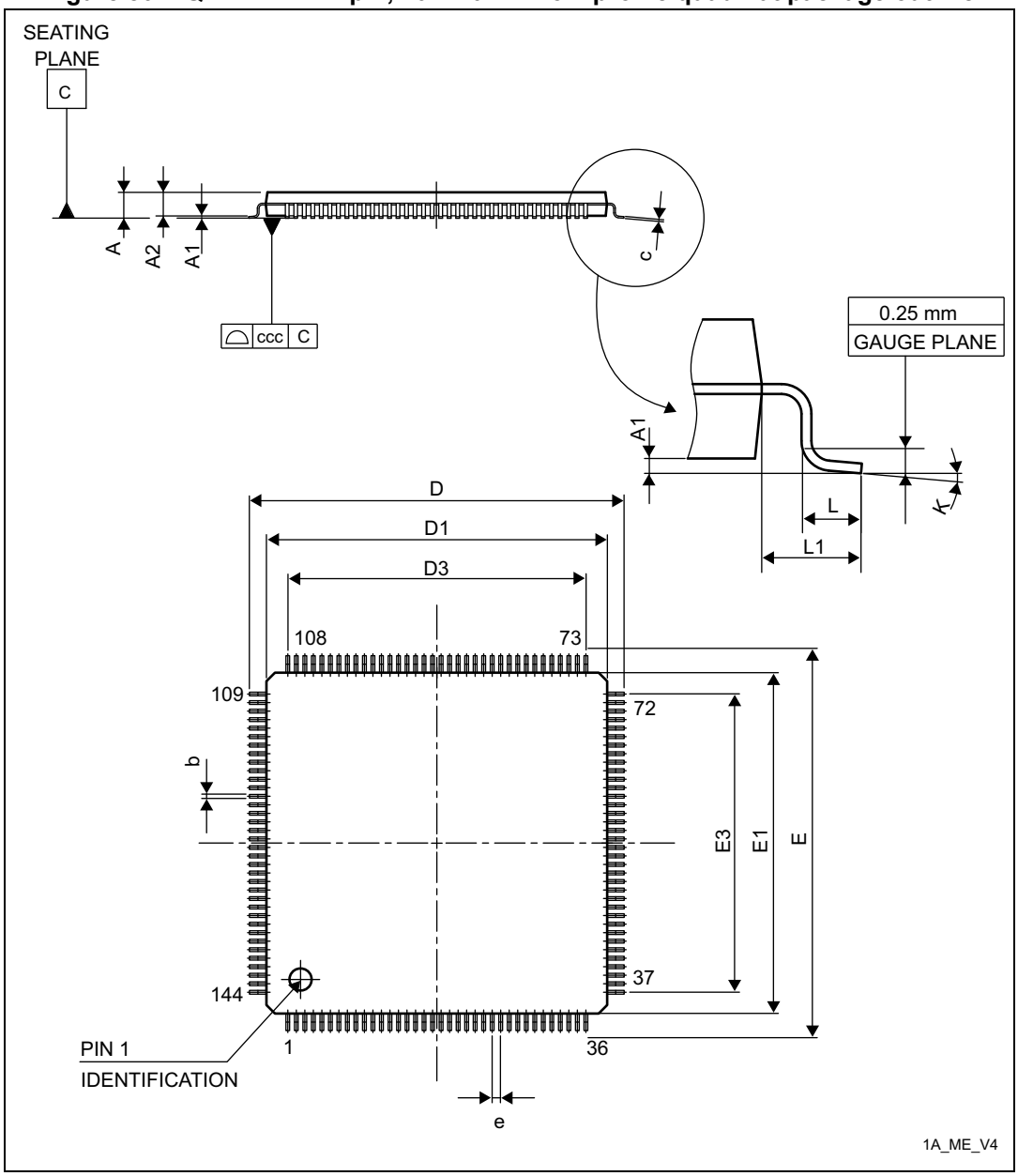
Figure 44. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

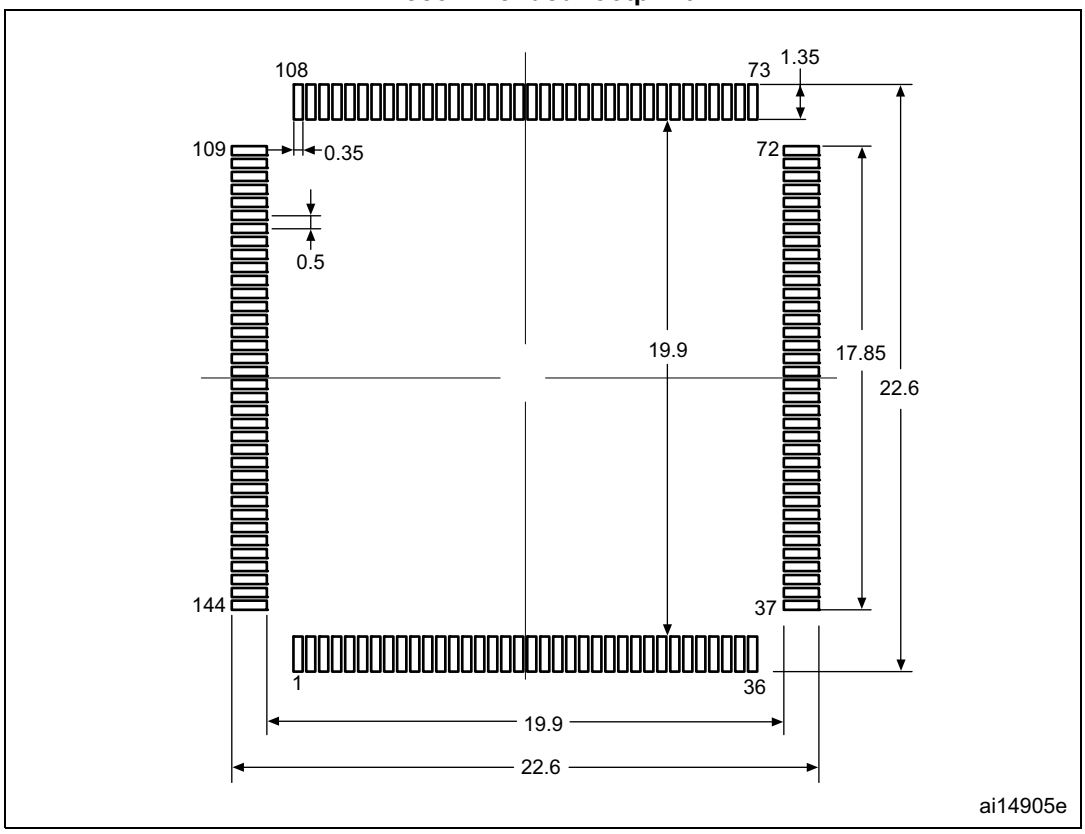
7.3 LQFP144 package information

Figure 80. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



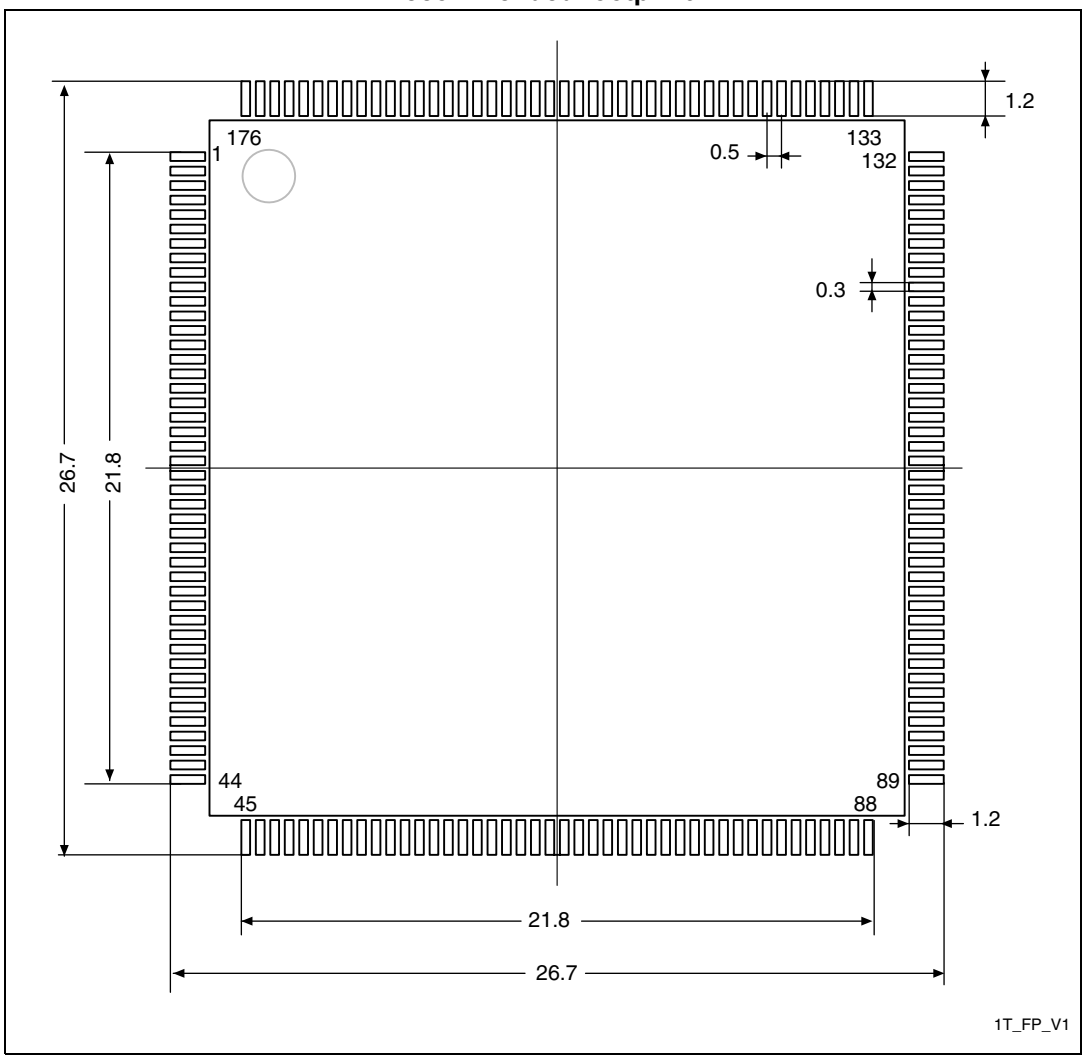
1. Drawing is not to scale.

Figure 81. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

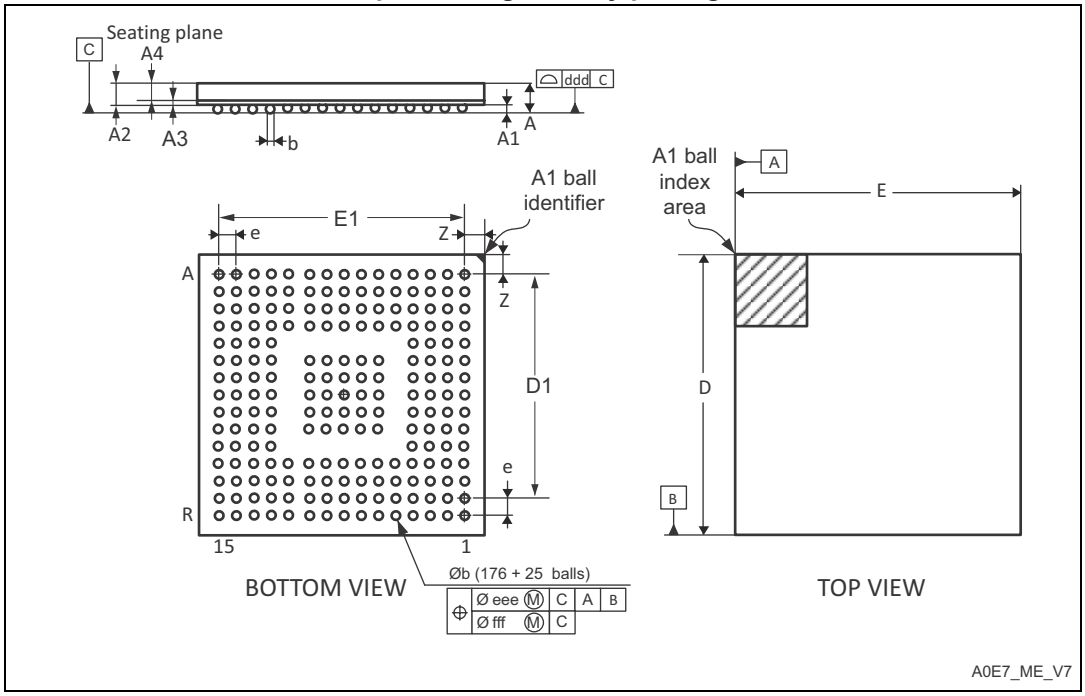
Figure 84. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.5 UFBGA176+25 package information

Figure 85. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 90. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 94. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	4 (continued)	Updated *Typical and maximum current consumption* conditions, as well as *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)* and *Table 19: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*. Added *Figure 21*, *Figure 22*, *Figure 23*, and *Figure 24*. Updated *Table 21: Typical and maximum current consumption in Sleep mode*, and added *Figure 25* and *Figure 26*. Updated *Table 23: Typical and maximum current consumptions in Standby mode* and *Table 24: Typical and maximum current consumptions in VBAT mode*. Updated *Table 22: Typical and maximum current consumptions in Stop mode*. Added *Figure 27: Typical current consumption vs. temperature in Stop mode*. Updated *Table 23: Typical and maximum current consumptions in Standby mode* and *Table 24: Typical and maximum current consumptions in VBAT mode*. Updated *On-chip peripheral current consumption* conditions and *Table 25: Peripheral current consumption*. Updated $t_{WUSTDBY}$ and t_{WUSTOP}, and added *Note 3* in *Table 26: Low-power mode wakeup timings*. Maximum f_{HSE_ext} and minimum $t_{w(HSE)}$ values updated in *Table 27: High-speed external user clock characteristics*. Updated C and g_m in *Table 29: HSE 4-26 MHz oscillator characteristics*. Updated R_F, I_2, g_m, and $t_{su(LSE)}$ in *Table 30: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Added *Note 3* and updated ACC_{HSI}, $IDD_{(HSI)}$ and $t_{su(HSI)}$ in *Table 31: HSI oscillator characteristics*. Added *Figure 32: ACCHSI versus temperature* Updated f_{LSI}, $t_{su(LSI)}$ and $IDD_{(LSI)}$ in *Table 32: LSI oscillator characteristics*. *Table 33: Main PLL characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLL)}$ and $IDD_{A(PLL)}$, added *Note 2* for f_{PLL_IN} minimum and maximum values. *Table 34: PLLI2S (audio PLL) characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLLI2S)}$ and $IDD_{A(PLLI2S)}$, added *Note 2* for f_{PLLI2S_IN} minimum and maximum values. Added *Note 1* in *Table 35: SSCG parameters constraint*. Updated *Table 36: Flash memory characteristics*. Modified *Table 37: Flash memory programming* and added *Note 1* for t_{prog}. Updated t_{prog} and added *Note 1* in *Table 38: Flash memory programming with VPP*. Modified *Figure 38: Recommended NRST pin protection*. Updated *Table 41: EMI characteristics* and EMI monitoring conditions in *Section : Electromagnetic Interference (EMI)*. Added *Note 2* related to $V_{ESD(HBM)}$ in *Table 42: ESD absolute maximum ratings*. Added *Section 6.3.15: I/O current injection characteristics*. Updated *Table 45: I/O static characteristics*. Modified maximum frequency values and conditions in *Table 47: I/O AC characteristics*.

Table 94. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	8	Removed Figure 4. Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package. Updated number of AHB buses in *Section 2: Description* and *Section 3.12: Clocks and startup*. Updated *Note 2* below *Figure 4: STM32F21x block diagram*. Changed System memory to System memory + OTP in *Figure 14: Memory map*. Added *Note 1* below *Table 15: VCAP1/VCAP2 operating conditions*. Updated V_{DDA} and V_{REF+} decoupling capacitor in *Figure 17: Power supply scheme* and updated *Note 3*. Changed simplex mode into half-duplex mode in *Section 3.24: Inter-integrated sound (I2S)*. Replaced DAC1_OUT and DAC2_OUT by DAC_OUT1 and DAC_OUT2, respectively. Changed TIM2_CH1/TIM2_ETR into TIM2_CH1_ETR for PA0 and PA5 in *Table 9: Alternate function mapping*. Updated note applying to I_{DD} (external clock and all peripheral disabled) in *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*. Updated *Note 3* below *Table 21: Typical and maximum current consumption in Sleep mode*. Removed f_{HSE_ext} typical value in *Table 27: High-speed external user clock characteristics*. Updated master I2S clock jitter conditions and values in *Table 34: PLLI2S (audio PLL) characteristics*. Updated equations in *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Swapped TTL and CMOS port conditions for V_{OL} and V_{OH} in *Table 46: Output voltage characteristics*. Updated $V_{IL(NRST)}$ and $V_{IH(NRST)}$ in *Table 48: NRST pin characteristics*. Updated *Table 53: SPI characteristics* and *Table 54: I2S characteristics*.Removed note 1 related to measurement points below *Figure 41: SPI timing diagram - slave mode and CPHA = 1*, *Figure 42: SPI timing diagram - master mode*, and *Figure 43: I2S slave timing diagram (Philips protocol)(1)*. Updated t_{HC} in *Table 60: ULPI timing*. Updated *Figure 47: Ethernet SMI timing diagram*, *Table 62: Dynamics characteristics: Ethernet MAC signals for SMI* and *Table 63: Dynamics characteristics: Ethernet MAC signals for RMII*. Update f_{TRIG} in *Table 65: ADC characteristics*. Updated I_{DDA} description in *Table 67: DAC characteristics*. Updated note below *Figure 52: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 53: Power supply and reference decoupling (VREF+ connected to VDDA)*. Replaced $t_{d(CLKL-NOEL)}$ by $t_{d(CLKH-NOEL)}$ in *Table 75: Synchronous multiplexed NOR/PSRAM read timings*, *Table 77: Synchronous non-multiplexed NOR/PSRAM read timings*, *Figure 59: Synchronous multiplexed NOR/PSRAM read timings* and *Figure 61: Synchronous non-multiplexed NOR/PSRAM read timings*.