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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f215zgt6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Figure 4. STM32F21x block diagram

1. The timers connected to APB2 are clocked from TIMxCLK up to 120 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 60 MHz.

2. The camera interface and Ethernet are available only in STM32F217xx devices.



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Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock	Max timer clock
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
Basic	TIM6, TIM7	16-bit	Any integer Up between 1 Yes 0 and 65536		No	30 MHz	60 MHz		
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	60 MHz	120 MHz
General	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	60 MHz	120 MHz
purpose	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	30 MHz	60 MHz
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	30 MHz	60 MHz

Table 4. Timer feature comparison (continued)

3.20.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.



3.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F21x devices (see *Table 4* for differences).

TIM2, TIM3, TIM4, TIM5

The STM32F21x include 4 full-featured general-purpose timers. TIM2 and TIM5 are 32-bit timers, and TIM3 and TIM4 are 16-bit timers. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

The counters of TIM2, TIM3, TIM4, TIM5 can be frozen in debug mode. Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases.

3.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

3.20.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout



The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.26 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F217xx devices.

The STM32F217xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard mediumindependent interface (MII) or a reduced medium-independent interface (RMII). The STM32F217xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F217xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F217xx.

The STM32F217xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F20x and STM32F21x reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.27 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one



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3.31.1 Cryptographic acceleration

The STM32F215xx and STM32F217xx devices embed a cryptographic accelerator. This cryptographic accelerator provides a set of hardware acceleration for the advanced cryptographic algorithms usually needed to provide confidentiality, authentication, data integrity and non repudiation when exchanging messages with a peer.

These algorithms consists of:

Encryption/Decryption

- DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
- AES (advanced encryption standard): ECB, CBC and CTR (counter mode) chaining algorithms, 128, 192 or 256-bit key

Universal hash

- SHA-1 (secure hash algorithm)
- MD5
- It also provides a true random number generator that deliver 32-bit random numbers produced by an integrated analog circuit.

3.32 True random number generator (RNG)

All STM32F2xxx products embed a true RNG that delivers 32-bit random numbers produced by an integrated analog circuit.

3.33 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

To provide fast I/O handling, the GPIOs are on the fast AHB1 bus with a clock up to 120 MHz that leads to a maximum I/O toggling speed of 60 MHz.

3.34 ADCs (analog-to-digital converters)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold





3.38 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F21x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.



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			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13		
	Port		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	12C1/12C2/12C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ЕТН	FSMC/SDIO/ OTG_HS	DCMI	AF014	AF15
		PH0 - OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
		PH1 - OSC_OUT	-	-				-	-	-	-	-	-	-	-	-	-	EVENTOUT
		PH2	-	-				-	-	-	-	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
		PH3	-	-				-	-	-	-	-	-	ETH_MII_COL	-	-	-	EVENTOUT
		PH4	-	-			I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_N XT	-	-	-	-	EVENTOUT
		PH5	-	-			I2C2_SDA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
		PH6	-	-			I2C2_SMBA	-	-	-	-	TIM12_CH1	-	ETH_MII_RXD2	-	-	-	EVENTOUT
,	Dort Ll	PH7	-	-			I2C3_SCL	-	-	-	-	-	-	ETH_MII_RXD3	-	-	-	EVENTOUT
ſ	-on n	PH8	-	-			I2C3_SDA	-	-	-	-	-	-	-	-	DCMI_HSYNC	-	EVENTOUT
		PH9	-	-			I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	-	DCMI_D0	-	EVENTOUT
		PH10	-	-	TIM5_CH1			-	-	-	-	-	-	-	-	DCMI_D1	-	EVENTOUT
		PH11	-	-	TIM5_CH2			-	-	-	-	-	-	-	-	DCMI_D2	-	EVENTOUT
		PH12	-	-	TIM5_CH3			-	-	-	-	-	-	-	-	DCMI_D3	-	EVENTOUT
		PH13	-	-		TIM8_CH1N		-	-	-	-	CAN1_TX	-	-	-	-	-	EVENTOUT
		PH14	-	-		TIM8_CH2N		-	-	-	-	-	-	-	-	DCMI_D4	-	EVENTOUT
		PH15	-	-		TIM8_CH3N		-	-	-	-	-	-	-	-	DCMI_D11	-	EVENTOUT
_		PI0	-	-	TIM5_CH4			SPI2_NSS I2S2_WS	-	-	-	-	-	-	-	DCMI_D13	-	EVENTOUT
		PI1	-	-				SPI2_SCK I2S2_SCK	-	-	-	-	-	-	-	DCMI_D8	-	EVENTOUT
		Pl2	-	-		TIM8_CH4		SPI2_MISO	-	-	-	-	-	-	-	DCMI_D9	-	EVENTOUT
		PI3	-	-		TIM8_ETR		SPI2_MOSI I2S2_SD	-	-	-	-	-	-	-	DCMI_D10	-	EVENTOUT
		Pl4	-	-		TIM8_BKIN			-	-	-	-	-	-	-	DCMI_D5	-	EVENTOUT
		PI5	-	-		TIM8_CH1		-	-	-	-	-	-	-	-	DCMI_VSYNC	-	EVENTOUT
	Port I	PI6	-	-		TIM8_CH2		-	-	-	-	-	-	-	-	DCMI_D6	-	EVENTOUT
		PI7	-	-		TIM8_CH3		-	-	-	-	-	-	-	-	DCMI_D7	-	EVENTOUT
		PI8	-	-				-	-	-	-	-	-	-	-	-	-	EVENTOUT
		PI9	-	-				-	-	-	-	CAN1_RX	-	-	-	-	-	EVENTOUT
		PI10	-	-				-	-	-	-	-	-	ETH _MII_RX_ER	-	-	-	EVENTOUT
		PI11	-	-				-	-	-	-	-	OTG_HS_ULPI_ DIR	-	-	-	-	EVENTOUT

Table 9. Alternate function mapping (continued)

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Operating power supply range	ADC operation	Maximum Flash memory access frequency (f _{Flashmax})	Number of wait states at maximum CPU frequency (f _{CPUmax} = 120 MHz) ⁽¹⁾	I/O operation	FSMC_CLK frequency for synchronous accesses	Possible Flash memory operations
V _{DD} =1.8 to 2.1 V	Conversion time up to 1 Msps	16 MHz with no Flash memory wait state	7 ⁽²⁾	 Degraded speed performance No I/O compensation 	Up to 30 MHz	8-bit erase and program operations only
V _{DD} = 2.1 to 2.4 V	Conversion time up to 1 Msps	18 MHz with no Flash memory wait state	6 ⁽²⁾	 Degraded speed performance No I/O compensation 	Up to 30 MHz	16-bit erase and program operations
V _{DD} = 2.4 to 2.7 V	Conversion time up to 2 Msps	24 MHz with no Flash memory wait state	4 ⁽²⁾	 Degraded speed performance I/O compensation works 	Up to 48 MHz	16-bit erase and program operations
V _{DD} = 2.7 to 3.6 V ⁽³⁾	Conversion time up to 2 Msps	30 MHz with no Flash memory wait state	3(2)	 Full-speed operation I/O compensation works 	$\begin{array}{c} - \mbox{ Up to} \\ 60\mbox{ MHz} \\ \mbox{when } \mbox{V}_{DD} = \\ 3.0\mbox{ to } 3.6\mbox{ V} \\ - \mbox{ Up to} \\ 48\mbox{ MHz} \\ \mbox{when } \mbox{V}_{DD} = \\ 2.7\mbox{ to } 3.0\mbox{ V} \end{array}$	32-bit erase and program operations

Table 14. Limitations depending on the operating power supply range

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 19*).

2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.

3. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.





Figure 19. Number of wait states versus $f_{\mbox{CPU}}$ and $V_{\mbox{DD}}$ range

6.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor to the VCAP1/VCAP2 pins. C_{EXT} is specified in *Table 15*.



1. Legend: ESR is the equivalent series resistance.

Symbol Parameter		Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 μF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

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Typical and maximum current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz and 3 wait states from 90 to 120 MHz).
- When the peripherals are enabled HCLK is the system clock, f_{PCLK1} = f_{HCLK}/4, and f_{PCLK2} = f_{HCLK}/2, except is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 19. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM ⁽¹⁾

Symbol	Baramatar	Conditions		Тур	Ма	Max ⁽²⁾	
Symbol	Farameter	Conditions	HCLK	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	Onit
			120 MHz	49	63	72	
			90 MHz	38	51	61	
			60 MHz	26	39	49	
		(3)	30 MHz	14	27	37	
		External clock ⁽³⁾ , all peripherals enabled ⁽⁴⁾	25 MHz	11	24	34	
			16 MHz ⁽⁵⁾	8	21	30	
			8 MHz	5	17	27	mA
			4 MHz	3	16	26	
1	Supply current		2 MHz	2	15	25	
'DD	in Run mode		120 MHz	21	34	44	
			90 MHz	17	30	40	
			60 MHz	12	25	35	
		(3)	30 MHz	7	20	30	
		External clock ⁽³⁾ , all peripherals disabled	25 MHz	5	18	28	
		F F	16 MHz ⁽⁵⁾	4.0	17.0	27.0	
			8 MHz	2.5	15.5	25.5	
			4 MHz	2.0	14.7	24.8	
			2 MHz	1.6	14.5	24.6	

1. Code and data processing running from SRAM1 using boot pins.

2. Guaranteed by characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.

3. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.

4. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

5. In this case HCLK = system clock/2.





Figure 23. Typical current consumption vs. temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals ON









Figure 25. Typical current consumption vs. temperature in Sleep mode, peripherals ON

Figure 26. Typical current consumption vs. temperature in Sleep mode, peripherals OFF







Figure 28. High-speed external clock source AC timing diagram

Figure 29. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).



Symbol	Parameter		Conditions	Min	Тур	Мах	Unit
R _{PU}	Weak pull-up equivalent	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	
	resistor	PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	kO
Weak pull-down R _{PD} equivalent resistor ⁽⁷⁾	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	K22	
	TESISION	PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
C _{IO} ⁽⁸⁾	I/O pin capacitan	ice	-	-	5	-	pF

Table 45. I/O static characteristics (continued)

1. Guaranteed by design, not tested in production.

2. Guaranteed by tests in production.

3. With a minimum of 200 mV.

- 4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to Table 44: I/O current injection susceptibility
- To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to Table 44: I/O current injection susceptibility
- 6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
- 7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
- 8. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 36*.



6.3.18 TIM timer characteristics

The parameters given in *Table 49* and *Table 50* are guaranteed by design.

Refer to Section 6.3.16: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Symbol	Parameter	Conditions	Min	Мах	Unit
		AHB/APB1	1	-	t _{TIMxCLK}
t _{res(TIM)}	Timer resolution time	from 1, f _{TIMxCLK} = 60 MHz	16.7	-	ns
		AHB/APB1	1	-	t _{TIMxCLK}
		f _{TIMxCLK} = 30 MHz	33.3	-	ns
f	Timer external clock		0	f _{TIMxCLK} /2	MHz
'EXT	frequency on CH1 to CH4		0	30	MHz
Res _{TIM}	Timer resolution		-	16/32	bit
	16-bit counter clock period		1	65536	t _{TIMxCLK}
toouwrep	selected	f _{TIMxCLK} = 60 MHz APB1= 30 MHz	0.0167	1092	μs
COUNTER	32-bit counter clock period		1	-	t _{TIMxCLK}
	selected		0.0167	71582788	μs
two count	Maximum possible count		-	65536 × 65536	t _{TIMxCLK}
WAX_COUNT			-	71.6	s

Table 49. Characteristics of	of TIMx connected to the APB1 dom	ain ⁽¹⁾
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1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.



Symbol	Parameter	Standard mode I ² C ⁽¹⁾⁽²⁾		Fast mode I ² C ⁽¹⁾⁽²⁾		Unit	
		Min	Max	Min	Max		
t _{w(SCLL)}	SCL clock low time	4.7	-	1.3	- µs		
t _{w(SCLH)}	SCL clock high time	4.0	-	0.6			
t _{su(SDA)}	SDA setup time	250	-	100	-		
t _{h(SDA)}	SDA data hold time	-	3450 ⁽³⁾	-	900 ⁽³⁾		
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rise time	-	1000	-	300 ns		
t _{f(SDA)} t _{f(SCL)}	SDA and SCL fall time	-	300	-	300	00	
t _{h(STA)}	Start condition hold time	4.0	-	0.6	-		
t _{su(STA)}	Repeated Start condition setup time	4.7	-	0.6	- µs		
t _{su(STO)}	Stop condition setup time	4.0	-	0.6	-	μs	
t _{w(STO:STA)}	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs	
Cb	Capacitive load for each bus line	-	400	-	400	pF	
t _{SP}	Pulse width of the spikes that are suppressed by the analog filter	0	50 ⁽⁴⁾	0	50	ns	

Table 51. I²C characteristics

1. Guaranteed by design, not tested in production.

f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.

3. The maximum Data hold time has only to be met if the interface does not stretch the low period of the SCL signal.

4. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$.







Figure 63. PC Card/CompactFlash controller waveforms for common memory read access

1. FSMC_NCE4_2 remains high (inactive during 8-bit access.







Symbol	millimeters			inches ⁽¹⁾			
	Min	Тур	Мах	Min	Тур	Мах	
С	0.090	-	0.200	0.0035	-	0.0079	
D	-	12.000	-	-	0.4724	-	
D1	-	10.000	-	-	0.3937	-	
D3	-	7.500	-	-	0.2953	-	
E	-	12.000	-	-	0.4724	-	
E1	-	10.000	-	-	0.3937	-	
E3	-	7.500	-	-	0.2953	-	
е	-	0.500	-	-	0.0197	-	
К	0°	3.5°	7°	0°	3.5°	7°	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295	
L1	-	1.000	-	-	0.0394	-	
ссс	-	-	0.080	-	-	0.0031	

Table 86. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flatpackage mechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.





1. Dimensions are expressed in millimeters.



Device marking



Figure 87. UFBGA176+25 marking (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

