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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f217iet6

1 Introduction

This datasheet provides the description of the STM32F215xx and STM32F217xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, refer to *Section 2.1: Full compatibility throughout the family*.

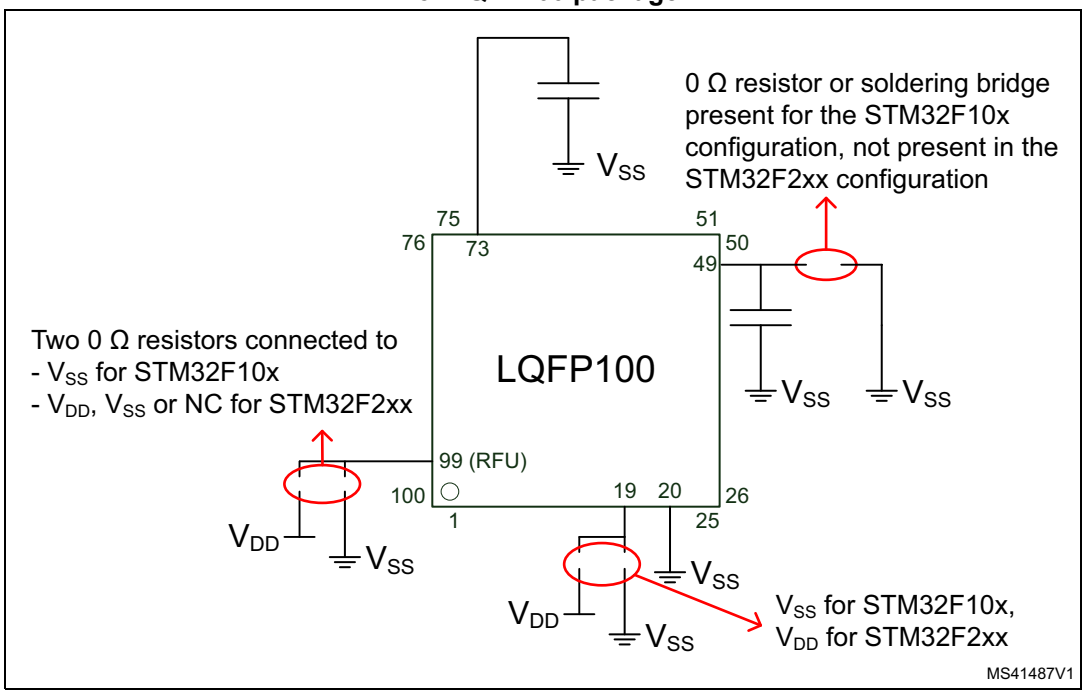
The STM32F215xx and STM32F217xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F21x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

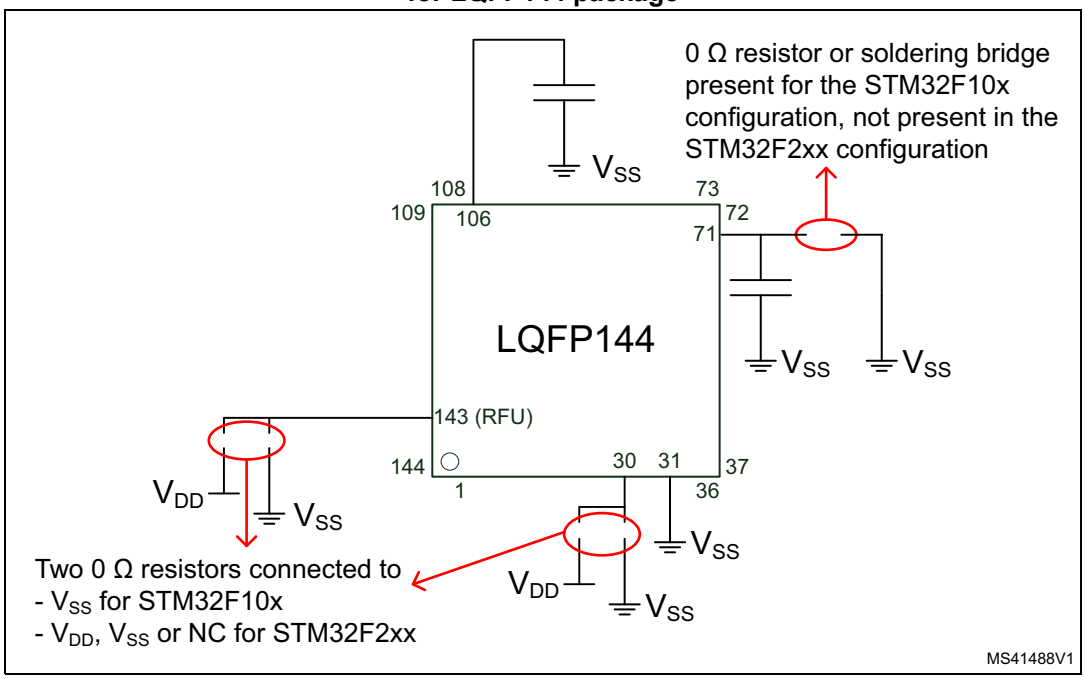
For information on the Cortex®-M3 core refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

Figure 2. Compatible board design between STM32F10x and STM32F2xx for LQFP100 package



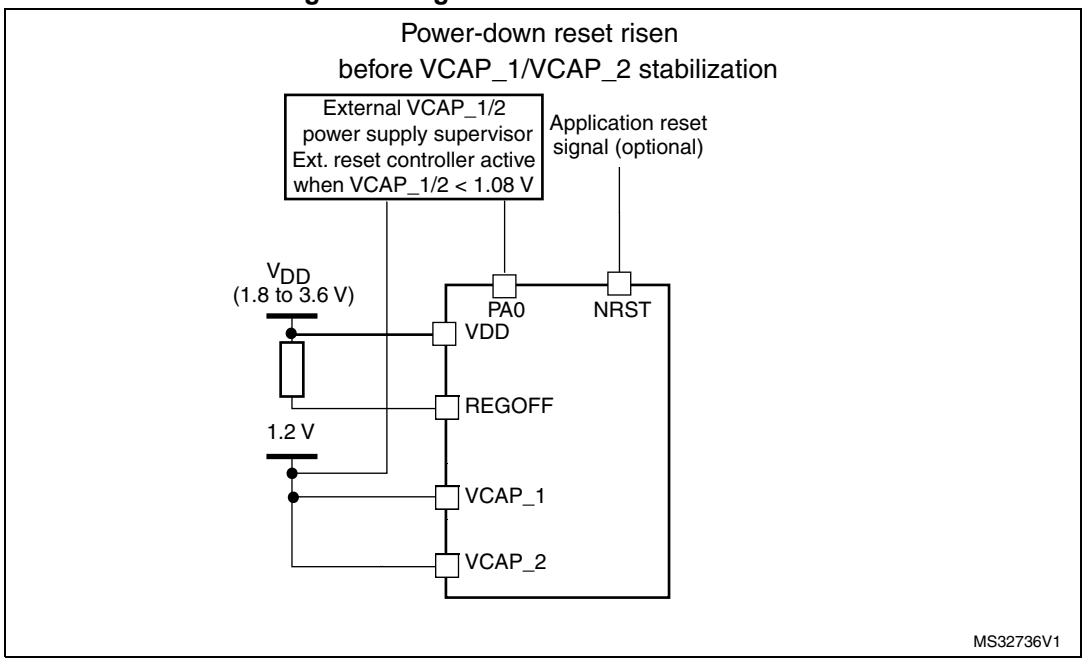
1. RFU = reserved for future use.

Figure 3. Compatible board design between STM32F10x and STM32F2xx for LQFP144 package



1. RFU = reserved for future use.

Figure 6. Regulator OFF/internal reset ON



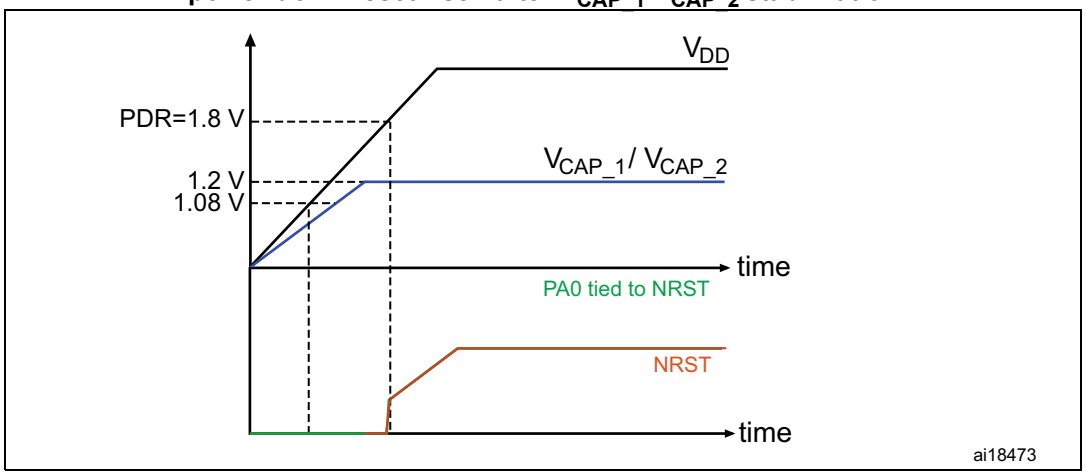
The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see *Figure 7*).
- Otherwise, If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is slower than the time for V_{DD} to reach 1.8 V, then PA0 should be asserted low externally (see *Figure 8*).
- If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

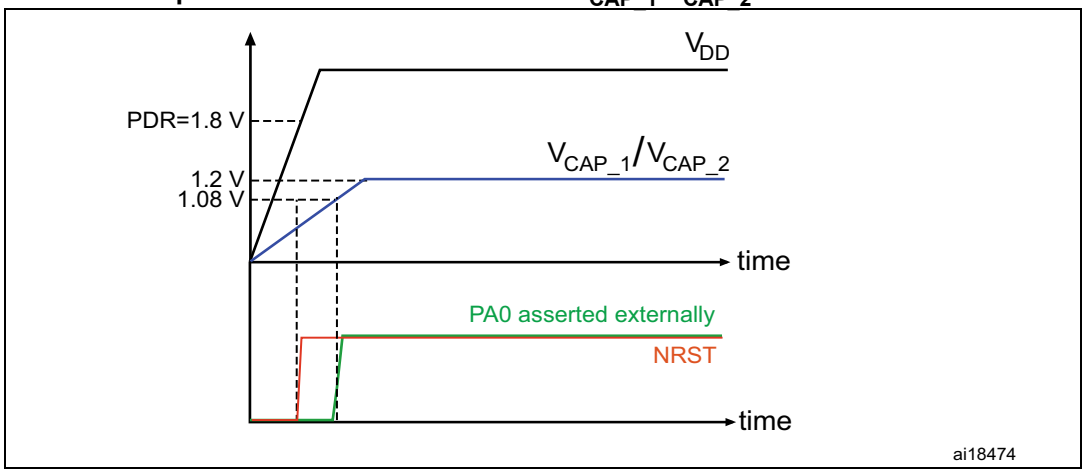
An external power supply supervisor should monitor both the external 1.2 V and the external V_{DD} supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.

Figure 7. Startup in regulator OFF: slow V_{DD} slope, power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid both whatever the internal reset mode (ON or OFF).

Figure 8. Startup in regulator OFF: fast V_{DD} slope, power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 3. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON/internal reset ON	Regulator ON/internal reset OFF	Regulator OFF/internal reset ON
LQFP64 LQFP100 LQFP144 LQFP176	Yes	No	No
UFBGA176	Yes REGOFF set to V_{SS}	No	Yes REGOFF set to V_{DD}

and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from the Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped when the device enters the Stop or Standby mode.

3.19 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery or an external supercapacitor.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

3.20 Timers and watchdogs

The STM32F21x devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock	Max timer clock
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	60 MHz	120 MHz

CAN is used). The 256 bytes of SRAM which are allocated for each CAN are not shared with any other peripheral.

3.28 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Internal FS OTG PHY support

3.29 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F21x devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 1024× 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.30 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 kHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

3.31 Digital camera interface (DCMI)

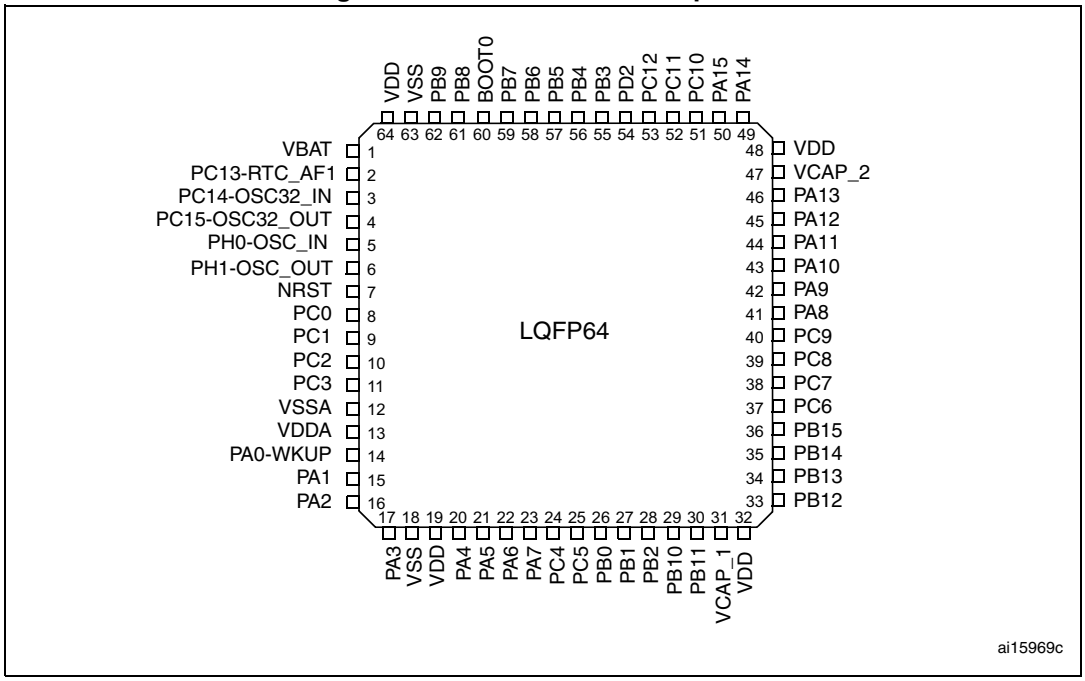
The camera interface is not available in STM32F215xx devices.

STM32F217xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain up to 27 Mbyte/s at 27 MHz or 48 Mbyte/s at 48 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw Bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

4 Pinouts and pin description

Figure 9. STM32F21x LQFP64 pinout



1. The above figure shows the package top view.

Table 7. STM32F21x pin and ball definitions (continued)

Pins					Pin name (function after reset)[1]	Pin type	I / O structure	Note	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	LQFP176	UFBGA176						
-	57	79	98	N15	PD10	I/O	FT	-	FSMC_D15, USART3_CK, EVENTOUT	-
-	58	80	99	N14	PD11	I/O	FT	-	FSMC_A16,USART3_CTS, EVENTOUT	-
-	59	81	100	N13	PD12	I/O	FT	-	FSMC_A17,TIM4_CH1, USART3_RTS, EVENTOUT	-
-	60	82	101	M15	PD13	I/O	FT	-	FSMC_A18,TIM4_CH2, EVENTOUT	-
-	-	83	102	-	V_{SS}	S		-	-	-
-	-	84	103	J13	V_{DD}	S		-	-	-
-	61	85	104	M14	PD14	I/O	FT	-	FSMC_D0,TIM4_CH3, EVENTOUT	-
-	62	86	105	L14	PD15	I/O	FT	-	FSMC_D1,TIM4_CH4, EVENTOUT	-
-	-	87	106	L15	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	88	107	K15	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	89	108	K14	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	90	109	K13	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	91	110	J15	PG6	I/O	FT	-	FSMC_INT2, EVENTOUT	-
-	-	92	111	J14	PG7	I/O	FT	-	FSMC_INT3,USART6_CK, EVENTOUT	-
-	-	93	112	H14	PG8	I/O	FT	-	USART6_RTS, ETH_PPS_OUT, EVENTOUT	-
-	-	94	113	G12	V_{SS}	S	-	-	-	-
-	-	95	114	H13	V_{DD}	S	-	-	-	-
37	63	96	115	H15	PC6	I/O	FT	-	I2S2_MCK, TIM8_CH1,SDIO_D6, USART6_TX, DCMI_D0,TIM3_CH1, EVENTOUT	-

Table 9. Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port A	PA0-WKUP	-	TIM2_CH1_ETR	TIM 5_CH1	TIM8_ETR	-	-		USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-		USART2_RTS	UART4_RX	-	-	ETH_MII _RX_CLK ETH_RMII _REF_CLK	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-		USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-		USART2_RX	-	-	OTG_HS_ULPI_D0	ETH _MII_COL	-	-	-	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-		-	OTG_HS_SOF	DCMI_HSYNC	-	EVENTOUT
	PA5	-	TIM2_CH1_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_C K	-	-	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCK	-	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII _RX_DV ETH_RMII _CRS_DV	-	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	-	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-		-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM 2_CH1 TIM 2_ETR	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	-	-	-	-	-	-	-	-	EVENTOUT

Table 29. HSE 4-26 MHz oscillator characteristics(1) (2)

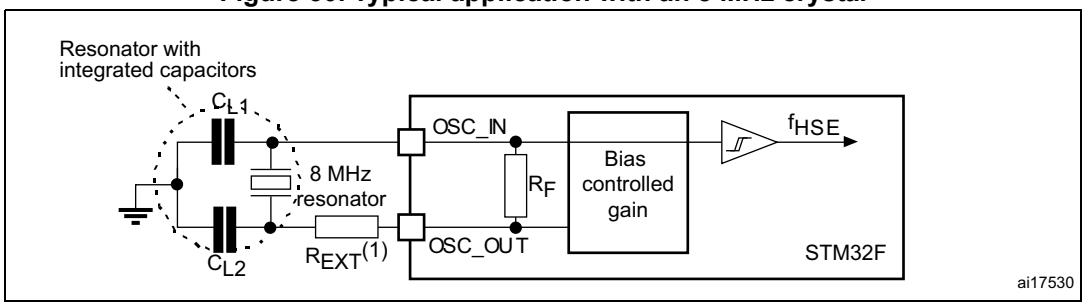
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	26	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	V_{DD}=3.3 V, ESR= 30 Ω, C_L=5 pF@25 MHz	-	449	-	µA
		V_{DD}=3.3 V, ESR= 30 Ω, C_L=10 pF@25 MHz	-	532	-	
g_m	Oscillator transconductance	Startup	5	-	-	mA/V
$t_{SU(HSE}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results, not tested in production.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 30*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 30. Typical application with an 8 MHz crystal

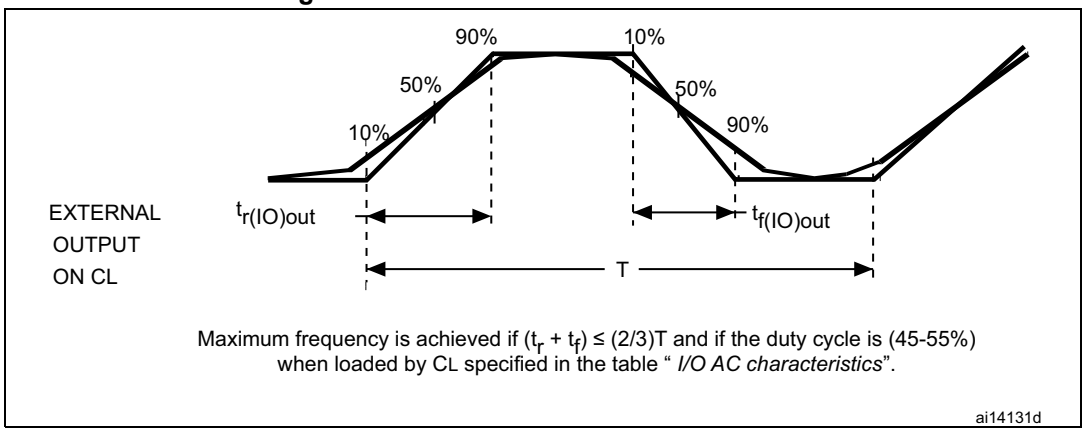


1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 30*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Figure 37. I/O AC characteristics definition



6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 48*).

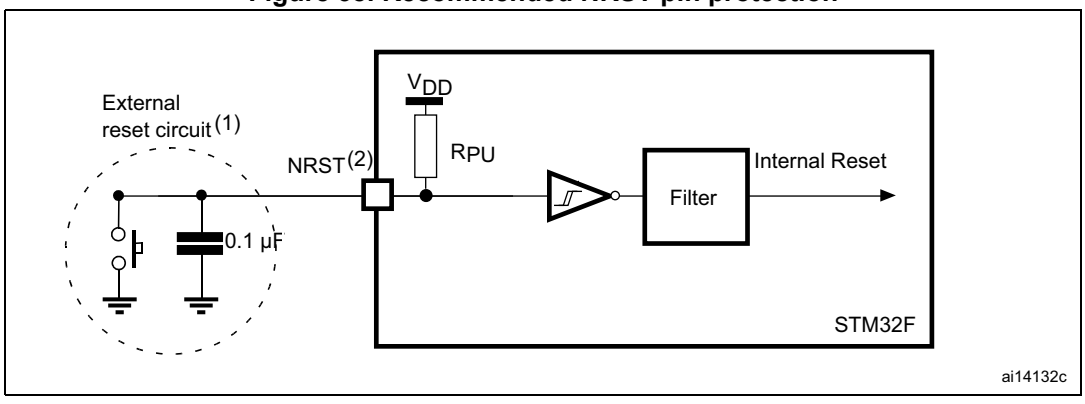
Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

Table 48. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

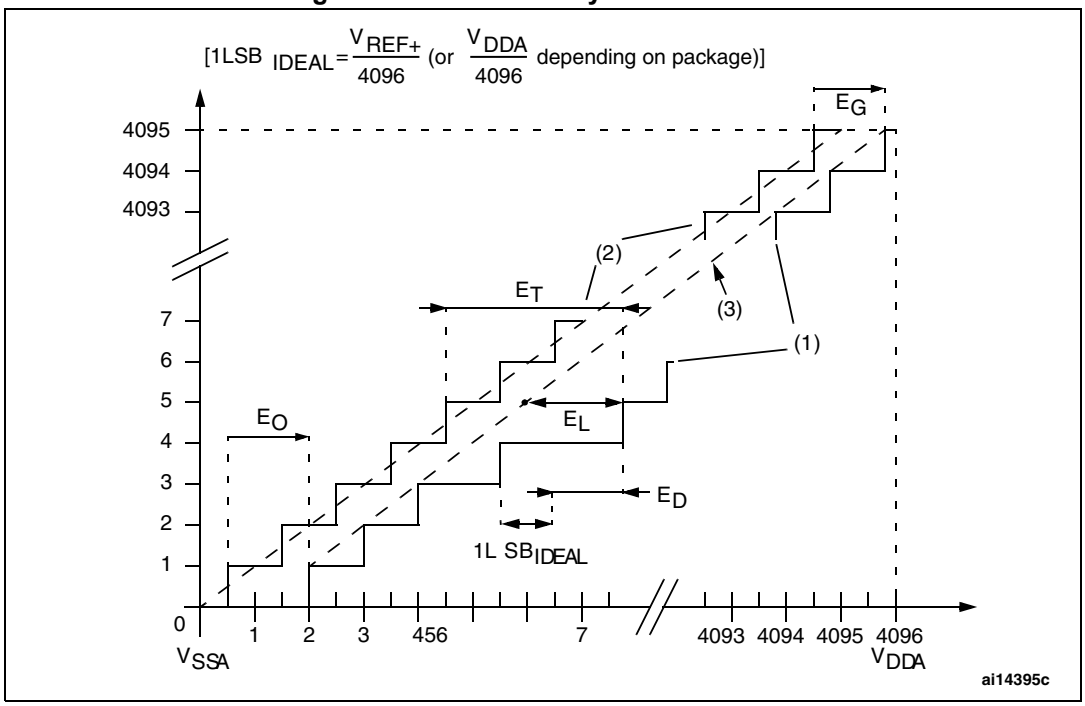
1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design, not tested in production.

Figure 38. Recommended NRST pin protection



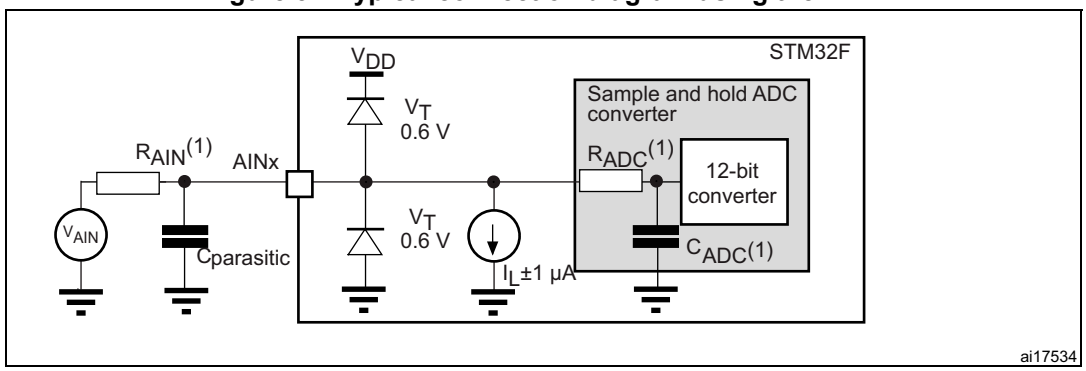
1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 48*. Otherwise the reset is not taken into account by the device.

Figure 50. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 51. Typical connection diagram using the ADC



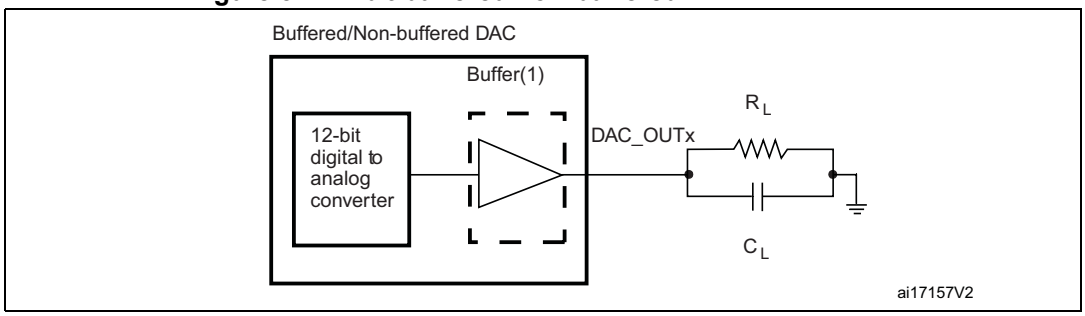
1. Refer to *Table 65* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Table 67. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Update rate(1)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
3. Guaranteed by characterization results, not tested in production.

Figure 54. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly, without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.22 Temperature sensor characteristics

Table 68. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

Table 75. Synchronous multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	5	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 60. Synchronous multiplexed PSRAM write timings

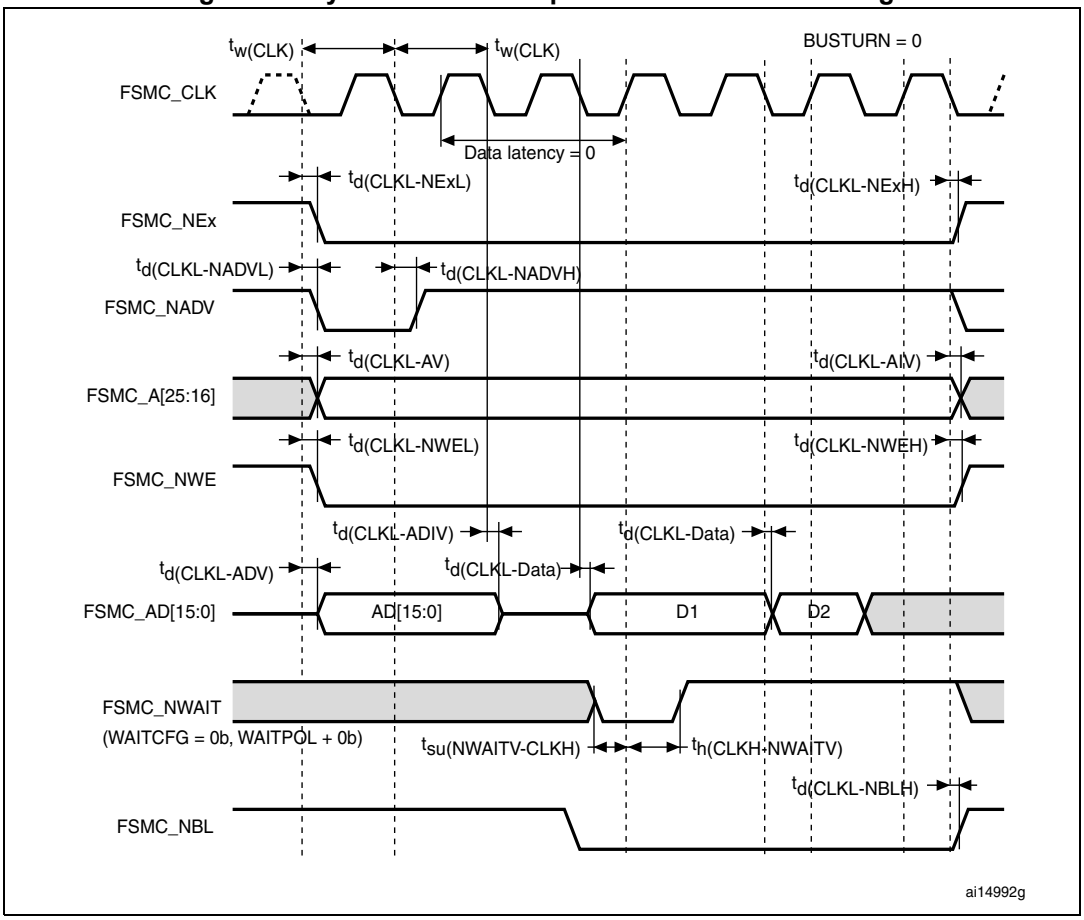


Table 76. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$- 1	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	3	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	7	-	ns

Table 80. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK}$ - 0.5	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK}$- 1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK}$- 3	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK}$+ 1.5	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}$	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK}$+ 1	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	$5T_{HCLK}$– 0.5	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK}$+ 1	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 69 through *Figure 72* represent synchronous waveforms, together with *Table 81* and *Table 82* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 94. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	4	Changed datasheet status to “Full Datasheet”. APB1 frequency changed form 36 MHz to 30 MHz. Introduced concept of SRAM1 and SRAM2. LQFP176 now in production. Removed WLCSP64+2 package. Updated *Figure 3: Compatible board design between STM32F10x and STM32F2xx for LQFP144 package* and *Figure 2: Compatible board design between STM32F10x and STM32F2xx for LQFP100 package*. Added camera interface for STM32F217Vx devices in *Table 2: STM32F215xx and STM32F217xx: features and peripheral counts*. Removed 16 MHz internal RC oscillator accuracy in *Section 3.12: Clocks and startup*. Updated *Section 3.16: Voltage regulator*. Modified I^2S sampling frequency range in *Section 3.12: Clocks and startup*, *Section 3.24: Inter-integrated sound (I2S)*, and *Section 3.30: Audio PLL (PLLI2S)*. Updated *Section 3.17: Real-time clock (RTC), backup SRAM and backup registers* and description of TIM2 and TIM5 in *Section 3.20.2: General-purpose timers (TIMx)*. Modified maximum baud rate (oversampling by 16) for USART1 in *Table 5: USART feature comparison*. Updated note related to RFU pin below *Figure 10: STM32F21x LQFP100 pinout*, *Figure 11: STM32F21x LQFP144 pinout*, *Figure 12: STM32F21x LQFP176 pinout*, *Figure 13: STM32F21x UFBGA176 ballout*, and *Table 7: STM32F21x pin and ball definitions*. Added RTC_50Hz as PB15 alternate function, and TT (3.6 V tolerant I/O) in *Table 7: STM32F21x pin and ball definitions* and *Table 9: Alternate function mapping*. PA15 added in *Table 7: STM32F21x pin and ball definitions*. In *Table 7: STM32F21x pin and ball definitions*, changed I2S2_CK and I2S3_CK to I2S2_SCK and I2S3_SCK, respectively. Removed ETH _RMII_TX_CLK for PC3/AF11 in *Table 9: Alternate function mapping*. Updated *Table 10: Voltage characteristics* and *Table 11: Current characteristics*. T_{STG} updated to –65 to +150 in *Table 12: Thermal characteristics*. Added CEXT and ESR in *Table 13: General operating conditions* as well as *Section 6.3.2: VCAP1/VCAP2 external capacitor*. Modified *Note 3* in *Table 14: Limitations depending on the operating power supply range*. Updated *Table 16: Operating conditions at power-up / power-down (regulator ON)*, and *Table 17: Operating conditions at power-up / power-down (regulator OFF)*. Updated notes below and added OSC_OUT pin in *Figure 15: Pin loading conditions*. and *Figure 16: Pin input voltage*. Updated V_{PVD}, V_{BOR1}, V_{BOR2}, V_{BOR3}, $T_{RSTTEMPO}$ typical value, and I_{RUSH}, added E_{RUSH} and *Note 2* in *Table 18: Embedded reset and power control block characteristics*.

Table 94. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	4 (continued)	Updated $t_{res(TIM)}$ in *Table 49: Characteristics of TIMx connected to the APB1 domain*. Modified $t_{res(TIM)}$ and f_{EXT} *Table 50: Characteristics of TIMx connected to the APB2 domain*. Changed $t_{w(SCKH)}$ to $t_{w(SCLH)}$, $t_{w(SCKL)}$ to $t_{w(SCLL)}$, $t_{r(SCK)}$ to $t_{r(SCL)}$, and $t_{f(SCK)}$ to $t_{f(SCL)}$ in *Table 51: I2C characteristics* and *Figure 39: I2C bus AC waveforms and measurement circuit*. Added *Table 56: USB OTG FS DC electrical characteristics* and updated *Table 57: USB OTG FS electrical characteristics*. Updated V_{DD} minimum value in *Table 61: Ethernet DC electrical characteristics*. Updated *Table 65: ADC characteristics* and R_{AIN} equation. Updated R_{AIN} equation. Updated *Table 67: DAC characteristics*. Updated t_{START} in *Table 68: Temperature sensor characteristics*. Updated *Table 70: Embedded internal reference voltage*. Modified FSMC_NOE waveform in *Figure 55: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms*. Shifted end of FSMC_NEx/NADV/addresses/NWE/NOE/NWAIT of a half FSMC_CLK period, changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, and $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and updated data latency from 1 to 0 in *Figure 59: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 60: Synchronous multiplexed PSRAM write timings*, *Figure 61: Synchronous non-multiplexed NOR/PSRAM read timings*, and *Figure 62: Synchronous non-multiplexed PSRAM write timings*, Changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and modified $t_{w(CLK)}$ minimum value in *Table 75*, *Table 76*, *Table 77*, and *Table 78*. Updated R typical value in *Table 69: VBAT monitoring characteristics*.Updated note 2 in *Table 71*, *Table 72*, *Table 73*, *Table 74*, *Table 75*, *Table 76*, *Table 77*, and *Table 78*. Modified $t_{h(NIOWR-D)}$ in *Figure 68: PC Card/CompactFlash controller waveforms for I/O space write access*. Modified FSMC_NCEx signal in *Figure 69: NAND controller waveforms for read access*, *Figure 70: NAND controller waveforms for write access*, *Figure 71: NAND controller waveforms for common memory read access*, and *Figure 72: NAND controller waveforms for common memory write access*. Specified Full speed (FS) mode for *Figure 86: USB OTG HS peripheral-only connection in FS mode* and *Figure 87: USB OTG HS host-only connection in FS mode*.

Table 94. Document revision history (continued)

Date	Revision	Changes
20-Dec-2011	6 (continued)	Appendix *A.2: USB OTG full speed (FS) interface solutions*: updated *Figure 85: USB OTG FS (full speed) host-only connection* and added *Note 2*, updated *Figure 86: OTG FS (full speed) connection dual-role with internal PHY* and added *Note 3* and *Note 4*, modified *Figure 87: OTG HS (high speed) device connection, host and dual-role in high-speed mode with external PHY* and added *Note 2*. Appendix *A.3: USB OTG high speed (HS) interface solutions*: removed figures *USB OTG HS device-only connection in FS mode* and *USB OTG HS host-only connection in FS mode*, updated *Figure 87: OTG HS (high speed) device connection, host and dual-role in high-speed mode with external PHY*. Added Appendix *A.4: Ethernet interface solutions*. Updated disclaimer on last page.