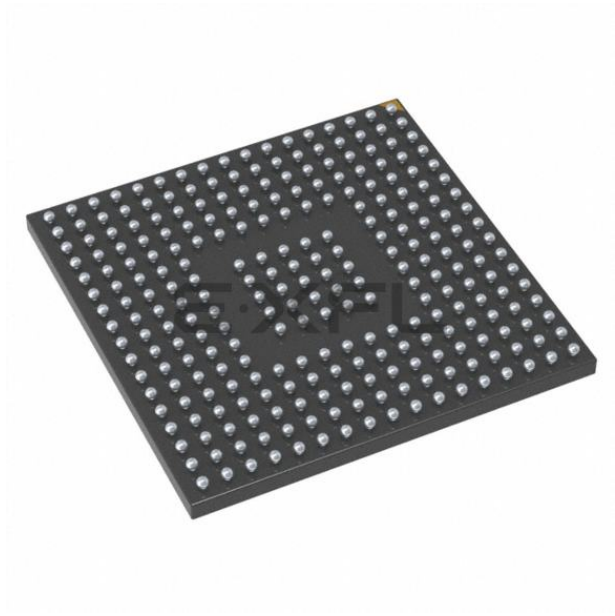

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f217igh6

Table 1. Device summary

Reference	Part numbers
STM32F215xx	STM32F215RG, STM32F215VG, STM32F215ZG STM32F215RE, STM32F215VE, STM32F215ZE
STM32F217xx	STM32F217VG, STM32F217IG, STM32F217ZG STM32F217VE, STM32F217IE, STM32F217ZE

List of figures

1 Introduction

This datasheet provides the description of the STM32F215xx and STM32F217xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F215xx and STM32F217xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F21x devices throughout the document.

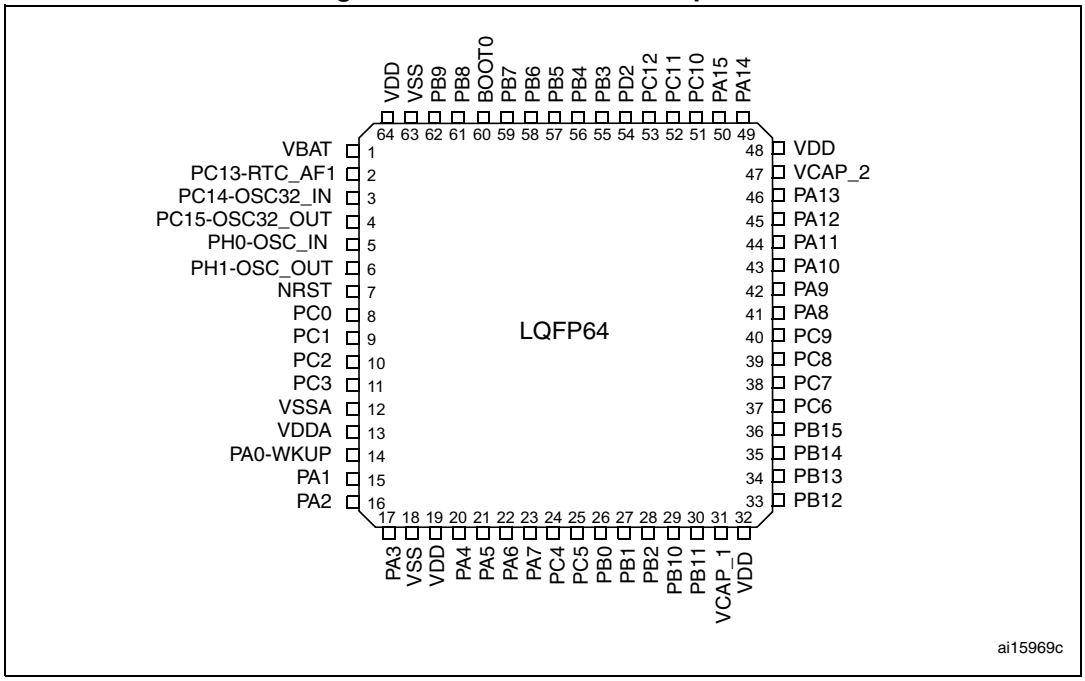
For information on programming, erasing and protection of the internal Flash memory, refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

4 Pinouts and pin description

Figure 9. STM32F21x LQFP64 pinout



1. The above figure shows the package top view.

Table 7. STM32F21x pin and ball definitions (continued)

Pins					Pin name (function after reset)(1)	Pin type	I / O structure	Note	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	LQFP176	UFBGA176						
38	64	97	116	G15	PC7	I/O	FT	-	I2S3_MCK, TIM8_CH2,SDIO_D7, USART6_RX, DCMI_D1,TIM3_CH2, EVENTOUT	-
39	65	98	117	G14	PC8	I/O	FT	-	TIM8_CH3,SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT	-
40	66	99	118	F14	PC9	I/O	FT	-	I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4,SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT	-
41	67	100	119	F15	PA8	I/O	FT	-	MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-
42	68	101	120	E15	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
43	69	102	121	D15	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, OTG_FS_ID,DCMI_D1, EVENTOUT	-
44	70	103	122	C15	PA11	I/O	FT	-	USART1_CTS, CAN1_RX, TIM1_CH4, OTG_FS_DM, EVENTOUT	-
45	71	104	123	B15	PA12	I/O	FT	-	USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT	-
46	72	105	124	A15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
47	73	106	125	F13	V_{CAP_2}	S	-	-	-	-
-	74	107	126	F12	V_{SS}	S	-	-	-	-
48	75	108	127	G13	V_{DD}	S	-	-	-	-
-	-	-	128	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	129	E13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.8 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 15*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 16*.

Figure 15. Pin loading conditions

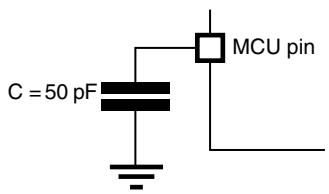


Figure 16. Pin input voltage

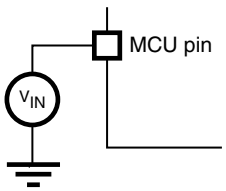


Table 13. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD}(2)	1.8	3.6	
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	
V_{IN}	Input voltage on RST and FT pins	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	5.5	
		1.7 V ≤ V_{DD} ≤ 2 V	–0.3	5.2	
	Input voltage on TTa pins	-	–0.3	V_{DD}+0.3	
	Input voltage on BOOT0 pin	-	0	9	
V_{CAP1}	Internal core voltage to be supplied externally in REGOFF mode	-	1.1	1.3	
V_{CAP2}					
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LQFP64	-	444	mW
		LQFP100	-	434	
		LQFP144	-	500	
		LQFP176	-	526	
		UFBGA176	-	513	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(4)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(4)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 65: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
4. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 14. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency ($f_{Flashmax}$)	Number of wait states at maximum CPU frequency (f_{CPUmax}= 120 MHz)(1)	I/O operation	FSMC_CLK frequency for synchronous accesses	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V	Conversion time up to 1 Msps	16 MHz with no Flash memory wait state	7(2)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1 Msps	18 MHz with no Flash memory wait state	6(2)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2 Msps	24 MHz with no Flash memory wait state	4(2)	– Degraded speed performance – I/O compensation works	Up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(3)	Conversion time up to 2 Msps	30 MHz with no Flash memory wait state	3(2)	– Full-speed operation – I/O compensation works	– Up to 60 MHz when V_{DD} = 3.0 to 3.6 V – Up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 19*).
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

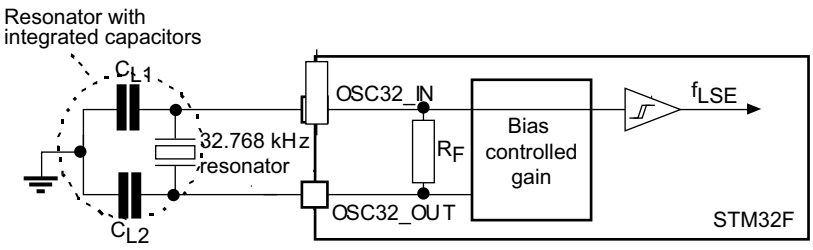
Table 30. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	-	-	-	1	µA
g_m	Oscillator Transconductance	-	2.8	-	-	µA/V
$t_{SU(LSE)}$ (2)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 31. Typical application with a 32.768 kHz crystal



6.3.9 Internal clock source characteristics

The parameters given in *Table 31* and *Table 32* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

High-speed internal (HSI) RC oscillator

Table 31. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user-trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	– 8	-	4.5	%
		T_A = –10 to 85 °C(3)	– 4	-	4	%
		T_A = 25 °C(4)	– 1	-	1	%
$t_{su(HSI)}$ (2)	HSI oscillator startup time	-	-	2.2	4.0	µs
$I_{DD(HSI)}$ (2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Table 38. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 39. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 43. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 44*.

Table 44. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	–0	NA	mA
	Injected current on NRST pin	–0	NA	
	Injected current on TTa pins: PA4 and PA5	–0	+5	
	Injected current on all FT pins	–5	NA	

1. NA stands for “not applicable”.

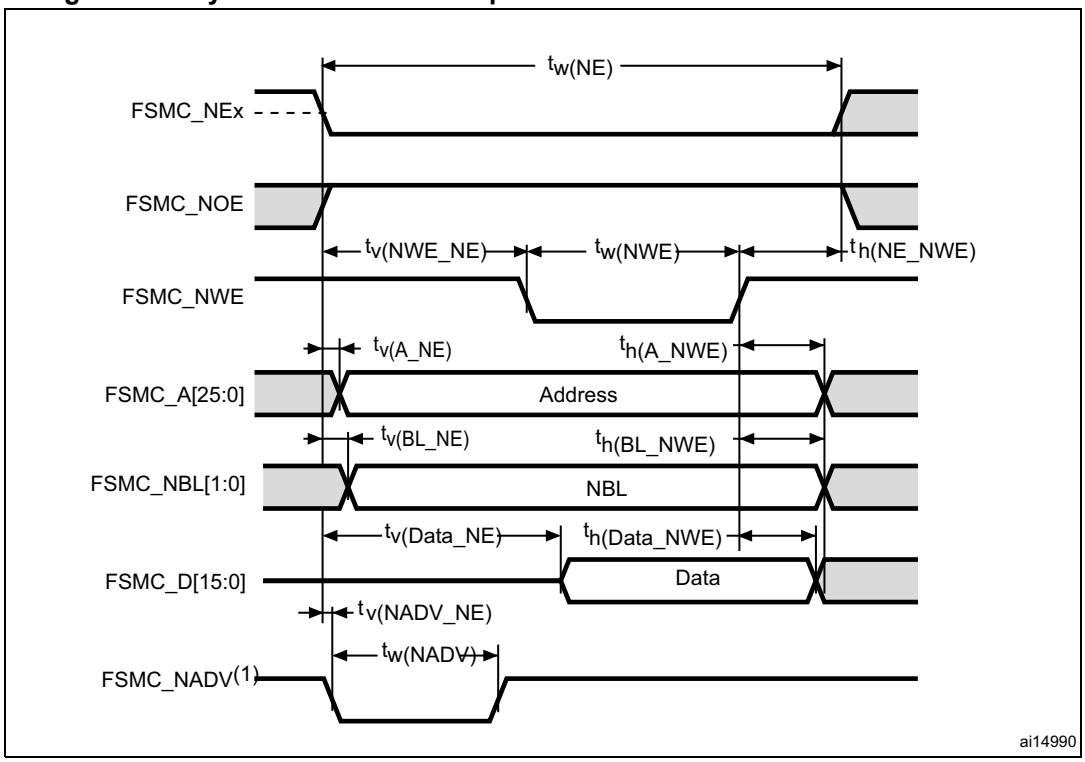
Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Table 54. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master, 16-bit data, audio frequency = 48 kHz, main clock disabled	1.23	1.24	MHz
		Slave	0	$64F_S$ (1)	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 50 pF	-	(2)	ns
$t_{v(WS)}$ (3)	WS valid time	Master	0.3	-	
$t_{h(WS)}$ (3)	WS hold time	Master	0	-	
$t_{su(WS)}$ (3)	WS setup time	Slave	3	-	
$t_{h(WS)}$ (3)	WS hold time	Slave	0	-	
$t_{w(CKH)}$ (3) $t_{w(CKL)}$ (3)	CK high and low time	Master f_{PCLK}= 30 MHz	396	-	
$t_{su(SD\_MR)}$ (3) $t_{su(SD\_SR)}$ (3)	Data input setup time	Master receiver Slave receiver	45 0	-	
$t_{h(SD\_MR)}$ (3)(4) $t_{h(SD\_SR)}$ (3)(4)	Data input hold time	Master receiver: f_{PCLK}= 30 MHz, Slave receiver: f_{PCLK}= 30 MHz	13 0	-	
$t_{v(SD\_ST)}$ (3)(4)	Data output valid time	Slave transmitter (after enable edge)	-	30	
$t_{h(SD\_ST)}$ (3)	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD\_MT)}$ (3)(4)	Data output valid time	Master transmitter (after enable edge)	-	6	
$t_{h(SD\_MT)}$ (3)	Data output hold time	Master transmitter (after enable edge)	0	-	

1. F_S is the sampling frequency. Refer to the I2S section of the STM32F20xxx/21xxx reference manual for more details. f_{CK} values reflect only the digital peripheral behavior which leads to a minimum of (I2SDIV/(2*I2SDIV+ODD), a maximum of (I2SDIV+ODD)/(2*I2SDIV+ODD) and F_S maximum values for each mode/condition.
2. Refer to *Table 47: I/O AC characteristics*.
3. Guaranteed by design, not tested in production.
4. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PLCLK} =125 ns.

Figure 56. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

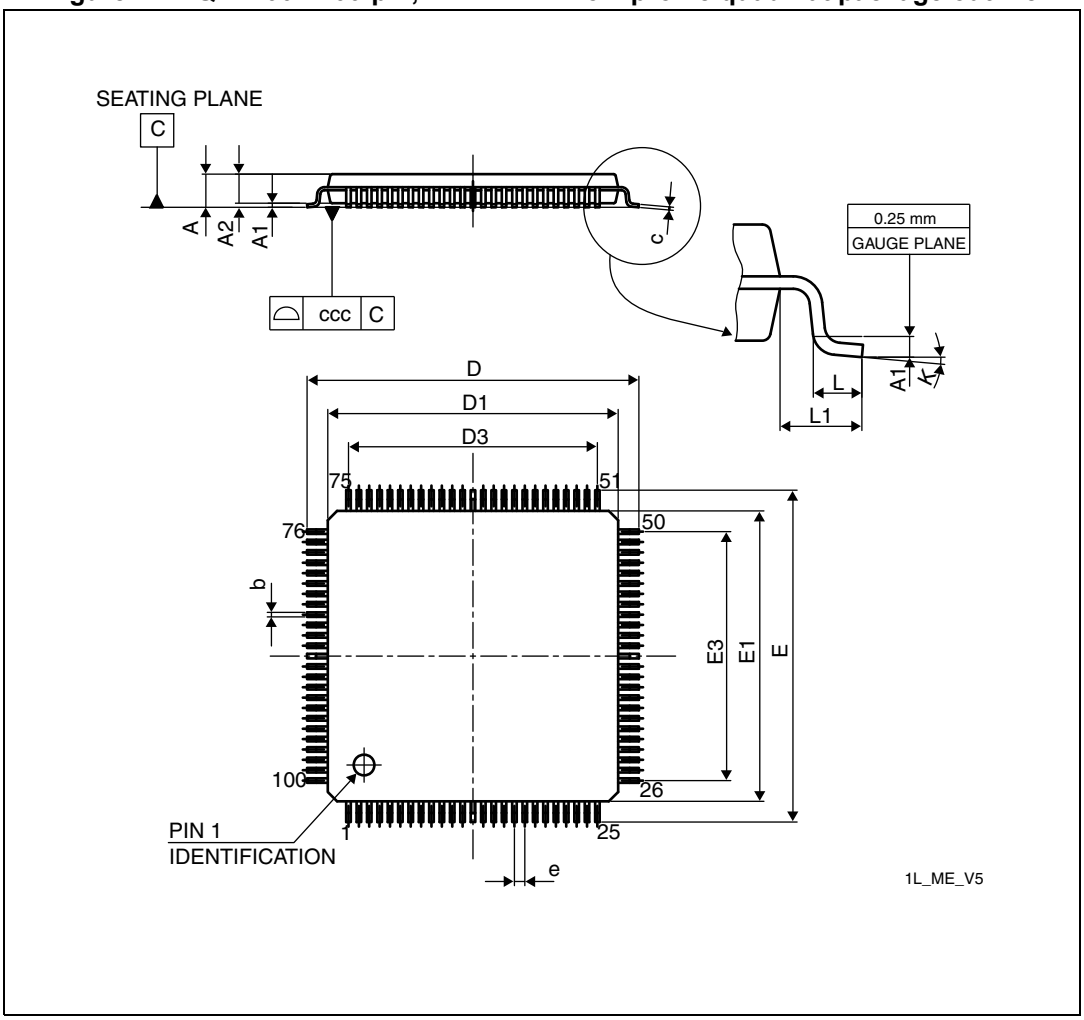
Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+4$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK}-0.5$	$T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$T_{HCLK}-0.5$	$T_{HCLK}+3$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK}-3$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK}-1$	-	ns
$t_{v(Data\_NE)}$	Data to FSMC_NEx low to Data valid	-	$T_{HCLK}+5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK}+1.5$	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

7.2 LQFP100 package information

Figure 77. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



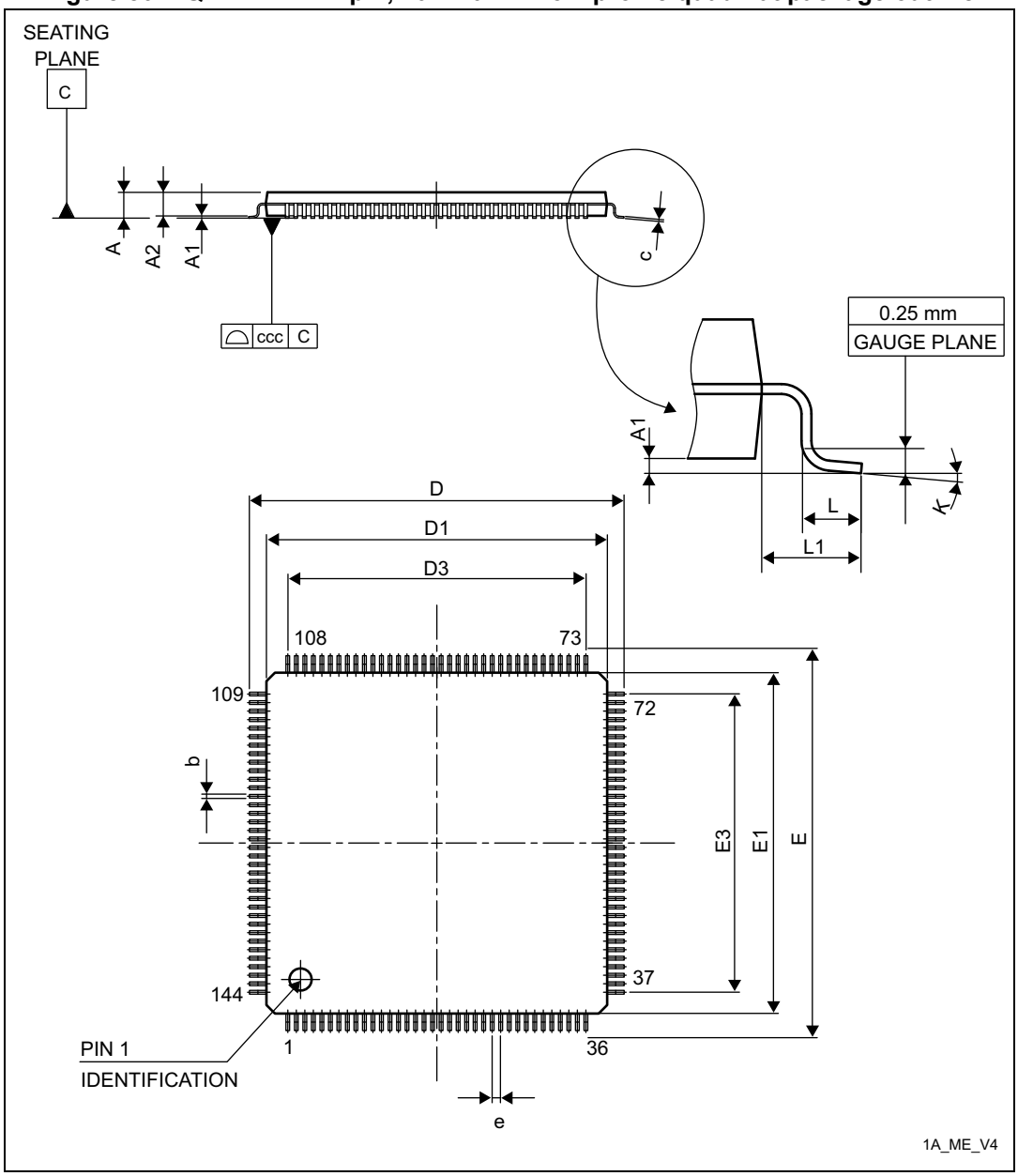
1. Drawing is not to scale.

Table 87. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591

7.3 LQFP144 package information

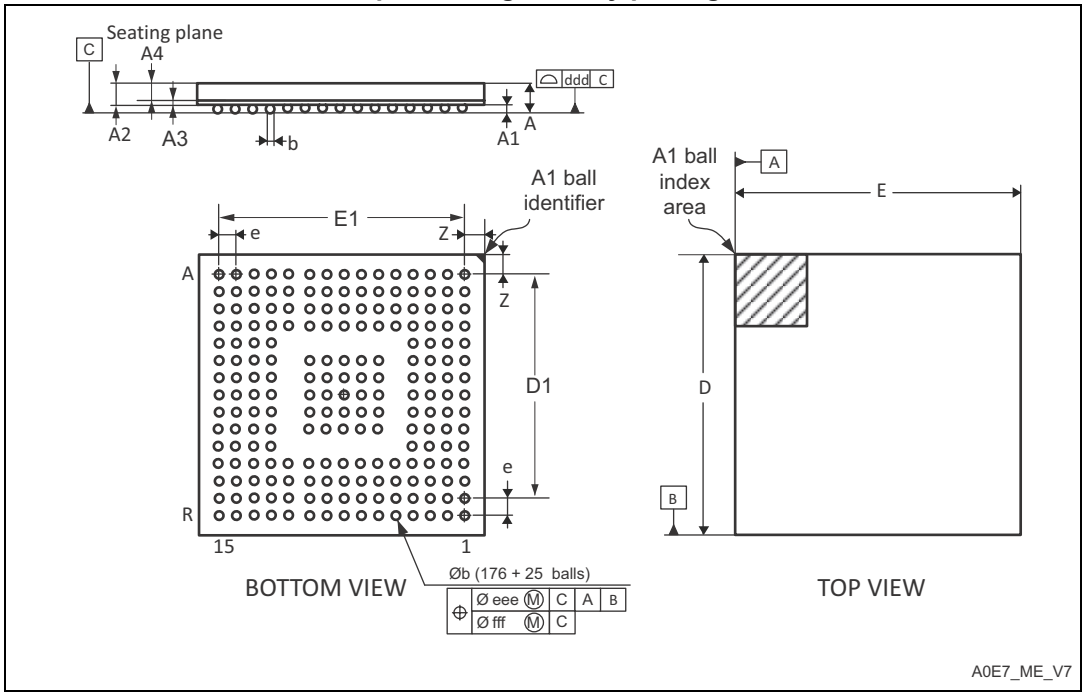
Figure 80. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.5 UFBGA176+25 package information

Figure 85. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 90. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

7.6 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 92. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 94. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	4 (continued)	Updated *Typical and maximum current consumption* conditions, as well as *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)* and *Table 19: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*. Added *Figure 21*, *Figure 22*, *Figure 23*, and *Figure 24*. Updated *Table 21: Typical and maximum current consumption in Sleep mode*, and added *Figure 25* and *Figure 26*. Updated *Table 23: Typical and maximum current consumptions in Standby mode* and *Table 24: Typical and maximum current consumptions in VBAT mode*. Updated *Table 22: Typical and maximum current consumptions in Stop mode*. Added *Figure 27: Typical current consumption vs. temperature in Stop mode*. Updated *Table 23: Typical and maximum current consumptions in Standby mode* and *Table 24: Typical and maximum current consumptions in VBAT mode*. Updated *On-chip peripheral current consumption* conditions and *Table 25: Peripheral current consumption*. Updated $t_{WUSTDBY}$ and t_{WUSTOP}, and added *Note 3* in *Table 26: Low-power mode wakeup timings*. Maximum f_{HSE_ext} and minimum $t_{w(HSE)}$ values updated in *Table 27: High-speed external user clock characteristics*. Updated C and g_m in *Table 29: HSE 4-26 MHz oscillator characteristics*. Updated R_F, I_2, g_m, and $t_{su(LSE)}$ in *Table 30: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Added *Note 3* and updated ACC_{HSI}, $IDD_{(HSI)}$ and $t_{su(HSI)}$ in *Table 31: HSI oscillator characteristics*. Added *Figure 32: ACCHSI versus temperature* Updated f_{LSI}, $t_{su(LSI)}$ and $IDD_{(LSI)}$ in *Table 32: LSI oscillator characteristics*. *Table 33: Main PLL characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLL)}$ and $IDD_{A(PLL)}$, added *Note 2* for f_{PLL_IN} minimum and maximum values. *Table 34: PLLI2S (audio PLL) characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLLI2S)}$ and $IDD_{A(PLLI2S)}$, added *Note 2* for f_{PLLI2S_IN} minimum and maximum values. Added *Note 1* in *Table 35: SSCG parameters constraint*. Updated *Table 36: Flash memory characteristics*. Modified *Table 37: Flash memory programming* and added *Note 1* for t_{prog}. Updated t_{prog} and added *Note 1* in *Table 38: Flash memory programming with VPP*. Modified *Figure 38: Recommended NRST pin protection*. Updated *Table 41: EMI characteristics* and EMI monitoring conditions in *Section : Electromagnetic Interference (EMI)*. Added *Note 2* related to $V_{ESD(HBM)}$ in *Table 42: ESD absolute maximum ratings*. Added *Section 6.3.15: I/O current injection characteristics*. Updated *Table 45: I/O static characteristics*. Modified maximum frequency values and conditions in *Table 47: I/O AC characteristics*.

Table 94. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	8	Removed Figure 4. Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package. Updated number of AHB buses in *Section 2: Description* and *Section 3.12: Clocks and startup*. Updated *Note 2* below *Figure 4: STM32F21x block diagram*. Changed System memory to System memory + OTP in *Figure 14: Memory map*. Added *Note 1* below *Table 15: VCAP1/VCAP2 operating conditions*. Updated V_{DDA} and V_{REF+} decoupling capacitor in *Figure 17: Power supply scheme* and updated *Note 3*. Changed simplex mode into half-duplex mode in *Section 3.24: Inter-integrated sound (I2S)*. Replaced DAC1_OUT and DAC2_OUT by DAC_OUT1 and DAC_OUT2, respectively. Changed TIM2_CH1/TIM2_ETR into TIM2_CH1_ETR for PA0 and PA5 in *Table 9: Alternate function mapping*. Updated note applying to I_{DD} (external clock and all peripheral disabled) in *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*. Updated *Note 3* below *Table 21: Typical and maximum current consumption in Sleep mode*. Removed f_{HSE_ext} typical value in *Table 27: High-speed external user clock characteristics*. Updated master I2S clock jitter conditions and values in *Table 34: PLLI2S (audio PLL) characteristics*. Updated equations in *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Swapped TTL and CMOS port conditions for V_{OL} and V_{OH} in *Table 46: Output voltage characteristics*. Updated $V_{IL(NRST)}$ and $V_{IH(NRST)}$ in *Table 48: NRST pin characteristics*. Updated *Table 53: SPI characteristics* and *Table 54: I2S characteristics*.Removed note 1 related to measurement points below *Figure 41: SPI timing diagram - slave mode and CPHA = 1*, *Figure 42: SPI timing diagram - master mode*, and *Figure 43: I2S slave timing diagram (Philips protocol)(1)*. Updated t_{HC} in *Table 60: ULPI timing*. Updated *Figure 47: Ethernet SMI timing diagram*, *Table 62: Dynamics characteristics: Ethernet MAC signals for SMI* and *Table 63: Dynamics characteristics: Ethernet MAC signals for RMII*. Update f_{TRIG} in *Table 65: ADC characteristics*. Updated I_{DDA} description in *Table 67: DAC characteristics*. Updated note below *Figure 52: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 53: Power supply and reference decoupling (VREF+ connected to VDDA)*. Replaced $t_{d(CLKL-NOEL)}$ by $t_{d(CLKH-NOEL)}$ in *Table 75: Synchronous multiplexed NOR/PSRAM read timings*, *Table 77: Synchronous non-multiplexed NOR/PSRAM read timings*, *Figure 59: Synchronous multiplexed NOR/PSRAM read timings* and *Figure 61: Synchronous non-multiplexed NOR/PSRAM read timings*.

Table 94. Document revision history (continued)

Date	Revision	Changes
04-Nov-2013	9 (continued)	Updated *Figure 75: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 86: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Updated *Figure 77: LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 80: LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline*, *Figure 83: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Updated *Figure 85: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline* and *Figure 85: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*. Removed Appendix A Application block diagrams.
27-Oct-2014	10	Updated V_{BAT} voltage range in *Figure 17: Power supply scheme*. Added caution note in *Section 6.1.6: Power supply scheme*. Updated V_{IN} in *Table 13: General operating conditions*. Removed note 1 in *Table 22: Typical and maximum current consumptions in Stop mode*. Updated *Table 44: I/O current injection susceptibility*, *Section 6.3.16: I/O port characteristics* and *Section 6.3.17: NRST pin characteristics*. Removed note 3 in *Table 68: Temperature sensor characteristics*. Added *Figure 79: LQFP100 marking (package top view)* and *Figure 82: LQFP144 marking (package top view)*.
23-Feb-2016	11	Updated *Section 1: Introduction*. Updated *Table 31: HSI oscillator characteristics* and its footnotes. Updated *Figure 34: PLL output clock waveforms in center spread mode*, *Figure 35: PLL output clock waveforms in down spread mode*, *Figure 52: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 53: Power supply and reference decoupling (VREF+ connected to VDDA)*. Updated *Section 7: Package information* and its subsections.
07-Jul-2016	12	Updated *Features* and *Section 2: Description*. Updated figures *1*, *2* and *3* in *Section 2.1: Full compatibility throughout the family*. Updated *Device marking* and *Figure 79* in *Section 7.2: LQFP100 package information*. Updated *Device marking* and *Figure 82* in *Section 7.3: LQFP144 package information*. Updated *Section 7.5: UFBGA176+25 package information* with introduction of *Device marking* and *Figure 87*. Updated *Table 93: Ordering information scheme*.
16-Aug-2016	13	Updated *Figure 52: Power supply and reference decoupling (VREF+ not connected to VDDA)*. Updated title of *Section 8: Ordering information*.