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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 140 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 132K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-LQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f217igt7 |

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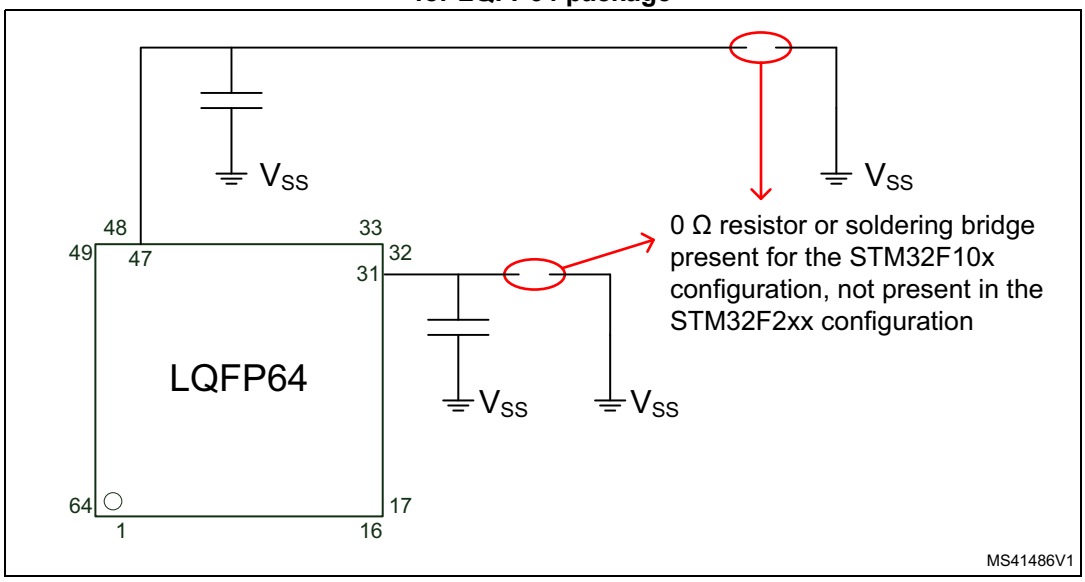
## 2.1 Full compatibility throughout the family

The STM32F215xx and STM32F217xx constitute the STM32F21x family whose members are fully pin-to-pin, software and feature compatible, allowing the user to try different memory densities and peripherals for a greater degree of freedom during the development cycle.

The STM32F215xx and STM32F217xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F215xx and STM32F217xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F21x family remains simple as only a few pins are impacted.

*Figure 1*, *Figure 2* and *Figure 3* provide compatible board designs between the STM32F21x and the STM32F10xxx family.

**Figure 1. Compatible board design between STM32F10x and STM32F2xx for LQFP64 package**



# 3 Functional overview

## 3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM® core, the STM32F21x family is compatible with all ARM® tools and software.

*Figure 4* shows the general block diagram of the STM32F21x family.

## 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M3 processors. It balances the inherent performance advantage of the ARM® Cortex®-M3 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher operating frequencies.

To release the processor full 150 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache which increases program execution speed from the 128-bit Flash memory. Based on CoreMark® benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz.

## 3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from the Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped when the device enters the Stop or Standby mode.*

## 3.19 $V_{BAT}$ operation

The $V_{BAT}$ pin allows to power the device $V_{BAT}$ domain from an external battery or an external supercapacitor.

$V_{BAT}$ operation is activated when $V_{DD}$ is not present.

The VBAT pin supplies the RTC, the backup registers and the backup SRAM.

*Note: When the microcontroller is supplied from $V_{BAT}$, external interrupts and RTC alarm/events do not exit it from $V_{BAT}$ operation.*

## 3.20 Timers and watchdogs

The STM32F21x devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

*Table 4* compares the features of the advanced-control, general-purpose and basic timers.

**Table 4. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary output | Max interface clock | Max timer clock |
|---|---|---|---|---|---|---|---|---|---|
| Advanced-control | TIM1, TIM8 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | Yes | 60 MHz | 120 MHz |

Table 4. Timer feature comparison (continued)

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary output | Max interface clock | Max timer clock |
|---|---|---|---|---|---|---|---|---|---|
| General purpose | TIM2, TIM5 | 32-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 30 MHz | 60 MHz |
| | TIM3, TIM4 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 30 MHz | 60 MHz |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 30 MHz | 60 MHz |
| General purpose | TIM9 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 60 MHz | 120 MHz |
| | TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 60 MHz | 120 MHz |
| | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 30 MHz | 60 MHz |
| | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 30 MHz | 60 MHz |

### 3.20.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

Table 7. STM32F21x pin and ball definitions (continued)

| Pins | | | | | Pin name (function after reset)[1] | Pin type | I / O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 13 | 22 | 33 | 39 | R1 | $V_{DDA}$ | S | - | - | - | - |
| 14 | 23 | 34 | 40 | N3 | PA0/WKUP (PA0) | I/O | FT | (4)(5) | USART2_CTS, UART4_TX, ETH_MII_CRS, TIM2_CH1_ETR, TIM5_CH1, TIM8_ETR, EVENTOUT | ADC123_IN0, WKUP |
| 15 | 24 | 35 | 41 | N2 | PA1 | I/O | FT | (4) | USART2_RTS, UART4_RX, ETH_RMII_REF_CLK, ETH_MII_RX_CLK, TIM5_CH2, TIM2_CH2, EVENTOUT | ADC123_IN1 |
| 16 | 25 | 36 | 42 | P2 | PA2 | I/O | FT | (4) | USART2_TX,TIM5_CH3, TIM9_CH1, TIM2_CH3, ETH_MDIO, EVENTOUT | ADC123_IN2 |
| - | - | - | 43 | F4 | PH2 | I/O | FT | - | ETH_MII_CRS, EVENTOUT | - |
| - | - | - | 44 | G4 | PH3 | I/O | FT | - | ETH_MII_COL, EVENTOUT | - |
| - | - | - | 45 | H4 | PH4 | I/O | FT | - | I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT | - |
| - | - | - | 46 | J4 | PH5 | I/O | FT | - | I2C2_SDA, EVENTOUT | - |
| 17 | 26 | 37 | 47 | R2 | PA3 | I/O | FT | (4) | USART2_RX, TIM5_CH4, TIM9_CH2, TIM2_CH4, OTG_HS_ULPI_D0, ETH_MII_COL, EVENTOUT | ADC123_IN3 |
| 18 | 27 | 38 | 48 | - | $V_{SS}$ | S | - | - | - | - |
| | | | | L4 | REGOFF | I/O | - | - | - | - |
| 19 | 28 | 39 | 49 | K4 | $V_{DD}$ | S | - | - | - | - |
| 20 | 29 | 40 | 50 | N4 | PA4 | I/O | TTa | (4) | SPI1_NSS, SPI3_NSS, USART2_CK, DCMI_HSYNC, OTG_HS_SOF, I2S3_WS, EVENTOUT | ADC12_IN4, DAC_OUT1 |
| 21 | 30 | 41 | 51 | P4 | PA5 | I/O | TTa | (4) | SPI1_SCK, OTG_HS_ULPI_CK, TIM2_CH1_ETR, TIM8_CH1N, EVENTOUT | ADC12_IN5 /DAC_OUT2 |

Table 7. STM32F21x pin and ball definitions (continued)

| Pins | | | | | Pin name (function after reset)[1] | Pin type | I / O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | 39 | 59 | 69 | P8 | PE8 | I/O | FT | - | FSMC_D5, TIM1_CH1N, EVENTOUT | - |
| - | 40 | 60 | 70 | P9 | PE9 | I/O | FT | - | FSMC_D6, TIM1_CH1, EVENTOUT | - |
| - | - | 61 | 71 | M9 | $V_{SS}$ | S | - | - | - | - |
| - | - | 62 | 72 | N9 | $V_{DD}$ | S | - | - | - | - |
| - | 41 | 63 | 73 | R9 | PE10 | I/O | FT | - | FSMC_D7, TIM1_CH2N, EVENTOUT | - |
| - | 42 | 64 | 74 | P10 | PE11 | I/O | FT | - | FSMC_D8,TIM1_CH2, EVENTOUT | - |
| - | 43 | 65 | 75 | R10 | PE12 | I/O | FT | - | FSMC_D9,TIM1_CH3N, EVENTOUT | - |
| - | 44 | 66 | 76 | N11 | PE13 | I/O | FT | - | FSMC_D10,TIM1_CH3, EVENTOUT | - |
| - | 45 | 67 | 77 | P11 | PE14 | I/O | FT | - | FSMC_D11,TIM1_CH4, EVENTOUT | - |
| - | 46 | 68 | 78 | R11 | PE15 | I/O | FT | - | FSMC_D12,TIM1_BKIN, EVENTOUT | - |
| 29 | 47 | 69 | 79 | R12 | PB10 | I/O | FT | - | SPI2_SCK, I2S2_SCK, I2C2_SCL, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, TIM2_CH3, EVENTOUT | - |
| 30 | 48 | 70 | 80 | R13 | PB11 | I/O | FT | - | I2C2_SDA,USART3_RX, OTG_HS_ULPI_D4, ETH_RMII_TX_EN, ETH_MII_TX_EN, TIM2_CH4, EVENTOUT | - |
| 31 | 49 | 71 | 81 | M10 | $V_{CAP\_1}$ | S | | - | - | - |
| 32 | 50 | 72 | 82 | N10 | $V_{DD}$ | S | | - | - | - |
| - | - | - | 83 | M11 | PH6 | I/O | FT | - | I2C2_SMBA, TIM12_CH1, ETH_MII_RXD2, EVENTOUT | - |
| - | - | - | 84 | N12 | PH7 | I/O | FT | - | I2C3_SCL, ETH_MII_RXD3, EVENTOUT | - |

Table 7. STM32F21x pin and ball definitions (continued)

| Pins | | | | | Pin name (function after reset)(1) | Pin type | I / O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 38 | 64 | 97 | 116 | G15 | PC7 | I/O | FT | - | I2S3_MCK, TIM8_CH2,SDIO_D7, USART6_RX, DCMI_D1,TIM3_CH2, EVENTOUT | - |
| 39 | 65 | 98 | 117 | G14 | PC8 | I/O | FT | - | TIM8_CH3,SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT | - |
| 40 | 66 | 99 | 118 | F14 | PC9 | I/O | FT | - | I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4,SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT | - |
| 41 | 67 | 100 | 119 | F15 | PA8 | I/O | FT | - | MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT | - |
| 42 | 68 | 101 | 120 | E15 | PA9 | I/O | FT | - | USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT | OTG_FS_ VBUS |
| 43 | 69 | 102 | 121 | D15 | PA10 | I/O | FT | - | USART1_RX, TIM1_CH3, OTG_FS_ID,DCMI_D1, EVENTOUT | - |
| 44 | 70 | 103 | 122 | C15 | PA11 | I/O | FT | - | USART1_CTS, CAN1_RX, TIM1_CH4, OTG_FS_DM, EVENTOUT | - |
| 45 | 71 | 104 | 123 | B15 | PA12 | I/O | FT | - | USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT | - |
| 46 | 72 | 105 | 124 | A15 | PA13 (JTMS-SWDIO) | I/O | FT | - | JTMS-SWDIO, EVENTOUT | - |
| 47 | 73 | 106 | 125 | F13 | $V_{CAP\_2}$ | S | - | - | - | - |
| - | 74 | 107 | 126 | F12 | $V_{SS}$ | S | - | - | - | - |
| 48 | 75 | 108 | 127 | G13 | $V_{DD}$ | S | - | - | - | - |
| - | - | - | 128 | E12 | PH13 | I/O | FT | - | TIM8_CH1N, CAN1_TX, EVENTOUT | - |
| - | - | - | 129 | E13 | PH14 | I/O | FT | - | TIM8_CH2N, DCMI_D4, EVENTOUT | - |

## Table 9. Alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_HS | DCMI | | |
| Port B | PB0 | - | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | - | - | - | - | - | - | OTG_HS_ULPI_D1 | ETH _MII_RXD2 | - | - | - | EVENTOUT |
| | PB1 | - | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | - | - | - | - | - | - | OTG_HS_ULPI_D2 | ETH _MII_RXD3 | - | - | - | EVENTOUT |
| | PB2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB3 | JTDO/ TRACESWO | TIM2_CH2 | - | - | - | SPI1_SCK | SPI3_SCK I2S3_SCK | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB4 | JTRST | - | TIM3_CH1 | - | - | SPI1_MISO | SPI3_MISO | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB5 | - | - | TIM3_CH2 | - | I2C1_SMBA | SPI1_MOSI | SPI3_MOSI I2S3_SD | - | - | CAN2_RX | OTG_HS_ULPI_D7 | ETH _PPS_OUT | - | DCMI_D10 | - | EVENTOUT |
| | PB6 | - | - | TIM4_CH1 | - | I2C1_SCL | - | - | USART1_TX | - | CAN2_TX | - | - | - | DCMI_D5 | - | EVENTOUT |
| | PB7 | - | - | TIM4_CH2 | - | I2C1_SDA | - | - | USART1_RX | - | - | - | - | FSMC_NL | DCMI_VSYNC | - | EVENTOUT |
| | PB8 | - | - | TIM4_CH3 | TIM10_CH1 | I2C1_SCL | - | - | - | - | CAN1_RX | - | ETH _MII_TXD3 | SDIO_D4 | DCMI_D6 | - | EVENTOUT |
| | PB9 | - | - | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | SPI2_NSS I2S2_WS | - | - | - | CAN1_TX | - | - | SDIO_D5 | DCMI_D7 | - | EVENTOUT |
| | PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | SPI2_SCK I2S2_SCK | - | USART3_TX | - | - | OTG_HS_ULPI_D3 | ETH_ MII_RX_ER | - | - | - | EVENTOUT |
| | PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | - | - | USART3_RX | - | - | OTG_HS_ULPI_D4 | ETH _MII_TX_EN ETH _RMII_TX_EN | - | - | - | EVENTOUT |
| | PB12 | - | TIM1_BKIN | - | - | I2C2_SMBA | SPI2_NSS I2S2_WS | - | USART3_CK | - | CAN2_RX | OTG_HS_ULPI_D5 | ETH _MII_TXD0 ETH _RMII_TXD0 | OTG_HS_ID | - | - | EVENTOUT |
| | PB13 | - | TIM1_CH1N | - | - | - | SPI2_SCK I2S2_SCK | - | USART3_CTS | - | CAN2_TX | OTG_HS_ULPI_D6 | ETH _MII_TXD1 ETH _RMII_TXD1 | - | - | - | EVENTOUT |
| | PB14 | - | TIM1_CH2N | - | TIM8_CH2N | - | SPI2_MISO | - | USART3_RTS | - | TIM12_CH1 | - | - | OTG_HS_DM | - | - | EVENTOUT |
| | PB15 | RTC_50Hz | TIM1_CH3N | - | TIM8_CH3N | - | SPI2_MOSI I2S2_SD | - | - | - | TIM12_CH2 | - | - | OTG_HS_DP | - | - | EVENTOUT |

**Table 20. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | Max(1) | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Run mode | External clock(2), all peripherals enabled(3) | 120 MHz | 61 | 81 | 93 | mA |
| | | | 90 MHz | 48 | 68 | 80 | |
| | | | 60 MHz | 33 | 53 | 65 | |
| | | | 30 MHz | 18 | 38 | 50 | |
| | | | 25 MHz | 14 | 34 | 46 | |
| | | | 16 MHz(4) | 10 | 30 | 42 | |
| | | | 8 MHz | 6 | 26 | 38 | |
| | | | 4 MHz | 4 | 24 | 36 | |
| | | | 2 MHz | 3 | 23 | 35 | |
| | | External clock(2), all peripherals disabled | 120 MHz | 33 | 54 | 66 | |
| | | | 90 MHz | 27 | 47 | 59 | |
| | | | 60 MHz | 19 | 39 | 51 | |
| | | | 30 MHz | 11 | 31 | 43 | |
| | | | 25 MHz | 8 | 28 | 41 | |
| | | | 16 MHz(4) | 6 | 26 | 38 | |
| | | | 8 MHz | 4 | 24 | 36 | |
| | | | 4 MHz | 3 | 23 | 35 | |
| | | | 2 MHz | 2 | 23 | 34 | |

1. Guaranteed by characterization results, tested in production at $V_{DD}$ max and $f_{HCLK}$ max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when $f_{HCLK}$ > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

**Table 21. Typical and maximum current consumption in Sleep mode**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | Max(1) | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(2), all peripherals enabled(3) | 120 MHz | 38 | 51 | 61 | mA |
| | | | 90 MHz | 30 | 43 | 53 | |
| | | | 60 MHz | 20 | 33 | 43 | |
| | | | 30 MHz | 11 | 25 | 35 | |
| | | | 25 MHz | 8 | 21 | 31 | |
| | | | 16 MHz | 6 | 19 | 29 | |
| | | | 8 MHz | 3.6 | 17.0 | 27.0 | |
| | | | 4 MHz | 2.4 | 15.4 | 25.3 | |
| | | | 2 MHz | 1.9 | 14.9 | 24.7 | |
| | | External clock(2), all peripherals disabled | 120 MHz | 8 | 21 | 31 | |
| | | | 90 MHz | 7 | 20 | 30 | |
| | | | 60 MHz | 5 | 18 | 28 | |
| | | | 30 MHz | 3.5 | 16.0 | 26.0 | |
| | | | 25 MHz | 2.5 | 16.0 | 25.0 | |
| | | | 16 MHz | 2.1 | 15.1 | 25.0 | |
| | | | 8 MHz | 1.7 | 15.0 | 25.0 | |
| | | | 4 MHz | 1.5 | 14.6 | 24.6 | |
| | | | 2 MHz | 1.4 | 14.2 | 24.3 | |

1. Guaranteed by characterization results, tested in production at $V_{DD}$ max and $f_{HCLK}$ max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when $f_{HCLK}$ > 25 MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

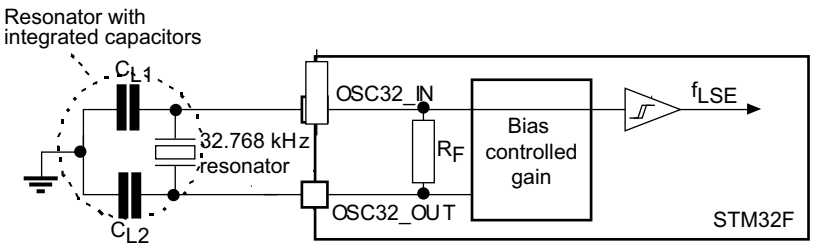
**Table 30. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | - | - | 18.4 | - | MΩ |
| $I_{DD}$ | LSE current consumption | - | - | - | 1 | µA |
| $g_m$ | Oscillator Transconductance | - | 2.8 | - | - | µA/V |
| $t_{SU(LSE)}$ (2) | startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Guaranteed by design, not tested in production.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

*Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 31. Typical application with a 32.768 kHz crystal**




## 6.3.9 Internal clock source characteristics

The parameters given in *Table 31* and *Table 32* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 13*.

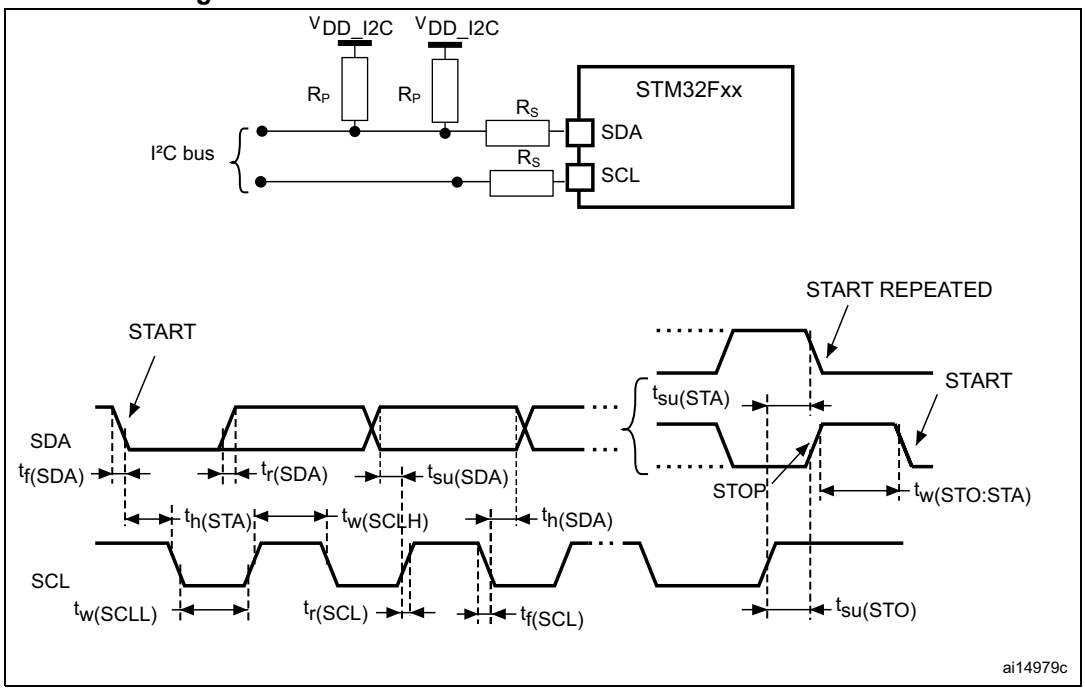
### High-speed internal (HSI) RC oscillator

**Table 31. HSI oscillator characteristics (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 16 | - | MHz |
| $ACC_{HSI}$ | HSI user-trimming step(2) | - | - | - | 1 | % |
| | Accuracy of the HSI oscillator | $T_A$ = –40 to 105 °C(3) | – 8 | - | 4.5 | % |
| | | $T_A$ = –10 to 85 °C(3) | – 4 | - | 4 | % |
| | | $T_A$ = 25 °C(4) | – 1 | - | 1 | % |
| $t_{su(HSI)}$ (2) | HSI oscillator startup time | - | - | 2.2 | 4.0 | µs |
| $I_{DD(HSI)}$ (2) | HSI oscillator power consumption | - | - | 60 | 80 | µA |

1. $V_{DD}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

**Figure 39. I²C bus AC waveforms and measurement circuit**




1. $R_S$= series protection resistor.
2. $R_P$ = external pull-up resistor.
3. $V_{DD\_I2C}$ is the I²C bus power supply.

**Table 52. SCL frequency ($f_{PCLK1}$= 30 MHz.,$V_{DD}$ = 3.3 V)(1)(2)**

| $f_{SCL}$ (kHz) | I2C_CCR value |
|---|---|
| | $R_P$ = 4.7 kΩ |
| 400 | 0x8019 |
| 300 | 0x8021 |
| 200 | 0x8032 |
| 100 | 0x0096 |
| 50 | 0x012C |
| 20 | 0x02EE |

1. $R_P$ = External pull-up resistance, $f_{SCL}$ = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

**Figure 40. SPI timing diagram - slave mode and CPHA = 0**

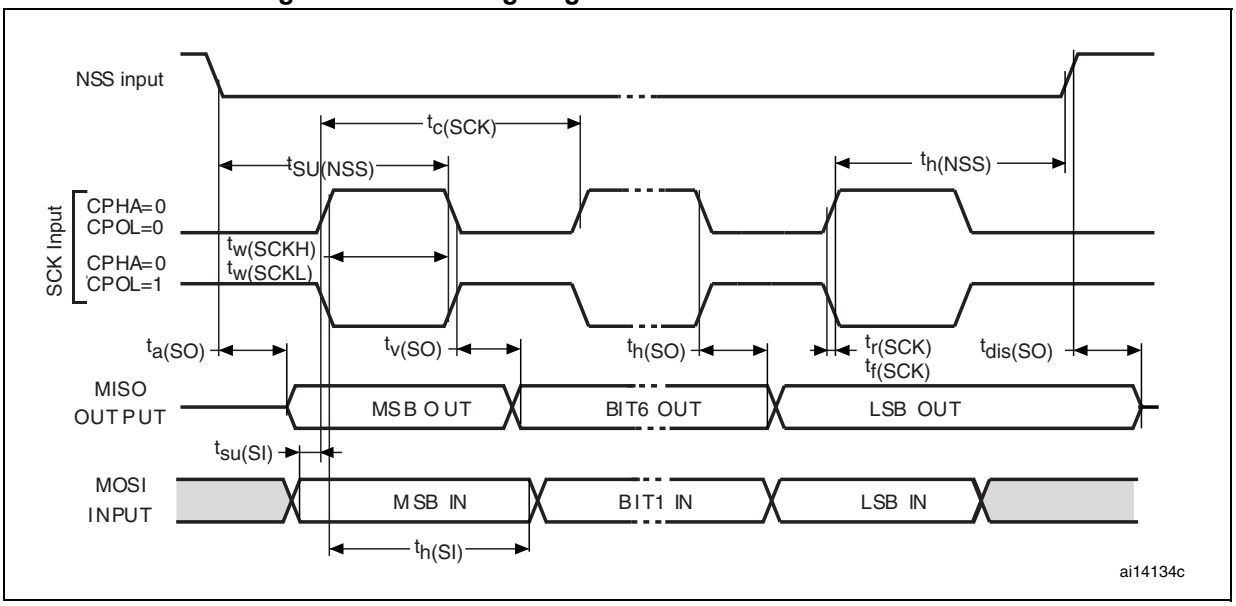



**Figure 41. SPI timing diagram - slave mode and CPHA = 1**

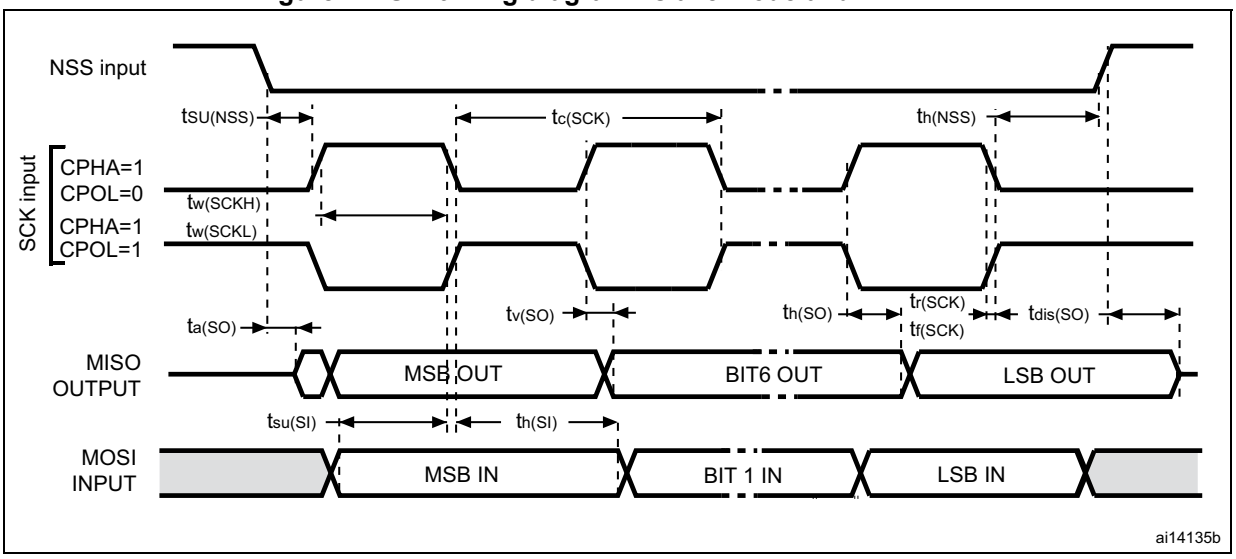


**Figure 45. USB OTG FS timings: definition of data signal rise and fall time**

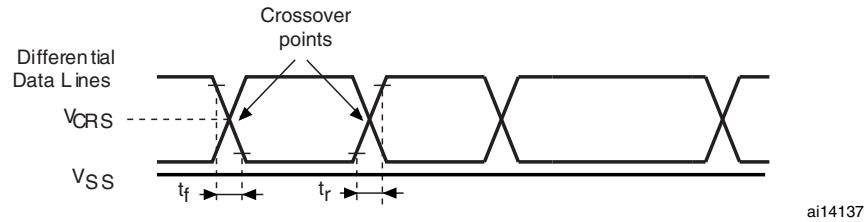



**Table 57. USB OTG FS electrical characteristics(1)**

| Driver characteristics | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | - | 1.3 | 2.0 | V |

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

## USB HS characteristics

*Table 58* shows the USB HS operating voltage.

**Table 58. USB HS DC electrical characteristics**

| Symbol | | Parameter | Min(1) | Max(1) | Unit |
|---|---|---|---|---|---|
| **Input level** | $V_{DD}$ | USB OTG HS operating voltage | 2.7 | 3.6 | V |

1. All the voltages are measured from the local ground potential.

**Table 59. Clock timing parameters**

| Parameter(1) | | Symbol | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency (first transition) | 8-bit ±10% | $F_{START\_8BIT}$ | 54 | 60 | 66 | MHz |
| Frequency (steady state) ±500 ppm | | $F_{STEADY}$ | 59.97 | 60 | 60.03 | MHz |
| Duty cycle (first transition) | 8-bit ±10% | $D_{START\_8BIT}$ | 40 | 50 | 60 | % |
| Duty cycle (steady state) ±500 ppm | | $D_{STEADY}$ | 49.975 | 50 | 50.025 | % |
| Time to reach the steady state frequency and duty cycle after the first transition | | $T_{STEADY}$ | - | - | 1.4 | ms |
| Clock startup time after the de-assertion of SuspendM | Peripheral | $T_{START\_DEV}$ | - | - | 5.6 | ms |
| | Host | $T_{START\_HOST}$ | - | - | - | |
| PHY preparation time after the first transition of the input clock | | $T_{PREP}$ | - | - | - | µs |

1. Guaranteed by design, not tested in production.

**Table 82. Switching characteristics for NAND Flash write cycles(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NWE)}$ | FSMC_NWE low width | $4T_{HCLK}$- 1 | $4T_{HCLK}$+ 3 | ns |
| $t_{v(NWE-D)}$ | FSMC_NWE low to FSMC_D[15-0] valid | - | 0 | ns |
| $t_{h(NWE-D)}$ | FSMC_NWE high to FSMC_D[15-0] invalid | $3T_{HCLK}$ | - | ns |
| $t_{d(D-NWE)}$ | FSMC_D[15-0] valid before FSMC_NWE high | $5T_{HCLK}$ | - | ns |
| $t_{d(ALE-NWE)}$ | FSMC_ALE valid before FSMC_NWE low | - | $3T_{HCLK}$+ 2 | ns |
| $t_{h(NWE-ALE)}$ | FSMC_NWE high to FSMC_ALE invalid | $3T_{HCLK}$- 2 | - | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results, not tested in production.

## 6.3.26 Camera interface (DCMI) timing specifications

**Table 83. DCMI characteristics**

| Symbol | Parameter | Conditions | Min | Max |
|---|---|---|---|---|
| - | Frequency ratio DCMI_PIXCLK/$f_{HCLK}$ | DCMI_PIXCLK= 48 MHz | - | 0.4 |

## 6.3.27 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 84* are derived from tests performed under ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 13*.

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

**Figure 73. SDIO high-speed mode**

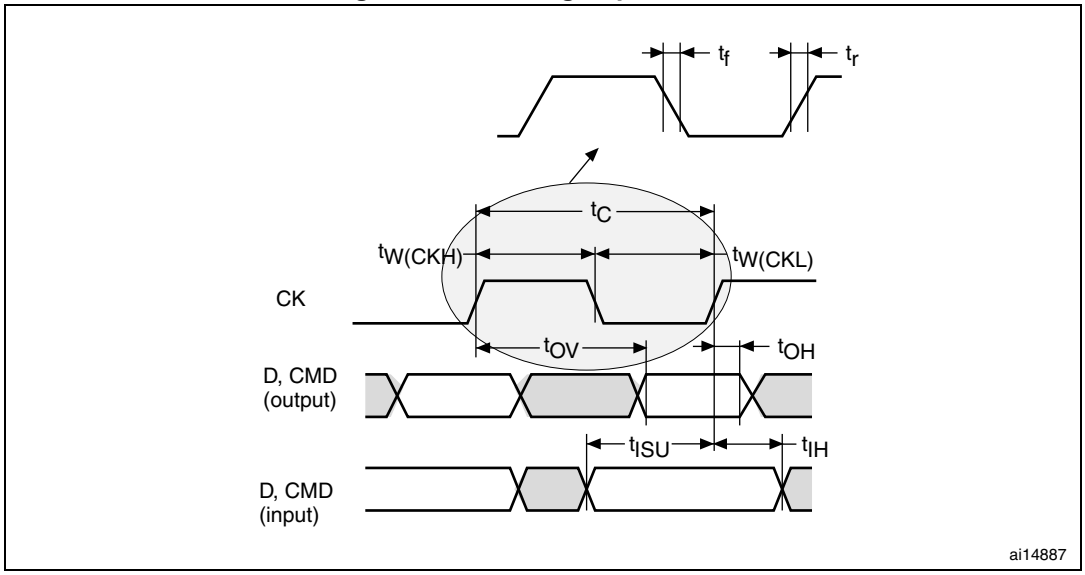


**Table 88. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | - | 17.500 | - | - | 0.6890 | - |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | - | 17.500 | - | - | 0.6890 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Table 94. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 25-Nov-2010 | 3 | Added WLCSP66 (64+2) package. Added note 1 related to LQFP176 on cover page.<br>Update I/Os in *Section : Features*.<br>Updated *Table 5: Multi-AHB matrix*.<br>Added case of BOR inactivation using IRROFF on WLCSP devices in *Section 3.15: Power supply supervisor*.<br>Reworked *Section 3.16: Voltage regulator* to clarify regulator off modes. Added *Section 3.19: VBAT operation*.<br>Modified $V_{DD\_3}$ pin in *Table 7: STM32F21x pin and ball definitions*, and added note related to the FSMC_NL pin.<br>Renamed BYPASS-REG REGOFF, and add IRROFF pin.<br>Changed $V_{SS\_SA}$ to $V_{SS}$, and $V_{DD\_SA}$ pin reserved for future use.<br>Updated maximum HSE crystal frequency to 26 MHz.<br>USART4/5 renamed UART4/5. USART4 pins renamed UART4 in *Table 7: STM32F21x pin and ball definitions*. Updated LIN and IrDA features for UART4/5 in *Table 5: USART feature comparison*.<br>*Section 6.2: Absolute maximum ratings*: Updated $V_{IN}$ minimum and maximum values and note for non-five-volt tolerant pins in *Table 10: Voltage characteristics*. Updated $I_{INJ(PIN)}$ maximum values and related notes in *Table 11: Current characteristics*.<br>Updated $V_{DDA}$ minimum value in *Table 13: General operating conditions*.<br>Added *Note 2* and updated Maximum CPU frequency in *Table 14: Limitations depending on the operating power supply range*; and added *Figure 19: Number of wait states versus fCPU and VDD range*.<br>Renamed Brownout Low, medium and High reset thresholds, Renamed $V_{BORL}/V_{BORM}/V_{BORH}$, $V_{BOR1}/V_{BOR2}/V_{BOR3}$ in *Table 18: Embedded reset and power control block characteristics*.<br>Changed $f_{LSI}$ typical value in *Table 32: LSI oscillator characteristics*. Added *Figure 33: ACCLSI versus temperature*.<br>Changed $f_{OSC\_IN}$ maximum value in *Table 29: HSE 4-26 MHz oscillator characteristics*.<br>Changed $f_{PLL\_IN}$ maximum value in *Table 33: Main PLL characteristics*, and updated jitter parameters in *Table 34: PLLI2S (audio PLL) characteristics*.<br>*Section 6.3.16: I/O port characteristics*: updated $V_{IH}$ and $V_{IL}$ in *Table 45: I/O static characteristics*.<br>Added *Note 1* below *Table 46: Output voltage characteristics*.<br>Updated $R_{PD}$ and $R_{PU}$ parameter description in *Table 56: USB OTG FS DC electrical characteristics*.<br>Updated $V_{REF+}$ minimum value in *Table 65: ADC characteristics*.<br>Updated *Table 70: Embedded internal reference voltage*.<br>Removed Ethernet and USB2 for 64-pin devices in *Table 93: Main applications versus package for STM32F2xxx microcontrollers*.<br>Added *A.2: USB OTG full speed (FS) interface solutions*, removed “OTG FS connection with external PHY” figure, updated *Figure 85*, *Figure 86*, and *Figure 87* to add STULPI01B. |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 20-Dec-2011 | 6 | Updated SDIO register addresses in *Figure 14: Memory map*.<br>Updated *Figure 3: Compatible board design between STM32F10x and STM32F2xx for LQFP144 package*, *Figure 2: Compatible board design between STM32F10x and STM32F2xx for LQFP100 package*, *Figure 1: Compatible board design between STM32F10x and STM32F2xx for LQFP64 package*, and added *Figure 4: Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package*.<br>Updated *Section 3.3: Memory protection unit*.<br>Updated *Section 3.6: Embedded SRAM*.<br>Updated *Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS)* to remove external FS OTG PHY support.<br>In *Table 7: STM32F21x pin and ball definitions*: changed SPI2_MCK and SPI3_MCK to I2S2_MCK and I2S3_MCK, respectively. Added ETH _RMII_TX_EN alternate function to PG11. Added EVENTOUT in the list of alternate functions for I/O pin/balls. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions.<br>In *Table 9: Alternate function mapping*: changed I2S3_SCK to I2S3_MCK for PC7/AF6, added FSMC_NCE3 for PG9, FSMC_NE3 for PG10, and FSMC_NCE2 for PD7. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions. Updated peripherals corresponding to AF12.<br>Removed CEXT and ESR from *Table 13: General operating conditions*.<br>Added maximum power consumption at $T_A$=25 °C in *Table 22: Typical and maximum current consumptions in Stop mode*.<br>Added CRYPTO, RNG, and HASH consumption in *Table 25: Peripheral current consumption*.<br>Updated md minimum value in *Table 35: SSCG parameters constraint*.<br>Added examples in *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*.<br>Updated *Table 53: SPI characteristics* and *Table 54: I2S characteristics*.<br>Updated *Figure 46: ULPI timing diagram* and *Table 60: ULPI timing*.<br>Updated *Table 62: Dynamics characteristics: Ethernet MAC signals for SMI*, *Table 63: Dynamics characteristics: Ethernet MAC signals for RMII*, and *Table 64: Dynamics characteristics: Ethernet MAC signals for MII*.<br>Updated maximum $f_S$ values in *Table 65: ADC characteristics*.<br>*Section 6.3.25: FSMC characteristics*: updated *Table 71* to*Table 82*, changed $C_L$ value to 30 pF, and modified FSMC configuration for asynchronous timings and waveforms. Updated *Figure 60: Synchronous multiplexed PSRAM write timings*.<br>Updated*Table 83: DCMI characteristics*.<br>Updated *Table 90: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm mechanical data*. |