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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f217vgt6

Table 1. Device summary

Reference	Part numbers
STM32F215xx	STM32F215RG, STM32F215VG, STM32F215ZG STM32F215RE, STM32F215VE, STM32F215ZE
STM32F217xx	STM32F217VG, STM32F217IG, STM32F217ZG STM32F217VE, STM32F217IE, STM32F217ZE

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Table 2. STM32F215xx and STM32F217xx: features and peripheral counts (continued)

Peripherals	STM32F215Rx	STM32F215Vx	STM32F215Zx	STM32F217Vx	STM32F217Zx	STM32F217Ix
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C					
	Junction temperature: –40 to + 125 °C					
Package	LQFP64	LQFP100	LQFP144	LQFP100	LQFP144	UFBGA176, LQFP176

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. Camera interface and Ethernet are available only in STM32F217x devices.
3. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.

and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from the Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped when the device enters the Stop or Standby mode.

3.19 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery or an external supercapacitor.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

3.20 Timers and watchdogs

The STM32F21x devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock	Max timer clock
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	60 MHz	120 MHz

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers TIM1, TIM2, TIM3, TIM4, TIM5 and TIM8 can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.35 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 and 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 7. STM32F21x pin and ball definitions (continued)

Pins					Pin name (function after reset)[1]	Pin type	I / O structure	Note	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	130	D13	PH15	I/O	FT	-	TIM8_CH3N, DCMI_D11, EVENTOUT	-
-	-	-	131	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS, I2S2_WS, DCMI_D13, EVENTOUT	-
-	-	-	132	D14	PI1	I/O	FT	-	SPI2_SCK, I2S2_SCK, DCMI_D8, EVENTOUT	-
-	-	-	133	C14	PI2	I/O	FT	-	TIM8_CH4,SPI2_MISO, DCMI_D9, EVENTOUT	-
-	-	-	134	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI, I2S2_SD, DCMI_D10, EVENTOUT	-
-	-	-	135	D9	V_{SS}	S	-	-	-	-
-	-	-	136	C9	V_{DD}	S	-	-	-	-
49	76	109	137	A14	PA14 (JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
50	77	110	138	A13	PA15 (JTDI)	I/O	FT	-	JTDI, SPI3_NSS, I2S3_WS,TIM2_CH1_ETR, SPI1_NSS/ EVENTOUT	-
51	78	111	139	B14	PC10	I/O	FT	-	SPI3_SCK, I2S3_SCK, UART4_TX, SDIO_D2, DCMI_D8, USART3_TX, EVENTOUT	-
52	79	112	140	B13	PC11	I/O	FT	-	UART4_RX, SPI3_MISO, SDIO_D3, DCMI_D4,USART3_RX, EVENTOUT	-
53	80	113	141	A12	PC12	I/O	FT	-	UART5_TX,SDIO_CK, DCMI_D9, SPI3_MOSI, I2S3_SD, USART3_CK, EVENTOUT	-
-	81	114	142	B12	PD0	I/O	FT	-	FSMC_D2,CAN1_RX, EVENTOUT	-
-	82	115	143	C12	PD1	I/O	FT	-	FSMC_D3, CAN1_TX, EVENTOUT	-

Table 8. FSMC pin definition (continued)

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PG3	-	A13	-	-	-
PG4	-	A14	-	-	-
PG5	-	A15	-	-	-
PG6	-	-	-	INT2	-
PG7	-	-	-	INT3	-
PD0	D2	D2	DA2	D2	Yes
PD1	D3	D3	DA3	D3	Yes
PD3	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	NE1	NE1	NCE2	Yes
PG9	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	-	-	-	-
PG12	-	NE4	NE4	-	-
PG13	-	A24	A24	-	-
PG14	-	A25	A25	-	-
PB7	-	NADV	NADV	-	Yes
PE0	-	NBL0	NBL0	-	Yes
PE1	-	NBL1	NBL1	-	Yes

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port H	PH0 - OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1 - OSC_OUT	-	-				-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-				-	-	-	-	-	-	ETH _MII_CRS	-	-	-	EVENTOUT
	PH3	-	-				-	-	-	-	-	-	ETH _MII_COL	-	-	-	EVENTOUT
	PH4	-	-			I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	-	EVENTOUT
	PH5	-	-			I2C2_SDA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH6	-	-			I2C2_SMBA	-	-	-	-	TIM12_CH1	-	ETH _MII_RXD2	-	-	-	EVENTOUT
	PH7	-	-			I2C3_SCL	-	-	-	-	-	-	ETH _MII_RXD3	-	-	-	EVENTOUT
	PH8	-	-			I2C3_SDA	-	-	-	-	-	-	-	-	DCMI_HSYNC	-	EVENTOUT
	PH9	-	-			I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	-	DCMI_D0	-	EVENTOUT
	PH10	-	-	TIM5_CH1			-	-	-	-	-	-	-	-	DCMI_D1	-	EVENTOUT
	PH11	-	-	TIM5_CH2			-	-	-	-	-	-	-	-	DCMI_D2	-	EVENTOUT
	PH12	-	-	TIM5_CH3			-	-	-	-	-	-	-	-	DCMI_D3	-	EVENTOUT
	PH13	-	-		TIM8_CH1N		-	-	-	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-		TIM8_CH2N		-	-	-	-	-	-	-	-	DCMI_D4	-	EVENTOUT
	PH15	-	-		TIM8_CH3N		-	-	-	-	-	-	-	-	DCMI_D11	-	EVENTOUT
Port I	PI0	-	-	TIM5_CH4			SPI2_NSS I2S2_WS	-	-	-	-	-	-	-	DCMI_D13	-	EVENTOUT
	PI1	-	-				SPI2_SCK I2S2_SCK	-	-	-	-	-	-	-	DCMI_D8	-	EVENTOUT
	PI2	-	-		TIM8_CH4		SPI2_MISO	-	-	-	-	-	-	-	DCMI_D9	-	EVENTOUT
	PI3	-	-		TIM8_ETR		SPI2_MOSI I2S2_SD	-	-	-	-	-	-	-	DCMI_D10	-	EVENTOUT
	PI4	-	-		TIM8_BKIN		-	-	-	-	-	-	-	-	DCMI_D5	-	EVENTOUT
	PI5	-	-		TIM8_CH1		-	-	-	-	-	-	-	-	DCMI_VSYNC	-	EVENTOUT
	PI6	-	-		TIM8_CH2		-	-	-	-	-	-	-	-	DCMI_D6	-	EVENTOUT
	PI7	-	-		TIM8_CH3		-	-	-	-	-	-	-	-	DCMI_D7	-	EVENTOUT
	PI8	-	-				-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-				-	-	-	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-				-	-	-	-	-	-	ETH _MII_RX_ER	-	-	-	EVENTOUT
	PI11	-	-				-	-	-	-	-	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT

Figure 14. Memory map

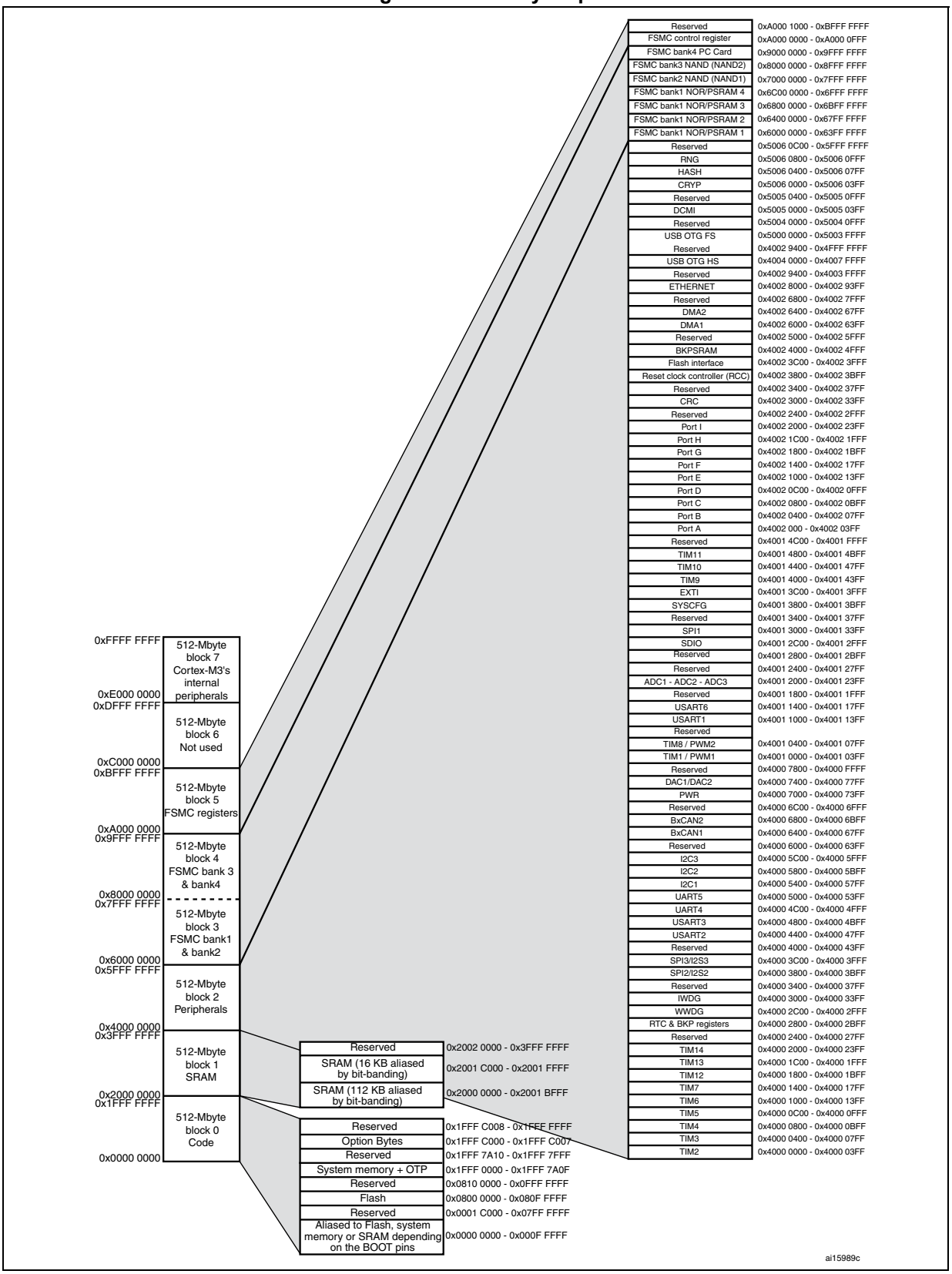


Table 21. Typical and maximum current consumption in Sleep mode

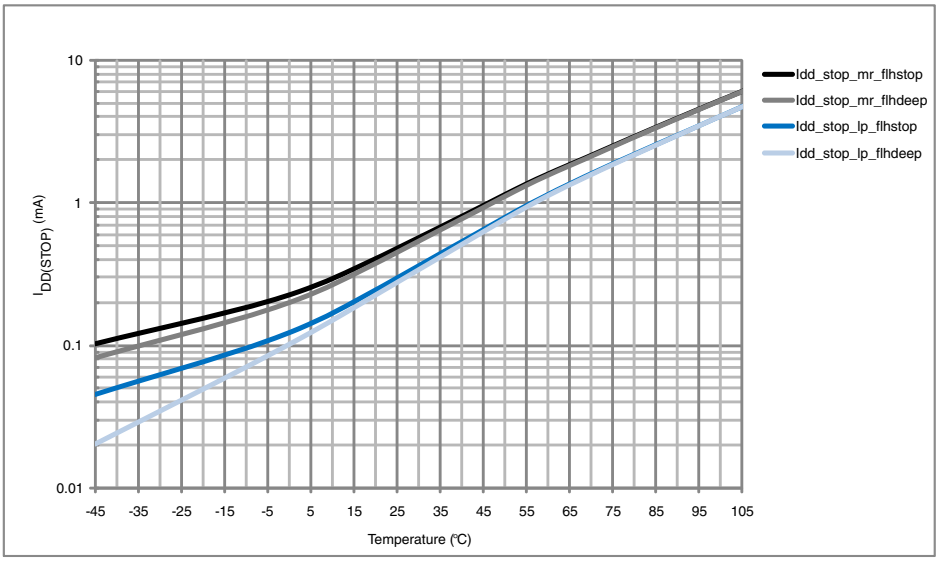
Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled(3)	120 MHz	38	51	61	mA
			90 MHz	30	43	53	
			60 MHz	20	33	43	
			30 MHz	11	25	35	
			25 MHz	8	21	31	
			16 MHz	6	19	29	
			8 MHz	3.6	17.0	27.0	
			4 MHz	2.4	15.4	25.3	
			2 MHz	1.9	14.9	24.7	
		External clock(2), all peripherals disabled	120 MHz	8	21	31	
			90 MHz	7	20	30	
			60 MHz	5	18	28	
			30 MHz	3.5	16.0	26.0	
			25 MHz	2.5	16.0	25.0	
			16 MHz	2.1	15.1	25.0	
			8 MHz	1.7	15.0	25.0	
			4 MHz	1.5	14.6	24.6	
			2 MHz	1.4	14.2	24.3	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Table 22. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.55	1.2	11.00	20.00	mA
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.50	1.2	11.00	20.00	
	Supply current in Stop mode with main regulator in Low-power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.35	1.1	8.00	15.00	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.30	1.1	8.00	15.00	

Figure 27. Typical current consumption vs. temperature in Stop mode



1. All typical and maximum values from table 18 and figure 26 will be reduced over time by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes

Table 25. Peripheral current consumption

Peripheral[1]		Typical consumption at 25 °C	Unit
AHB1	GPIO A	0.45	mA
	GPIO B	0.43	
	GPIO C	0.46	
	GPIO D	0.44	
	GPIO E	0.44	
	GPIO F	0.42	
	GPIO G	0.44	
	GPIO H	0.42	
	GPIO I	0.43	
	OTG_HS + ULPI	3.64	
	CRC	1.17	
	BKPSRAM	0.21	
	DMA1	2.76	
	DMA2	2.85	
	ETH_MAC + ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	2.99	
AHB2	OTG_FS	3.16	
	DCMI	0.60	
AHB3	FSMC	1.74	
AHB2	CRYPTO	0.39	mA
	HASH	0.50	
	RNG	0.43	

Figure 28. High-speed external clock source AC timing diagram

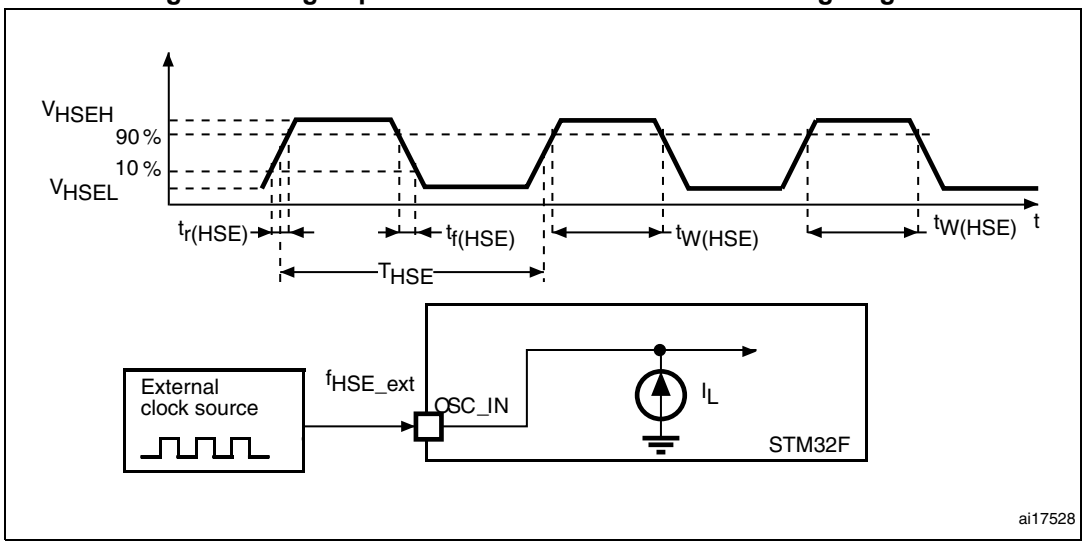
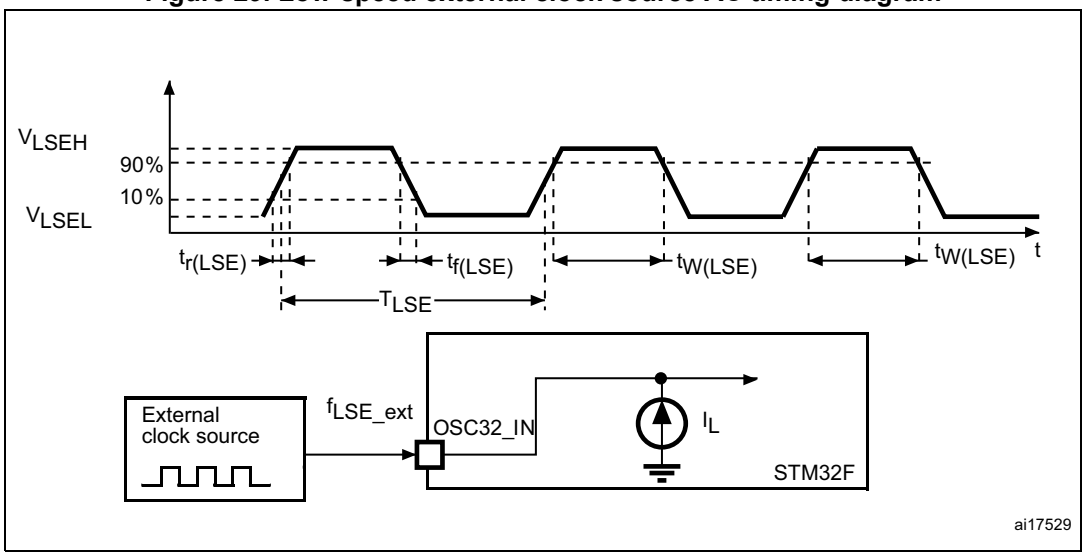


Figure 29. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Figure 46. ULPI timing diagram

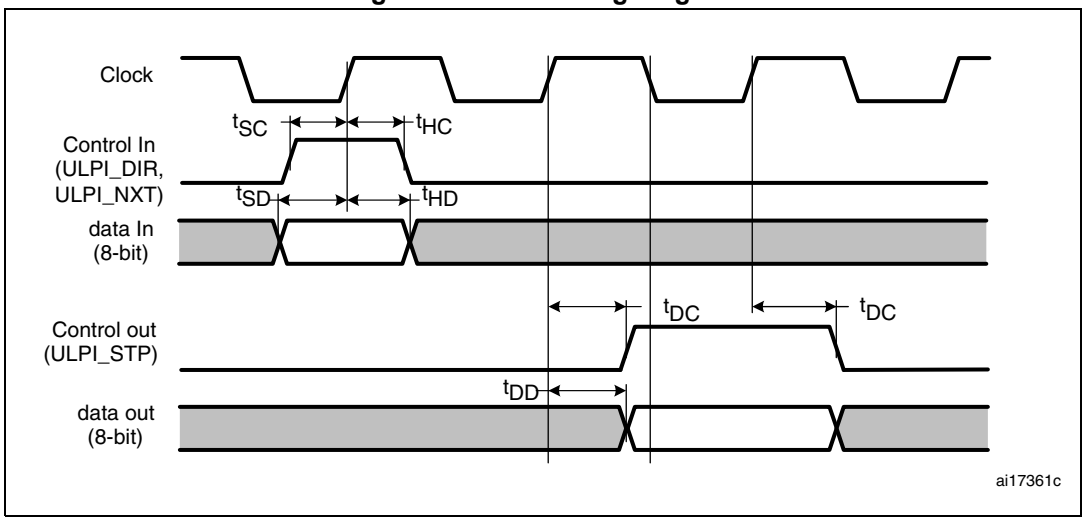


Table 60. ULPI timing

Symbol	Parameter	Value(1)		Unit
		Min	Max	
t_{SC}	Control in (ULPI_DIR) setup time	-	2.0	ns
	Control in (ULPI_NXT) setup time	-	1.5	
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0	-	
t_{SD}	Data in setup time	-	2.0	
t_{HD}	Data in hold time	0	-	
t_{DC}	Control out (ULPI_STP) setup time and hold time	-	9.2	
t_{DD}	Data out available from clock rising edge	-	10.7	

1. V_{DD} = 2.7 V to 3.6 V and T_A = –40 to 85 °C.

Ethernet characteristics

Table 61 shows the Ethernet operating voltage.

Table 61. Ethernet DC electrical characteristics

Symbol		Parameter	Min(1)	Max(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 62 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 47* shows the corresponding timing diagram.

Table 76. Synchronous multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	0	-	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	2	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	0.5	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 61. Synchronous non-multiplexed NOR/PSRAM read timings

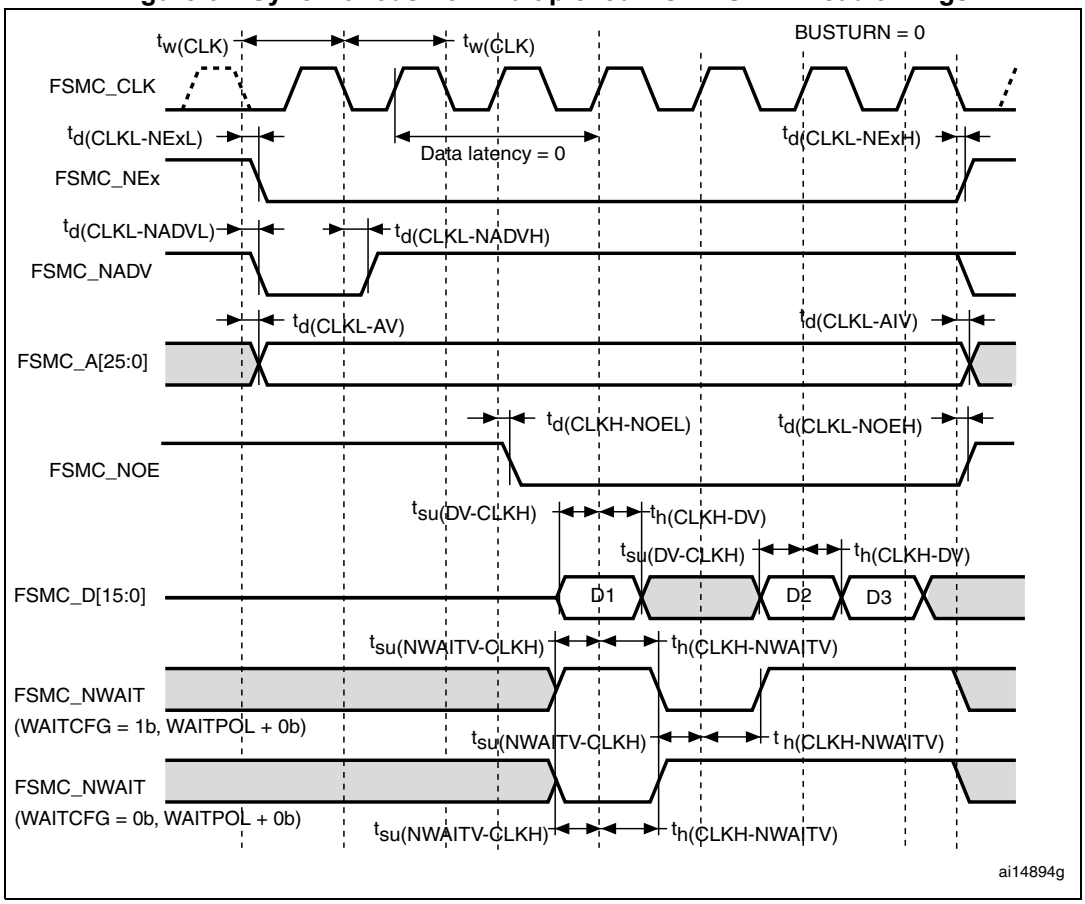


Table 77. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2.5	ns

Table 80. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK}$ - 0.5	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK}$- 1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK}$- 3	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK}$+ 1.5	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}$	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK}$+ 1	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	$5T_{HCLK}$– 0.5	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK}$+ 1	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 69 through *Figure 72* represent synchronous waveforms, together with *Table 81* and *Table 82* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 94. Document revision history (continued)

Date	Revision	Changes
24-Apr-2012	7	Updated number of USB OTG HS and FS, added *Note 1* related to FSMC and *Note 3* related to SPI/I2S in *Table 2: STM32F215xx and STM32F217xx: features and peripheral counts*. Added *Note 2* and update TIM5 in *Figure 4: STM32F21x block diagram*. Updated maximum number of maskable interrupts in *Section 3.10: Nested vectored interrupt controller (NVIC)*. Removed STM32F215xx in *Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS)*. Removed support of I2C for OTG PHY in *Section 3.29: Universal serial bus on-the-go high-speed (OTG_HS)*. Removed OTG_HS_SCL, OTG_HS_SDA, OTG_FS_INTN in *Table 7: STM32F21x pin and ball definitions* and *Table 9: Alternate function mapping*. PH10 alternate function TIM5_CH1_ETR renamed TIM5_CH1. Added *Table 8: FSMC pin definition*. Updated $V_{POR/PDR}$ in *Table 18: Embedded reset and power control block characteristics*. Updated V_{DDA} and V_{REF+} decoupling capacitor in *Figure 17: Power supply scheme*. Updated typical values in *Table 23: Typical and maximum current consumptions in Standby mode* and *Table 24: Typical and maximum current consumptions in VBAT mode*. Updated *Table 29: HSE 4-26 MHz oscillator characteristics* and *Table 30: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Updated *Table 36: Flash memory characteristics*, *Table 37: Flash memory programming*, and *Table 38: Flash memory programming with VPP*. Updated *Section : Output driving current*. Updated *Note 3* and removed note related to minimum hold time value in *Table 51: I2C characteristics*. Updated *Table 63: Dynamics characteristics: Ethernet MAC signals for RMII*. Updated C_{ADC}, I_{VREF+}, and I_{VDDA} in *Table 65: ADC characteristics*. Updated note concerning ADC accuracy vs. negative injection current below *Table 66: ADC accuracy*. Updated *Figure 85: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*. Appendix *A.1: Main applications versus package*: removed number of address lines for FSMC/NAND in *Table 93: Main applications versus package for STM32F2xxx microcontrollers*. Appendix *A.4: Ethernet interface solutions*: updated *Figure 92: Complete audio player solution 1* and *Figure 93: Complete audio player solution 2*.

Table 94. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	8	Removed Figure 4. Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package. Updated number of AHB buses in *Section 2: Description* and *Section 3.12: Clocks and startup*. Updated *Note 2* below *Figure 4: STM32F21x block diagram*. Changed System memory to System memory + OTP in *Figure 14: Memory map*. Added *Note 1* below *Table 15: VCAP1/VCAP2 operating conditions*. Updated V_{DDA} and V_{REF+} decoupling capacitor in *Figure 17: Power supply scheme* and updated *Note 3*. Changed simplex mode into half-duplex mode in *Section 3.24: Inter-integrated sound (I2S)*. Replaced DAC1_OUT and DAC2_OUT by DAC_OUT1 and DAC_OUT2, respectively. Changed TIM2_CH1/TIM2_ETR into TIM2_CH1_ETR for PA0 and PA5 in *Table 9: Alternate function mapping*. Updated note applying to I_{DD} (external clock and all peripheral disabled) in *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*. Updated *Note 3* below *Table 21: Typical and maximum current consumption in Sleep mode*. Removed f_{HSE_ext} typical value in *Table 27: High-speed external user clock characteristics*. Updated master I2S clock jitter conditions and values in *Table 34: PLLI2S (audio PLL) characteristics*. Updated equations in *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Swapped TTL and CMOS port conditions for V_{OL} and V_{OH} in *Table 46: Output voltage characteristics*. Updated $V_{IL(NRST)}$ and $V_{IH(NRST)}$ in *Table 48: NRST pin characteristics*. Updated *Table 53: SPI characteristics* and *Table 54: I2S characteristics*.Removed note 1 related to measurement points below *Figure 41: SPI timing diagram - slave mode and CPHA = 1*, *Figure 42: SPI timing diagram - master mode*, and *Figure 43: I2S slave timing diagram (Philips protocol)(1)*. Updated t_{HC} in *Table 60: ULPI timing*. Updated *Figure 47: Ethernet SMI timing diagram*, *Table 62: Dynamics characteristics: Ethernet MAC signals for SMI* and *Table 63: Dynamics characteristics: Ethernet MAC signals for RMII*. Update f_{TRIG} in *Table 65: ADC characteristics*. Updated I_{DDA} description in *Table 67: DAC characteristics*. Updated note below *Figure 52: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 53: Power supply and reference decoupling (VREF+ connected to VDDA)*. Replaced $t_{d(CLKL-NOEL)}$ by $t_{d(CLKH-NOEL)}$ in *Table 75: Synchronous multiplexed NOR/PSRAM read timings*, *Table 77: Synchronous non-multiplexed NOR/PSRAM read timings*, *Figure 59: Synchronous multiplexed NOR/PSRAM read timings* and *Figure 61: Synchronous non-multiplexed NOR/PSRAM read timings*.