STMicroelectronics - STM32F217VGT6TR Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f217vgt6tr

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2 Description

The STM32F21x family is based on the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of up to 120 MHz. The family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 128 Kbytes of system SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

The devices also feature an adaptive real-time memory accelerator (ART Accelerator™) that allows to achieve a performance equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz. This performance has been validated using the CoreMark® benchmark.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. a true number random generator (RNG). They also feature standard and advanced communication interfaces. New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a cryptographic acceleration cell, and a camera interface for CMOS sensors. The devices also feature standard peripherals.

- Up to three I^2Cs
- Three SPIs, two I^2Ss. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external PLL to allow synchronization.
- Four USARTs and two UARTs
- A USB OTG high-speed with full-speed capability (with the ULPI)
- A second USB OTG (full-speed)
- Two CANs
- An SDIO interface
- Ethernet and camera interface available on STM32F217xx devices only.

Note: The STM32F215xx and STM32F217xx devices operate in the –40 to +105 °C temperature range from a 1.8 V to 3.6 V power supply.

A comprehensive set of power-saving modes allow the design of low-power applications.

STM32F215xx and STM32F217xx devices are offered in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.These features make the STM32F215xx and STM32F217xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 4 shows the general block diagram of the device family.

Table 2. STM32F215xx and STM32F217xx: features and peripheral counts (continued)

Peripherals	STM32F215Rx	STM32F215Vx	STM32F215Zx	STM32F217Vx	STM32F217Zx	STM32F217Ix
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C					
	Junction temperature: –40 to + 125 °C					
Package	LQFP64	LQFP100	LQFP144	LQFP100	LQFP144	UFBGA176, LQFP176

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. Camera interface and Ethernet are available only in STM32F217x devices.
3. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.

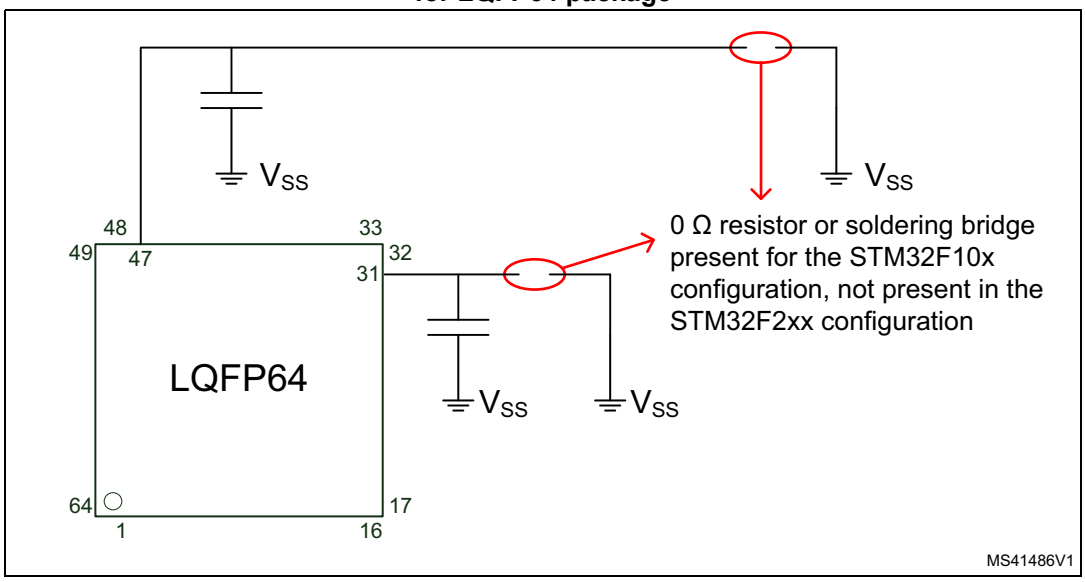
2.1 Full compatibility throughout the family

The STM32F215xx and STM32F217xx constitute the STM32F21x family whose members are fully pin-to-pin, software and feature compatible, allowing the user to try different memory densities and peripherals for a greater degree of freedom during the development cycle.

The STM32F215xx and STM32F217xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F215xx and STM32F217xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F21x family remains simple as only a few pins are impacted.

Figure 1, *Figure 2* and *Figure 3* provide compatible board designs between the STM32F21x and the STM32F10xxx family.

Figure 1. Compatible board design between STM32F10x and STM32F2xx for LQFP64 package



This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

3.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In particular, the ethernet and USB OTG FS peripherals can be clocked by the system clock.

Several prescalers and PLLs allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 120 MHz and the maximum frequency the high-speed APB domains is 60 MHz. The maximum allowed frequency of the low-speed APB domain is 30 MHz.

The devices embed a dedicate PLL (PLLI2S) that allow them to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

Table 7. STM32F21x pin and ball definitions (continued)

Pins					Pin name (function after reset)[1]	Pin type	I / O structure	Note	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	LQFP176	UFBGA176						
-	39	59	69	P8	PE8	I/O	FT	-	FSMC_D5, TIM1_CH1N, EVENTOUT	-
-	40	60	70	P9	PE9	I/O	FT	-	FSMC_D6, TIM1_CH1, EVENTOUT	-
-	-	61	71	M9	V_{SS}	S	-	-	-	-
-	-	62	72	N9	V_{DD}	S	-	-	-	-
-	41	63	73	R9	PE10	I/O	FT	-	FSMC_D7, TIM1_CH2N, EVENTOUT	-
-	42	64	74	P10	PE11	I/O	FT	-	FSMC_D8,TIM1_CH2, EVENTOUT	-
-	43	65	75	R10	PE12	I/O	FT	-	FSMC_D9,TIM1_CH3N, EVENTOUT	-
-	44	66	76	N11	PE13	I/O	FT	-	FSMC_D10,TIM1_CH3, EVENTOUT	-
-	45	67	77	P11	PE14	I/O	FT	-	FSMC_D11,TIM1_CH4, EVENTOUT	-
-	46	68	78	R11	PE15	I/O	FT	-	FSMC_D12,TIM1_BKIN, EVENTOUT	-
29	47	69	79	R12	PB10	I/O	FT	-	SPI2_SCK, I2S2_SCK, I2C2_SCL, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, TIM2_CH3, EVENTOUT	-
30	48	70	80	R13	PB11	I/O	FT	-	I2C2_SDA,USART3_RX, OTG_HS_ULPI_D4, ETH_RMII_TX_EN, ETH_MII_TX_EN, TIM2_CH4, EVENTOUT	-
31	49	71	81	M10	V_{CAP_1}	S		-	-	-
32	50	72	82	N10	V_{DD}	S		-	-	-
-	-	-	83	M11	PH6	I/O	FT	-	I2C2_SMBA, TIM12_CH1, ETH_MII_RXD2, EVENTOUT	-
-	-	-	84	N12	PH7	I/O	FT	-	I2C3_SCL, ETH_MII_RXD3, EVENTOUT	-

Figure 21. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals ON

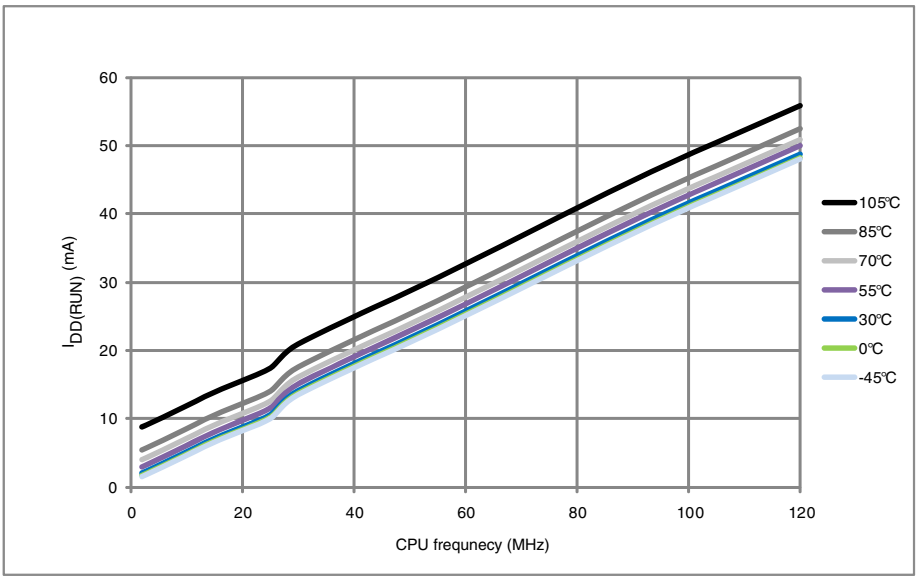


Figure 22. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals OFF

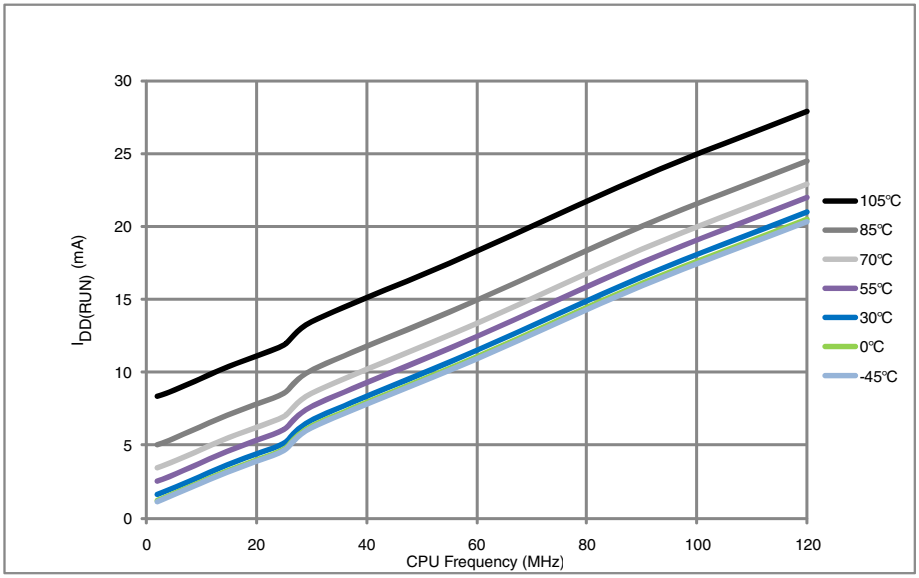
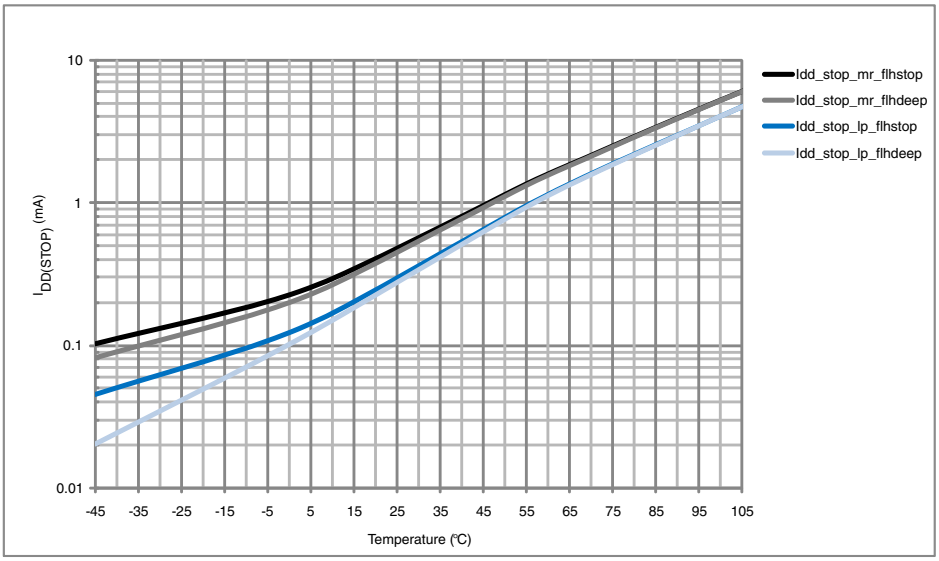


Table 22. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.55	1.2	11.00	20.00	mA
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.50	1.2	11.00	20.00	
	Supply current in Stop mode with main regulator in Low-power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.35	1.1	8.00	15.00	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.30	1.1	8.00	15.00	

Figure 27. Typical current consumption vs. temperature in Stop mode



1. All typical and maximum values from table 18 and figure 26 will be reduced over time by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 27* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 13*.

Table 27. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)	-	1	-	26	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 28* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 13*.

Table 28. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Table 34. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12.288 MHz N=432, R=5 on 1000 samples		-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design, not tested in production.
3. Value given with main PLL running.
4. Guaranteed by characterization results, not tested in production.

Table 36. Flash memory characteristics

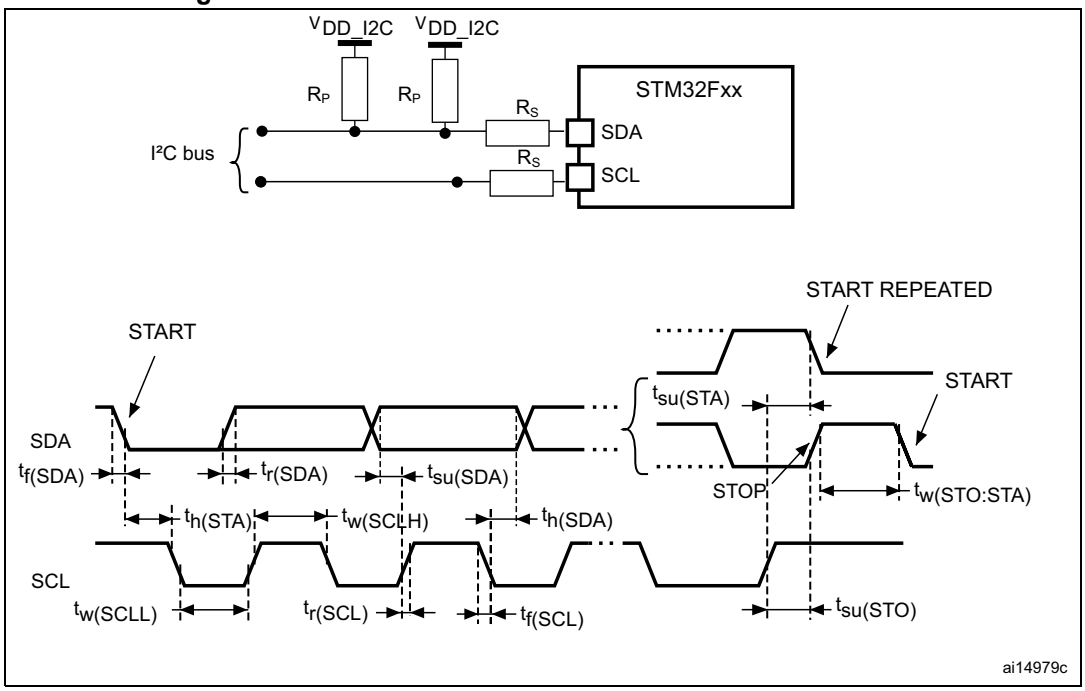
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode V_{DD} = 3.3 V	-	12	-	

Table 37. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization results, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

Figure 39. I²C bus AC waveforms and measurement circuit



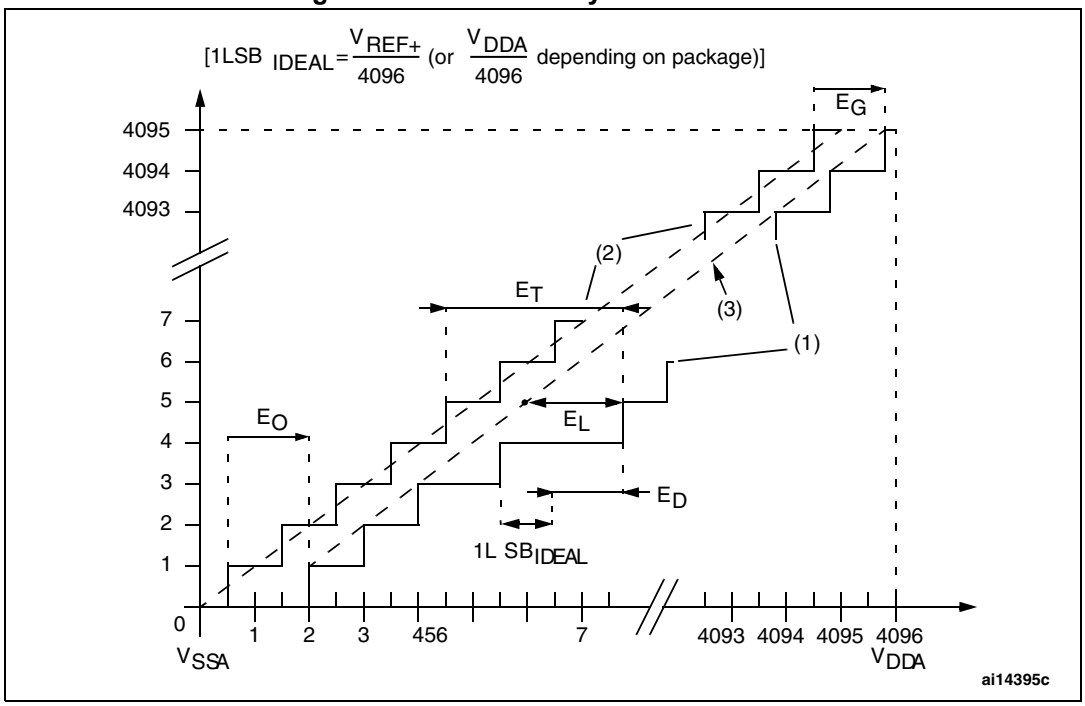
1. R_S= series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I²C bus power supply.

Table 52. SCL frequency (f_{PCLK1}= 30 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

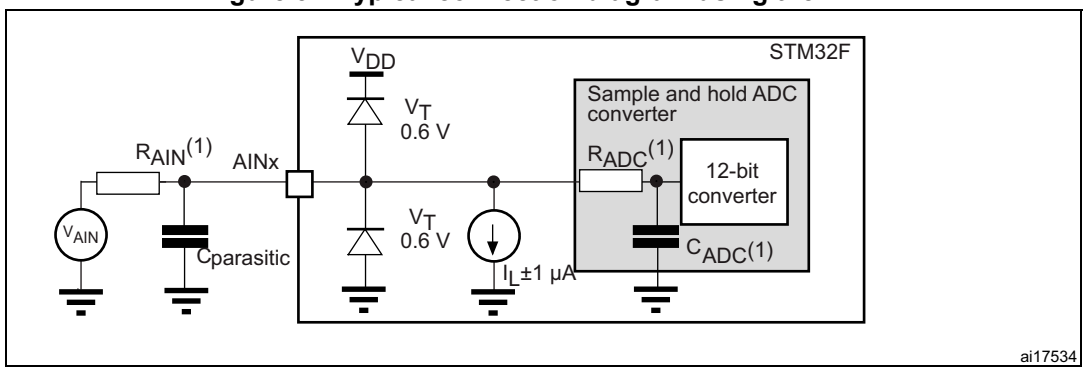
1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 50. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 51. Typical connection diagram using the ADC



1. Refer to *Table 65* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 59. Synchronous multiplexed NOR/PSRAM read timings

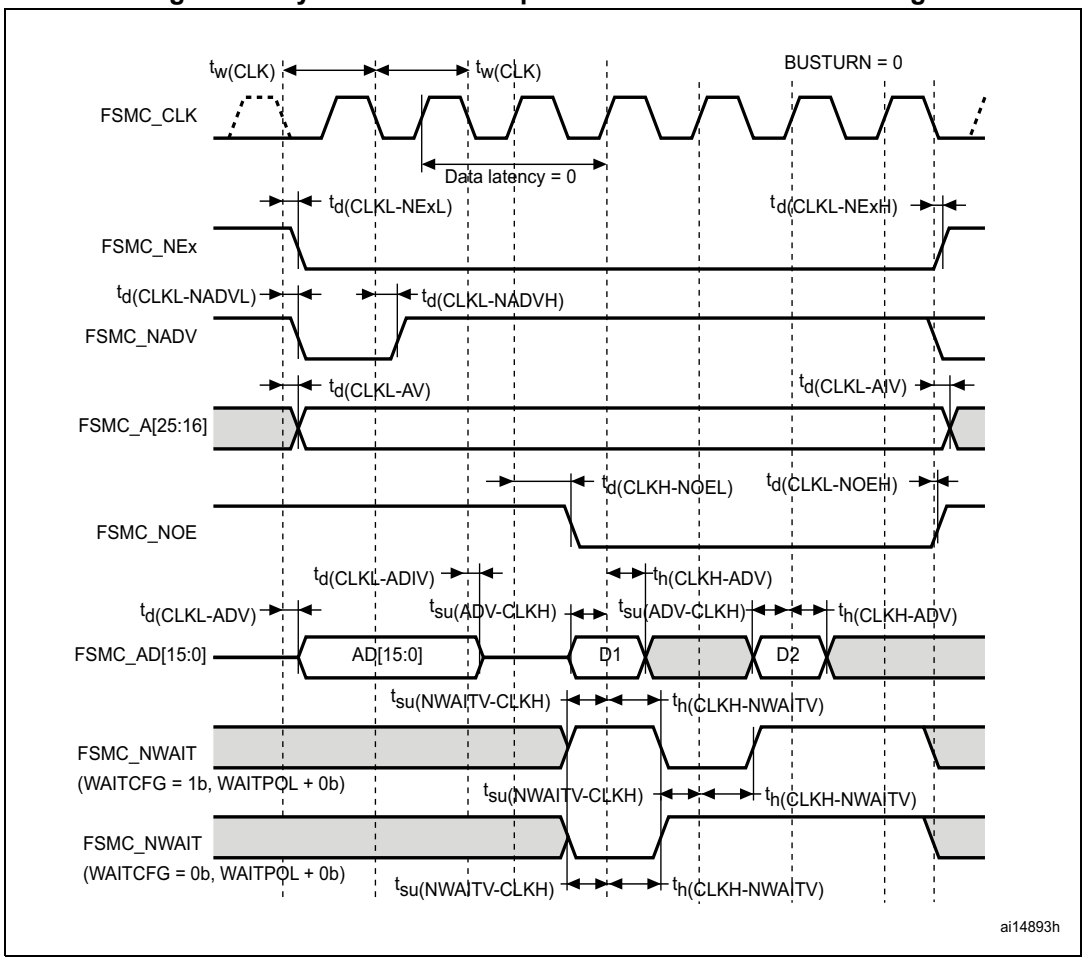


Table 75. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1.5	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	2.5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	0	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	3	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns

Table 77. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	4	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	3	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	8	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 62. Synchronous non-multiplexed PSRAM write timings

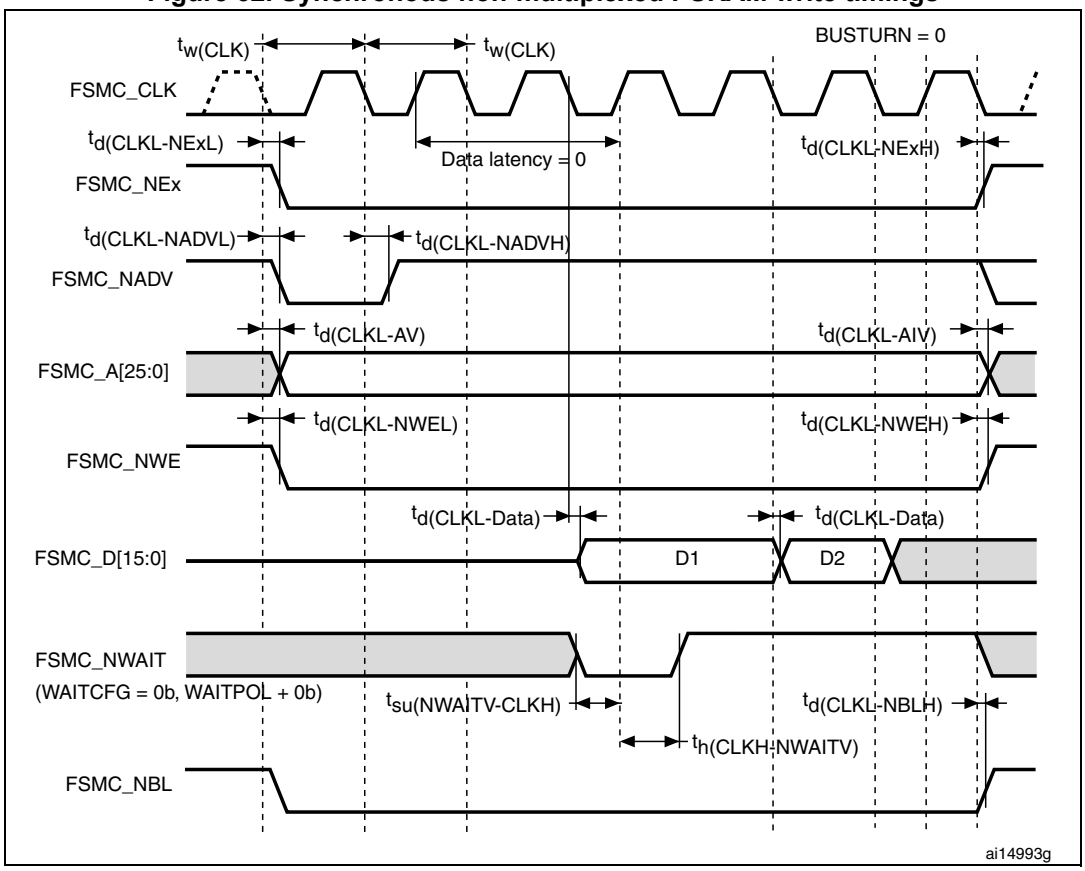
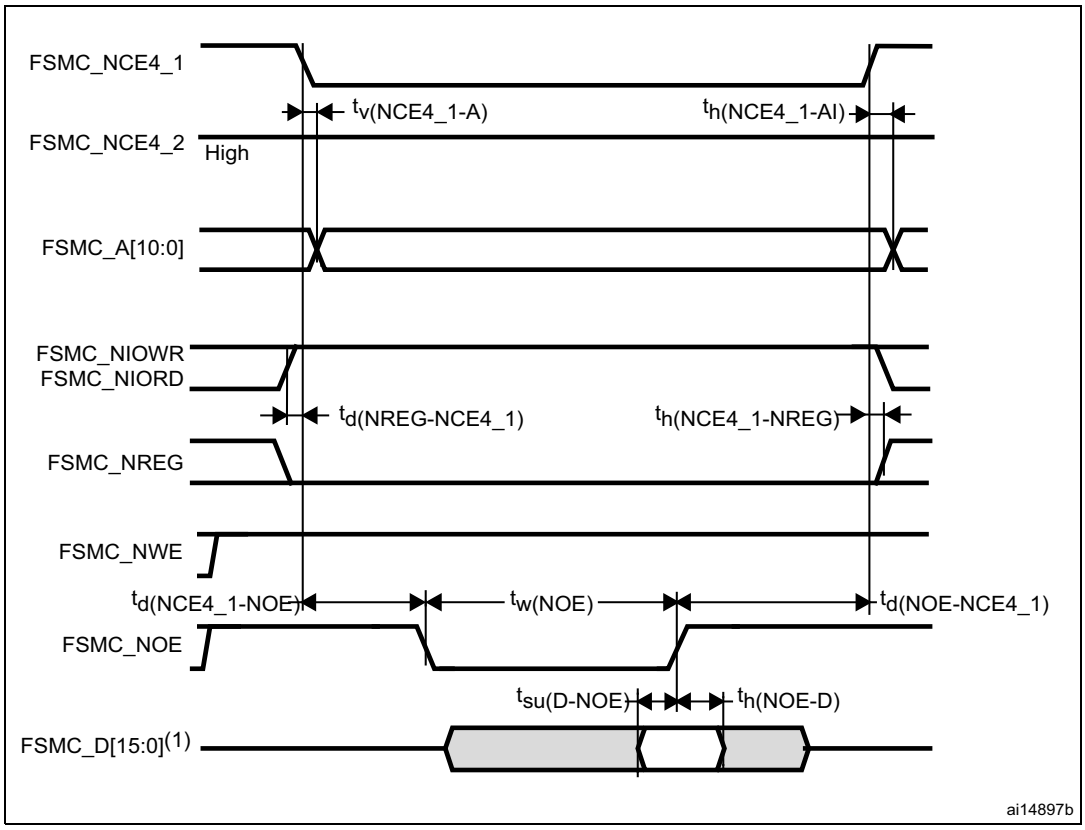


Table 78. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$- 1	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns

Figure 65. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 74. SD default mode

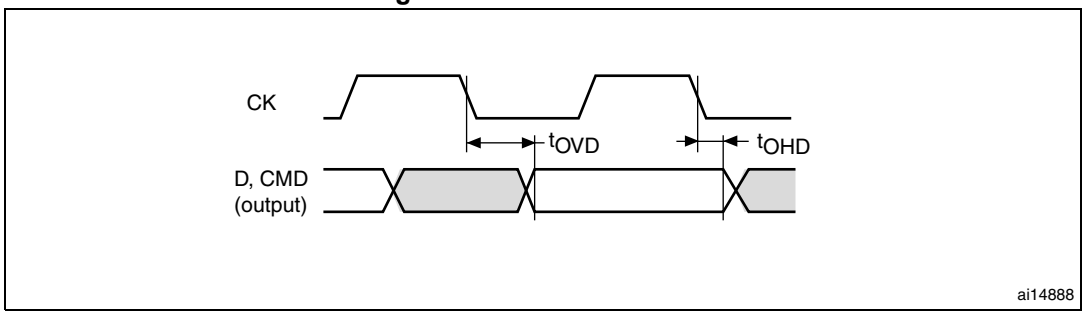


Table 84. SD/MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq 30$ pF	0	48	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	8/3	-
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	32	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	31	-	
t_r	Clock rise time	$C_L \leq 30$ pF	-	3.5	
t_f	Clock fall time	$C_L \leq 30$ pF	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	0.3	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

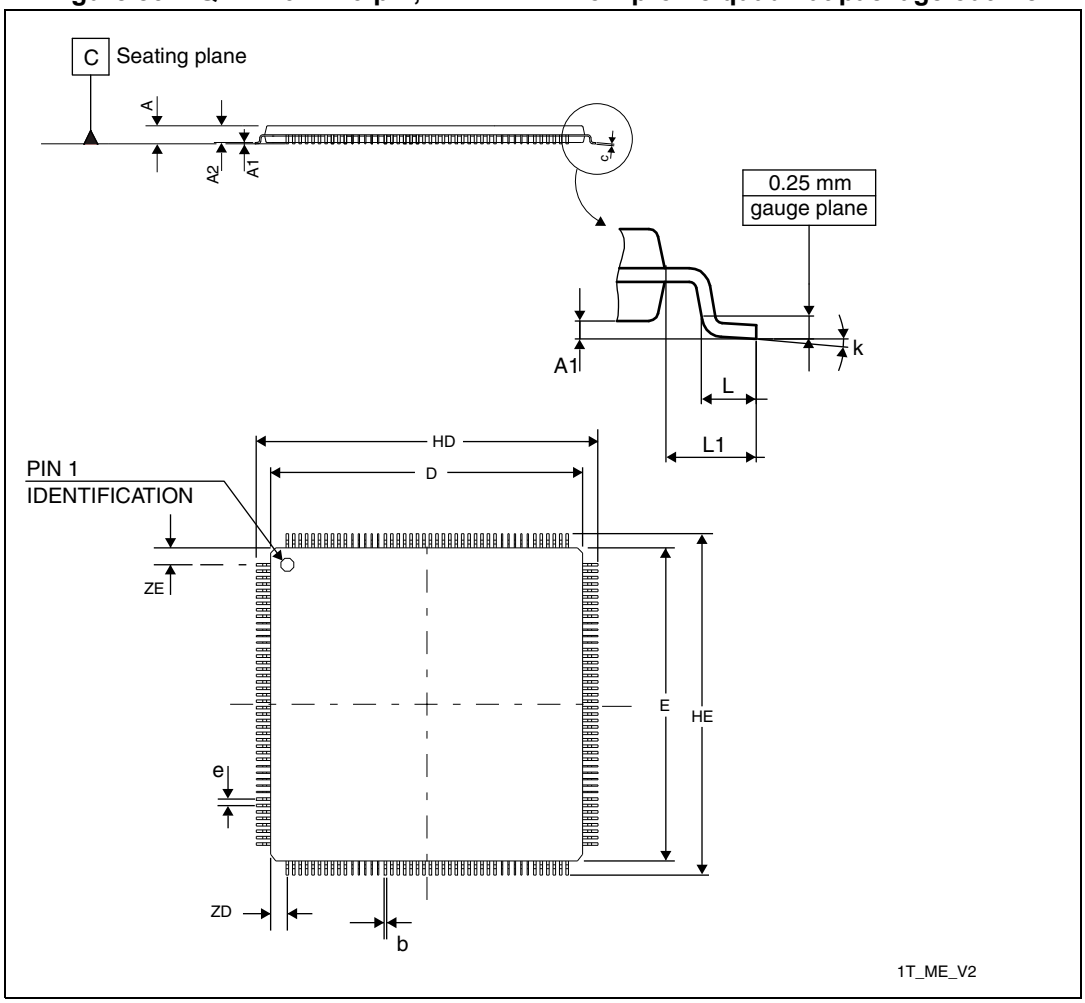
6.3.28 RTC characteristics

Table 85. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

7.4 LQFP176 package information

Figure 83. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline



1. Drawing is not to scale.

Table 89. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data

Symbol	Dimensions					
	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

Table 94. Document revision history (continued)

Date	Revision	Changes
04-Nov-2013	9 (continued)	Updated *Figure 75: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 86: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Updated *Figure 77: LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 80: LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline*, *Figure 83: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Updated *Figure 85: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline* and *Figure 85: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*. Removed Appendix A Application block diagrams.
27-Oct-2014	10	Updated V_{BAT} voltage range in *Figure 17: Power supply scheme*. Added caution note in *Section 6.1.6: Power supply scheme*. Updated V_{IN} in *Table 13: General operating conditions*. Removed note 1 in *Table 22: Typical and maximum current consumptions in Stop mode*. Updated *Table 44: I/O current injection susceptibility*, *Section 6.3.16: I/O port characteristics* and *Section 6.3.17: NRST pin characteristics*. Removed note 3 in *Table 68: Temperature sensor characteristics*. Added *Figure 79: LQFP100 marking (package top view)* and *Figure 82: LQFP144 marking (package top view)*.
23-Feb-2016	11	Updated *Section 1: Introduction*. Updated *Table 31: HSI oscillator characteristics* and its footnotes. Updated *Figure 34: PLL output clock waveforms in center spread mode*, *Figure 35: PLL output clock waveforms in down spread mode*, *Figure 52: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 53: Power supply and reference decoupling (VREF+ connected to VDDA)*. Updated *Section 7: Package information* and its subsections.
07-Jul-2016	12	Updated *Features* and *Section 2: Description*. Updated figures *1*, *2* and *3* in *Section 2.1: Full compatibility throughout the family*. Updated *Device marking* and *Figure 79* in *Section 7.2: LQFP100 package information*. Updated *Device marking* and *Figure 82* in *Section 7.3: LQFP144 package information*. Updated *Section 7.5: UFBGA176+25 package information* with introduction of *Device marking* and *Figure 87*. Updated *Table 93: Ordering information scheme*.
16-Aug-2016	13	Updated *Figure 52: Power supply and reference decoupling (VREF+ not connected to VDDA)*. Updated title of *Section 8: Ordering information*.