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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f217vgt7

1 Introduction

This datasheet provides the description of the STM32F215xx and STM32F217xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F215xx and STM32F217xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F21x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

3.4 Embedded Flash memory

The STM32F21x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbyte available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All STM32F21x products embed:

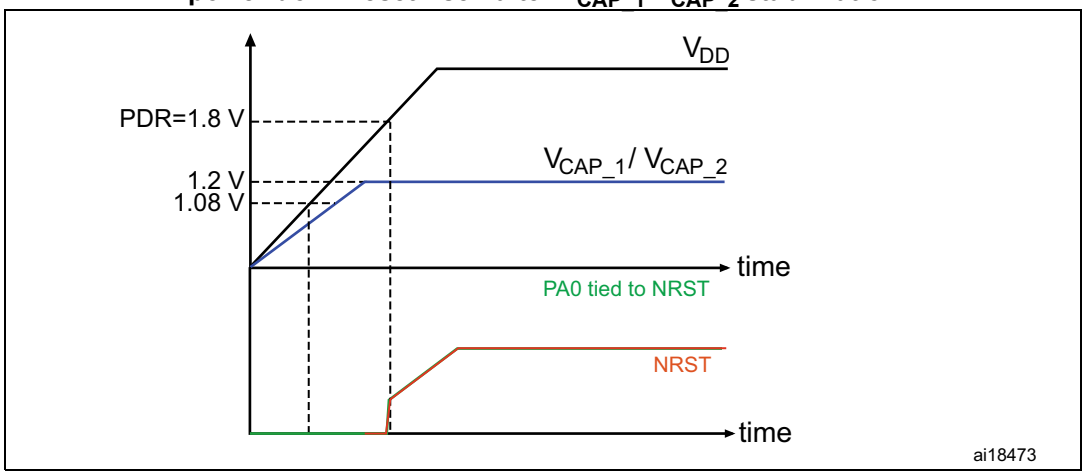
- Up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states
- 4 Kbytes of backup SRAM.

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

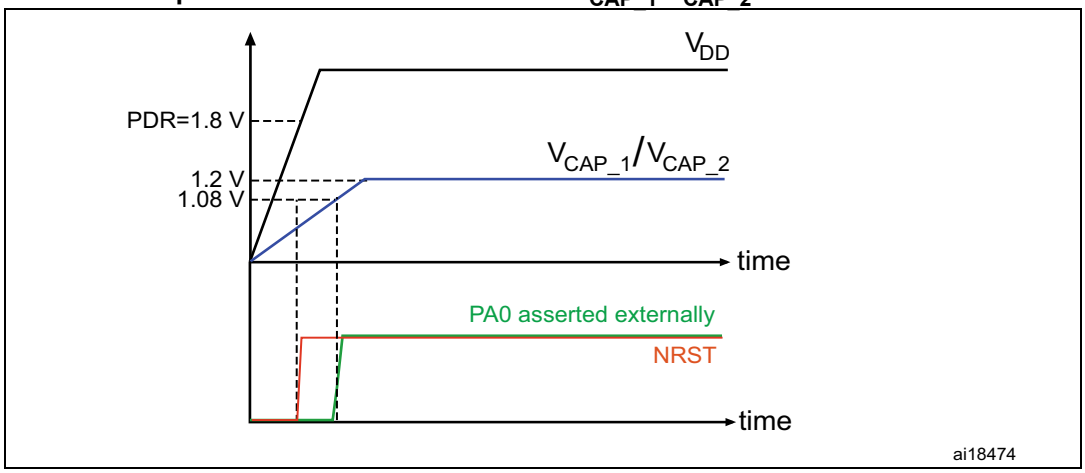
The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 7. Startup in regulator OFF: slow V_{DD} slope, power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid both whatever the internal reset mode (ON or OFF).

Figure 8. Startup in regulator OFF: fast V_{DD} slope, power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 3. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON/internal reset ON	Regulator ON/internal reset OFF	Regulator OFF/internal reset ON
LQFP64 LQFP100 LQFP144 LQFP176	Yes	No	No
UFBGA176	Yes REGOFF set to V_{SS}	No	Yes REGOFF set to V_{DD}

3.17 Real-time clock (RTC), backup SRAM and backup registers

The backup domain of the STM32F21x devices includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Its main features are the following:

- Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.
- It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.
- Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.
- A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The 4-Kbyte backup SRAM is an EEPROM-like area.It can be used to store data which need to be retained in VBAT and standby mode.This memory area is disabled to minimize power consumption (see *Section 3.18: Low-power modes*). It can be enabled by software.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.18: Low-power modes*).

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or the V_{BAT} pin.

3.18 Low-power modes

The STM32F21x family supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC

and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from the Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped when the device enters the Stop or Standby mode.

3.19 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery or an external supercapacitor.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

3.20 Timers and watchdogs

The STM32F21x devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock	Max timer clock
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	60 MHz	120 MHz

Table 7. STM32F21x pin and ball definitions (continued)

Pins					Pin name (function after reset)(1)	Pin type	I / O structure	Note	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	LQFP176	UFBGA176						
38	64	97	116	G15	PC7	I/O	FT	-	I2S3_MCK, TIM8_CH2,SDIO_D7, USART6_RX, DCMI_D1,TIM3_CH2, EVENTOUT	-
39	65	98	117	G14	PC8	I/O	FT	-	TIM8_CH3,SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT	-
40	66	99	118	F14	PC9	I/O	FT	-	I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4,SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT	-
41	67	100	119	F15	PA8	I/O	FT	-	MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-
42	68	101	120	E15	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
43	69	102	121	D15	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, OTG_FS_ID,DCMI_D1, EVENTOUT	-
44	70	103	122	C15	PA11	I/O	FT	-	USART1_CTS, CAN1_RX, TIM1_CH4, OTG_FS_DM, EVENTOUT	-
45	71	104	123	B15	PA12	I/O	FT	-	USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT	-
46	72	105	124	A15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
47	73	106	125	F13	V_{CAP_2}	S	-	-	-	-
-	74	107	126	F12	V_{SS}	S	-	-	-	-
48	75	108	127	G13	V_{DD}	S	-	-	-	-
-	-	-	128	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	129	E13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-

Table 7. STM32F21x pin and ball definitions (continued)

Pins					Pin name (function after reset)[1]	Pin type	I / O structure	Note	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	132	160	B7	PG15	I/O	FT	-	USART6_CTS, DCMI_D13, EVENTOUT	-
55	89	133	161	A10	PB3 (JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, SPI3_SCK, I2S3_SCK, TIM2_CH2, SPI1_SCK, EVENTOUT	-
56	90	134	162	A9	PB4	I/O	FT	-	NJTRST, SPI3_MISO, TIM3_CH1, SPI1_MISO, EVENTOUT	-
57	91	135	163	A6	PB5	I/O	FT	-	I2C1_SMBA, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT,TIM3_CH2, SPI1_MOSI, SPI3_MOSI, DCMI_D10, I2S3_SD, EVENTOUT	-
58	92	136	164	B6	PB6	I/O	FT	-	I2C1_SCL, TIM4_CH1, CAN2_TX, DCMI_D5,USART1_TX, EVENTOUT	-
59	93	137	165	B5	PB7	I/O	FT	-	I2C1_SDA, FSMC_NL[6], DCMI_VSYNC, USART1_RX, TIM4_CH2, EVENTOUT	-
60	94	138	166	D6	BOOT0	I	B	-	-	V_{PP}
61	95	139	167	A5	PB8	I/O	FT	-	TIM4_CH3,SDIO_D4, TIM10_CH1, DCMI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-
62	96	140	168	B4	PB9	I/O	FT	-	SPI2_NSS, I2S2_WS, TIM4_CH4, TIM11_CH1, SDIO_D5, DCMI_D7, I2C1_SDA, CAN1_TX, EVENTOUT	-
-	97	141	169	A4	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, DCMI_D2, EVENTOUT	-
-	98	142	170	A3	PE1	I/O	FT	-	FSMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	D5	V_{SS}	S		-	-	-

Table 13. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD}(2)	1.8	3.6	
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	
V_{IN}	Input voltage on RST and FT pins	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	5.5	
		1.7 V ≤ V_{DD} ≤ 2 V	–0.3	5.2	
	Input voltage on TTa pins	-	–0.3	V_{DD}+0.3	
	Input voltage on BOOT0 pin	-	0	9	
V_{CAP1}	Internal core voltage to be supplied externally in REGOFF mode	-	1.1	1.3	
V_{CAP2}					
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LQFP64	-	444	mW
		LQFP100	-	434	
		LQFP144	-	500	
		LQFP176	-	526	
		UFBGA176	-	513	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(4)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(4)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

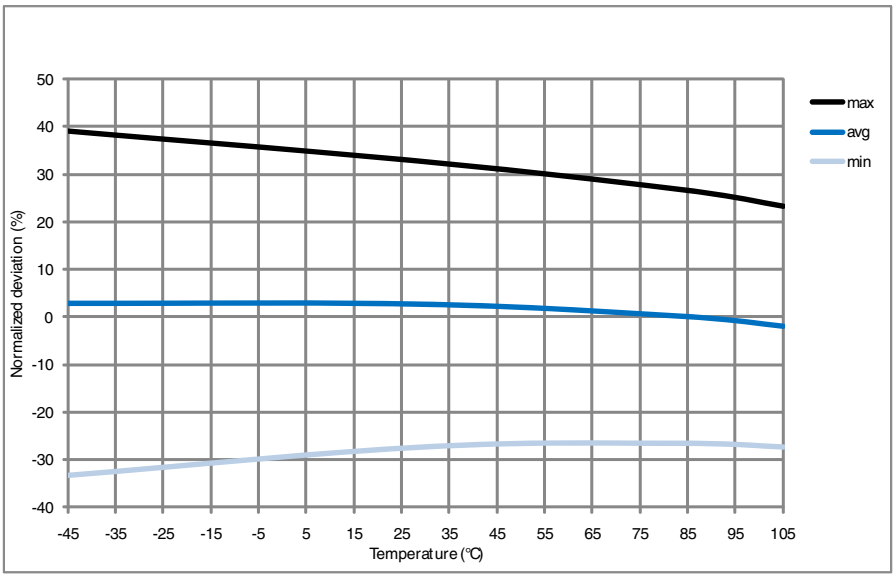
1. When the ADC is used, refer to *Table 65: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
4. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 20. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled(3)	120 MHz	61	81	93	mA
			90 MHz	48	68	80	
			60 MHz	33	53	65	
			30 MHz	18	38	50	
			25 MHz	14	34	46	
			16 MHz(4)	10	30	42	
			8 MHz	6	26	38	
			4 MHz	4	24	36	
			2 MHz	3	23	35	
		External clock(2), all peripherals disabled	120 MHz	33	54	66	
			90 MHz	27	47	59	
			60 MHz	19	39	51	
			30 MHz	11	31	43	
			25 MHz	8	28	41	
			16 MHz(4)	6	26	38	
			8 MHz	4	24	36	
			4 MHz	3	23	35	
			2 MHz	2	23	34	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

Figure 33. ACC_{LSI} versus temperature



6.3.10 PLL characteristics

The parameters given in *Table 33* and *Table 34* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

Table 33. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10(2)	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	120	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	-	48	MHz
f_{VCO_OUT}	PLL VCO output	-	192	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Table 36. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode V_{DD} = 3.3 V	-	12	-	

Table 37. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization results, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC® code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 41. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/120 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, peripheral clock disabled	0.1 to 30 MHz	25	dBµV
			30 to 130 MHz		
			130 MHz to 1GHz		
			SAE EMI Level	4	-
		V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, PLL spread spectrum enabled, peripheral clock disabled	0.1 to 30 MHz	28	dBµV
			30 to 130 MHz	26	
			130 MHz to 1GHz	22	
			SAE EMI level	4	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 42. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Guaranteed by characterization results, not tested in production.
2. On V_{BAT} pin, $V_{ESD(HBM)}$ is limited to 1000 V.

Table 47. I/O AC characteristics(1) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	12.5	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	50(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} >2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 40 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	100(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	50(3)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} > 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	10	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-3	6	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} > 2.70 V	-	-	100(3)	MHz
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	50(3)	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	120(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	100(3)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} > 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	6	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

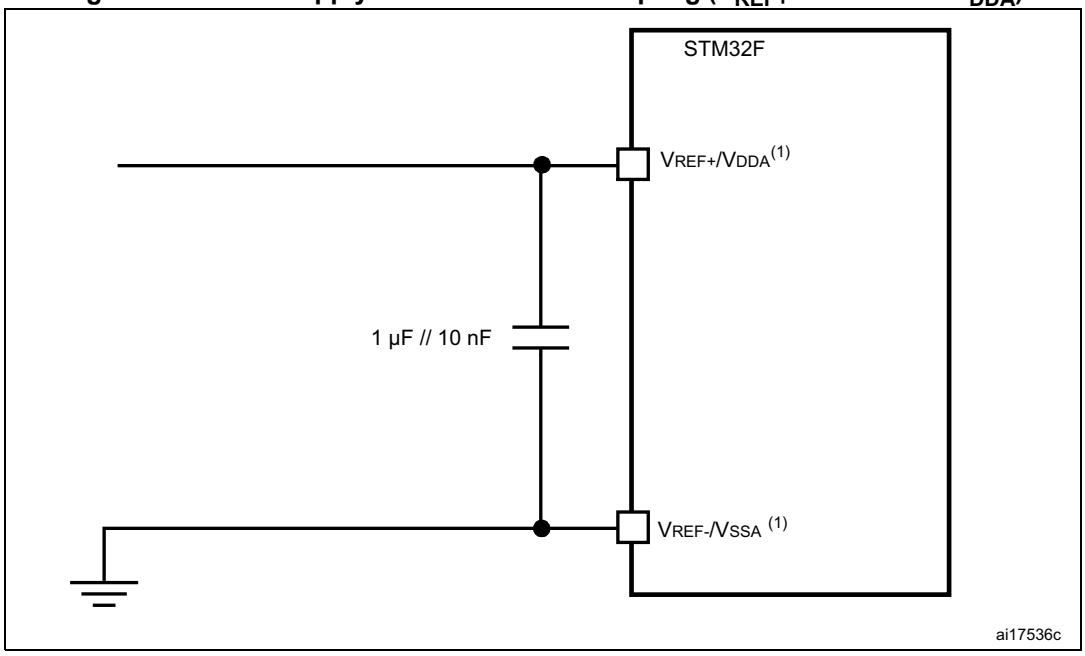
1. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F20/21xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
2. The maximum frequency is defined in *Figure 37*.
3. For maximum frequencies above 50 MHz and V_{DD} above 2.4 V, the compensation cell should be used.

Table 54. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master, 16-bit data, audio frequency = 48 kHz, main clock disabled	1.23	1.24	MHz
		Slave	0	$64F_S$ (1)	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 50 pF	-	(2)	ns
$t_{v(WS)}$ (3)	WS valid time	Master	0.3	-	
$t_{h(WS)}$ (3)	WS hold time	Master	0	-	
$t_{su(WS)}$ (3)	WS setup time	Slave	3	-	
$t_{h(WS)}$ (3)	WS hold time	Slave	0	-	
$t_{w(CKH)}$ (3) $t_{w(CKL)}$ (3)	CK high and low time	Master f_{PCLK}= 30 MHz	396	-	
$t_{su(SD\_MR)}$ (3) $t_{su(SD\_SR)}$ (3)	Data input setup time	Master receiver Slave receiver	45 0	-	
$t_{h(SD\_MR)}$ (3)(4) $t_{h(SD\_SR)}$ (3)(4)	Data input hold time	Master receiver: f_{PCLK}= 30 MHz, Slave receiver: f_{PCLK}= 30 MHz	13 0	-	
$t_{v(SD\_ST)}$ (3)(4)	Data output valid time	Slave transmitter (after enable edge)	-	30	
$t_{h(SD\_ST)}$ (3)	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD\_MT)}$ (3)(4)	Data output valid time	Master transmitter (after enable edge)	-	6	
$t_{h(SD\_MT)}$ (3)	Data output hold time	Master transmitter (after enable edge)	0	-	

1. F_S is the sampling frequency. Refer to the I2S section of the STM32F20xxx/21xxx reference manual for more details. f_{CK} values reflect only the digital peripheral behavior which leads to a minimum of (I2SDIV/(2*I2SDIV+ODD), a maximum of (I2SDIV+ODD)/(2*I2SDIV+ODD) and F_S maximum values for each mode/condition.
2. Refer to *Table 47: I/O AC characteristics*.
3. Guaranteed by design, not tested in production.
4. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PLCLK} =125 ns.

Figure 53. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



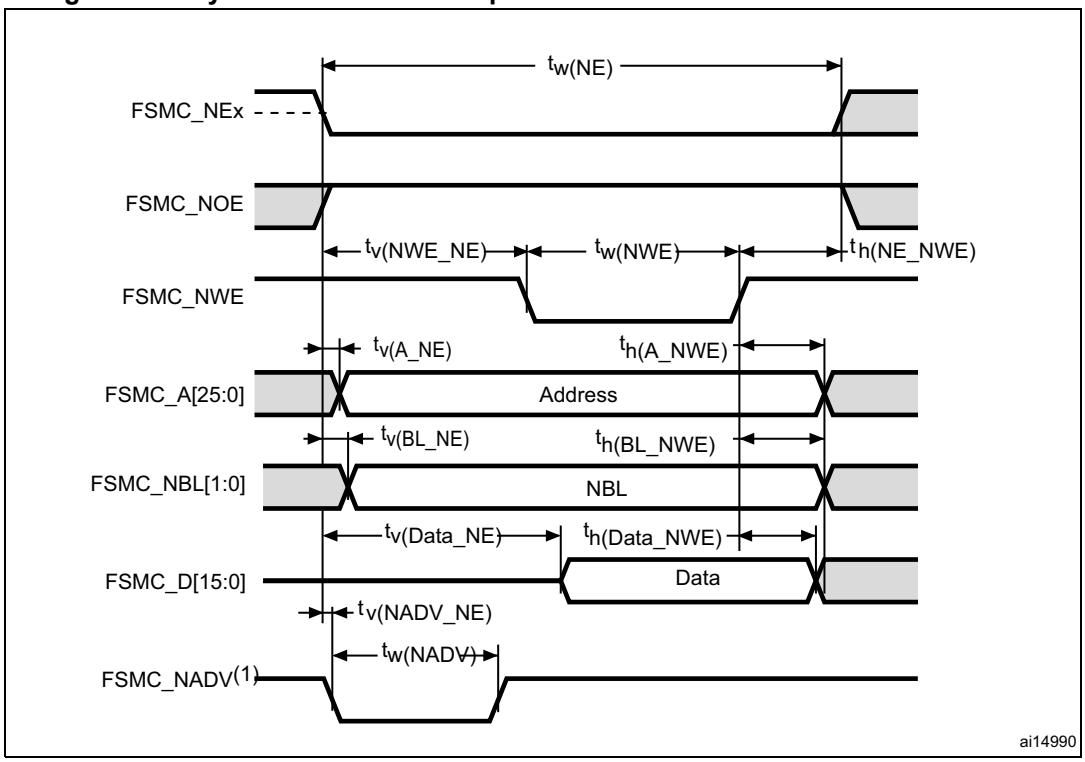
1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.21 DAC electrical characteristics

Table 67. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.8	-	3.6	V	-
V_{REF+}	Reference supply voltage	1.8	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.8 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	

Figure 56. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+4$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK}-0.5$	$T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$T_{HCLK}-0.5$	$T_{HCLK}+3$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK}-3$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK}-1$	-	ns
$t_{v(Data\_NE)}$	Data to FSMC_NEx low to Data valid	-	$T_{HCLK}+5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK}+1.5$	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Table 78. Synchronous non-multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	5	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	6	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	8	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	2	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	2	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

PC Card/CompactFlash controller waveforms and timings

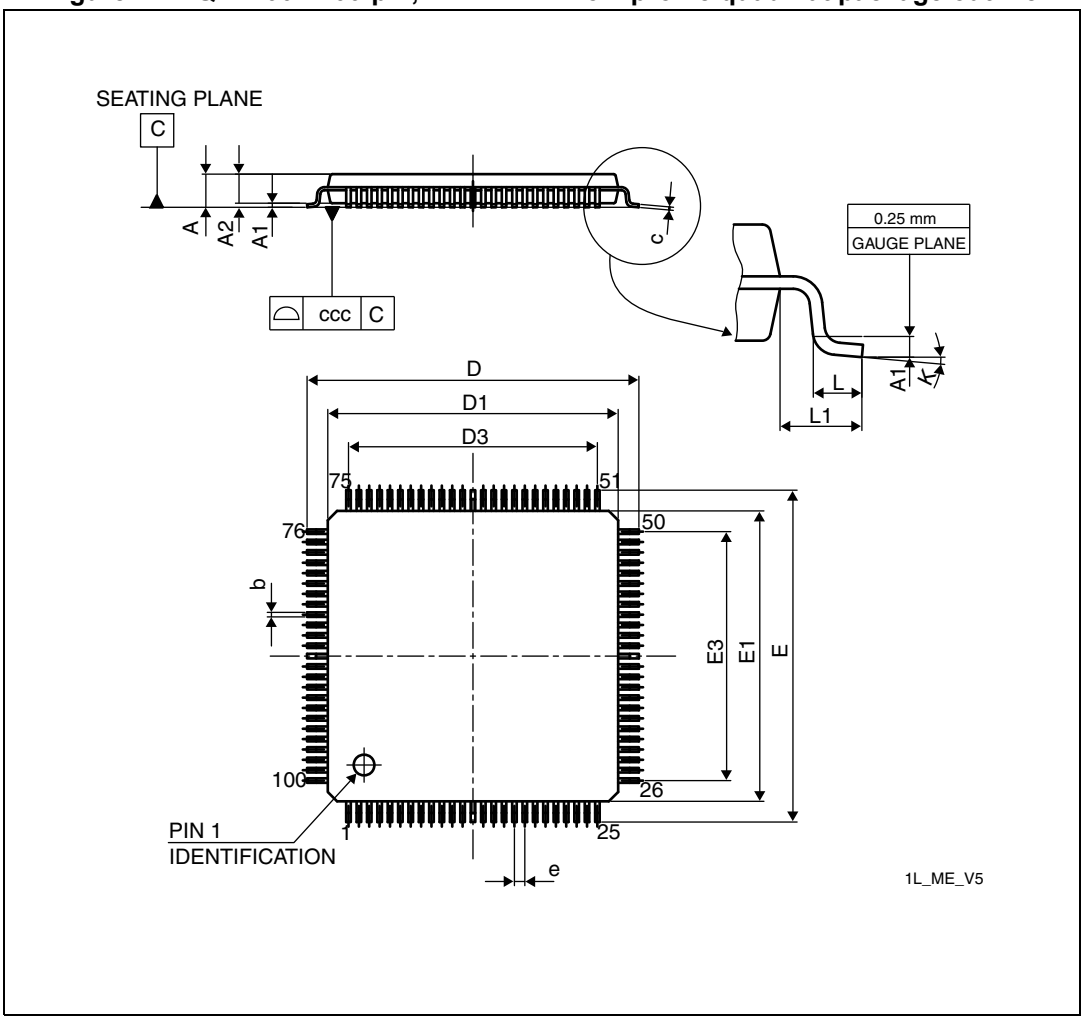
Figure 63 through *Figure 68* represent synchronous waveforms, with *Table 79* and *Table 80* providing the corresponding timings. The results shown in these table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

7.2 LQFP100 package information

Figure 77. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 87. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591

Table 94. Document revision history (continued)

Date	Revision	Changes
14-Jun-2011	5	Added SDIO in *Table 2: STM32F215xx and STM32F217xx: features and peripheral counts*. Updated V_{IN} for 5V tolerant pins in *Table 10: Voltage characteristics*. Updated jitter parameters description in *Table 33: Main PLL characteristics*. Remove jitter values for system clock in *Table 34: PLLI2S (audio PLL) characteristics*. Updated *Table 41: EMI characteristics*. Update *Note 2* in *Table 51: I2C characteristics*. Updated Avg_Slope typical value and T_{S_temp} minimum value in *Table 68: Temperature sensor characteristics*. Updated T_{S_vbat} minimum value in *Table 69: VBAT monitoring characteristics*. Updated $T_{S\_vrefint}$ minimum value in *Table 70: Embedded internal reference voltage*. Added Software option in *Section 8: Ordering information*. In *Table 93: Main applications versus package for STM32F2xxx microcontrollers*, renamed USB1 and USB2, USB OTG FS and USB OTG HS, respectively; and removed USB OTG FS and camera interface for 64-pin package; added USB OTG HS on 64-pin package; and added *Note 1* and *Note 2*. Updated disclaimer on cover page.