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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l051f3p6tr

2 Description

The low density value line STM8L05xxx devices are members of the STM8L ultra low power 8-bit family.

The value line STM8L05xxx ultra low power family features an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-Application debugging and ultra-fast Flash programming.

Low density value line STM8L05xxx microcontrollers feature embedded data EEPROM and low power, low-voltage, single-supply program Flash memory.

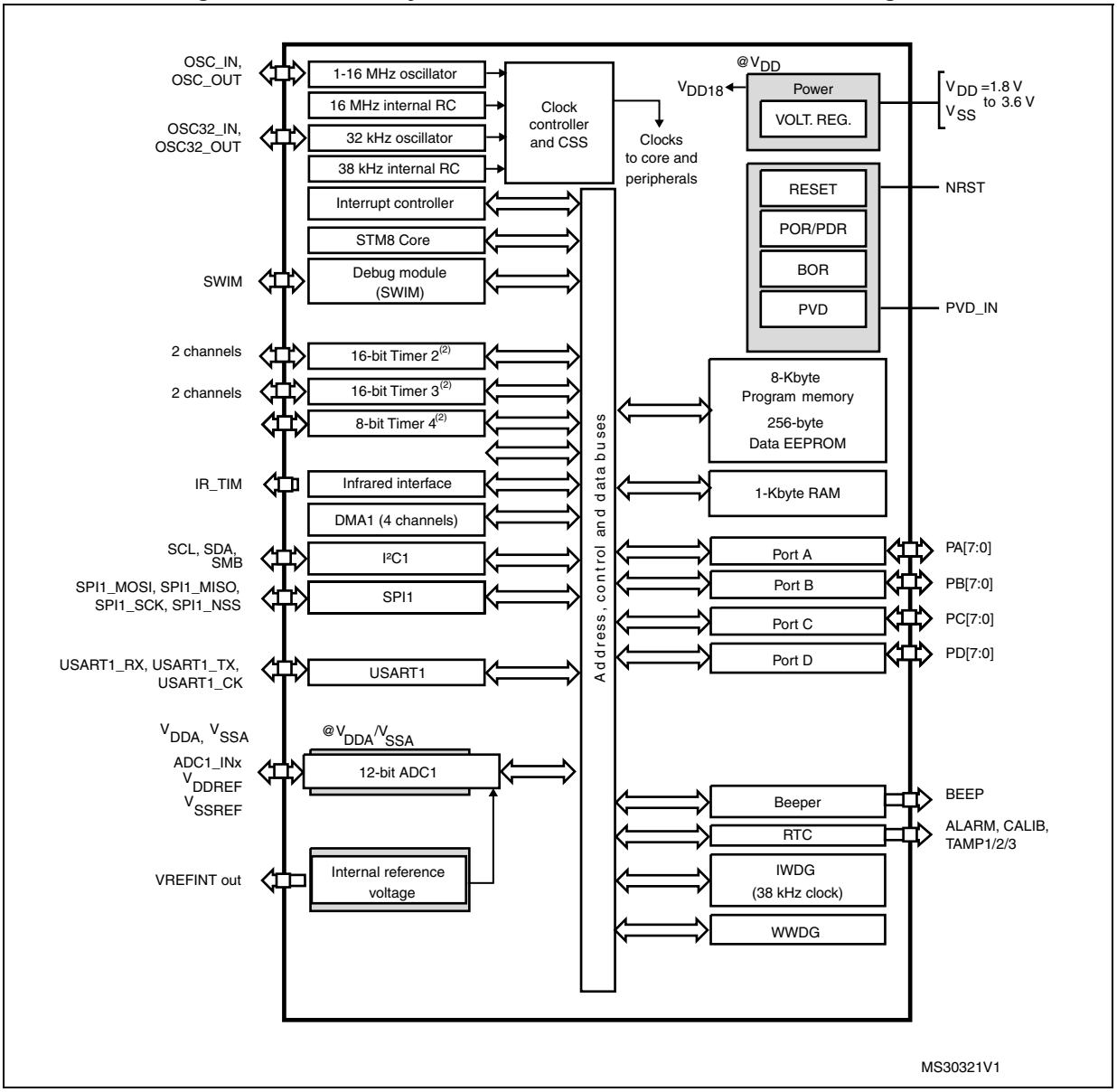
The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, a real-time clock, two 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as an SPI, an I^2C interface, and one USART.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

All value line STM8L ultra low power products are based on the same architecture with the same memory mapping and a coherent pinout.

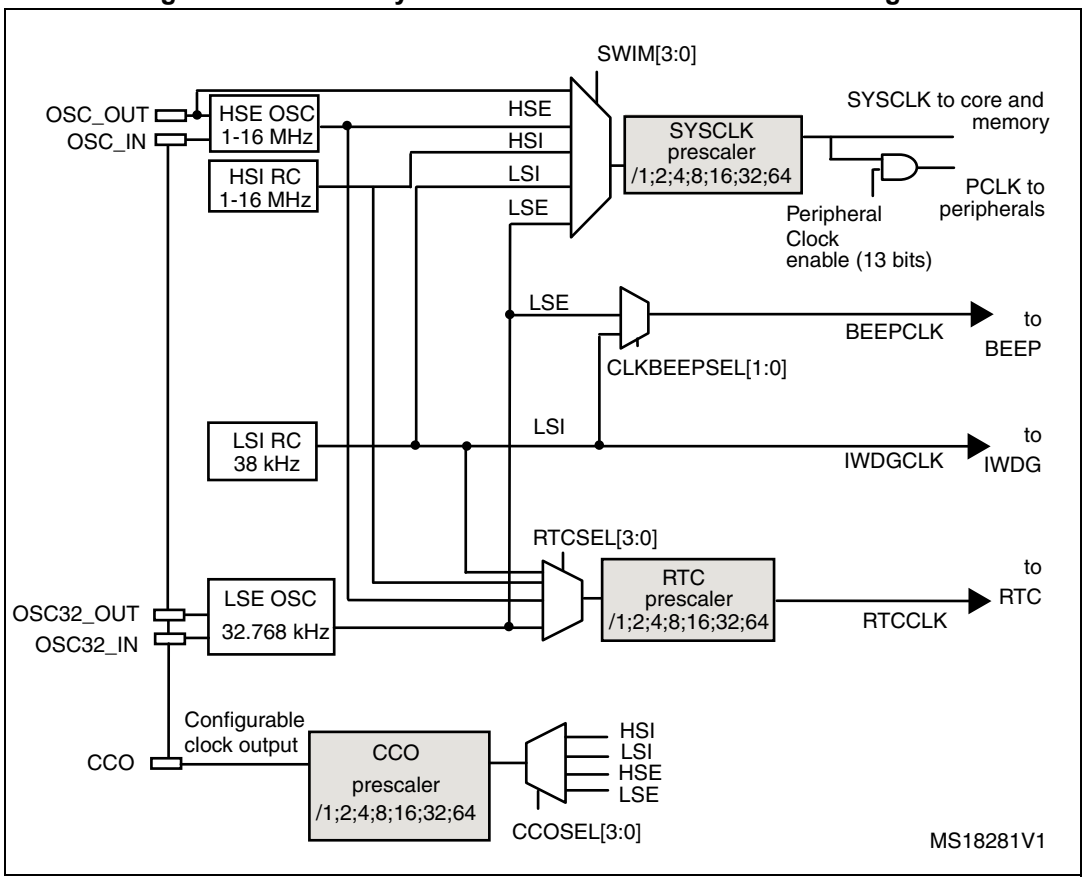
3 Functional overview

Figure 1. Low density value line STM8L05xxx device block diagram



1. **Legend**:
   ADC: Analog-to-digital converter
   BOR: Brownout reset
   DMA: Direct memory access
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent watchdog
   POR/PDR: Power-on reset / power-down reset
   RTC: Real-time clock
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   WWDG: Window watchdog

Figure 2. Low density value line STM8L05xxx clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to Section HSE clock in the STM8L15x and STM8L16x reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to Section LSE clock in the STM8L15x and STM8L16x reference manual (RM0031).

4 Pin description

Figure 3. STM8L051F3 20-pin TSSOP20 package pinout

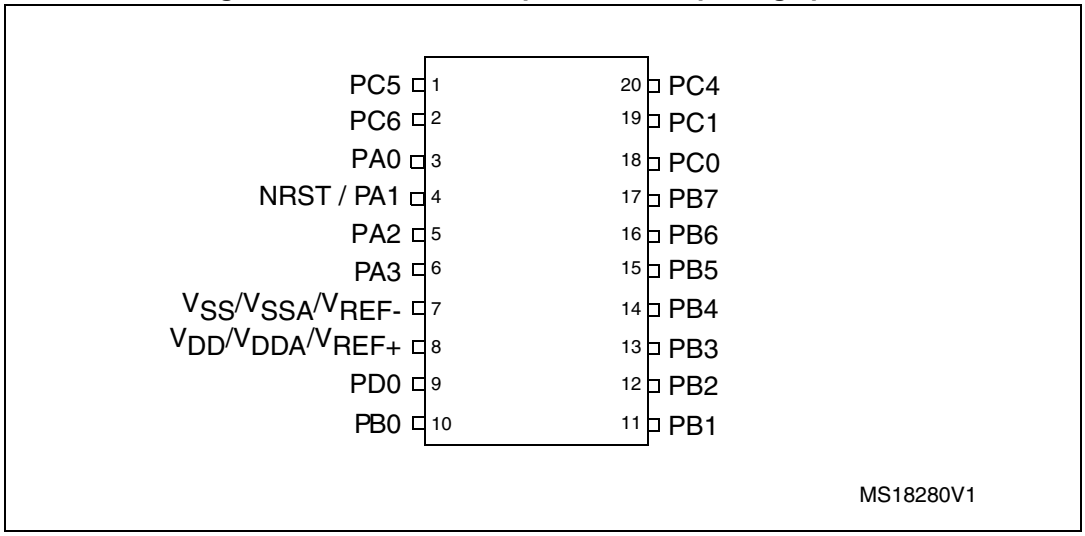


Table 3. Legend/abbreviation for *Table 4*

Type	I= input, O = output, S = power supply	
Level	Output	HS = high sink/source (20 mA)
	Input	FT - five volt tolerant
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 4. Low density value line STM8L05xxx pin description (continued)

pin n°	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
TSSOP20				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
2	PC6/OSC32_OUT/*[SPI_SCK]*(2) */[USART_RX]*/TIM2_CH2	I/O		**X**	X	X	HS	X	X	**Port C6**	LSE oscillator output */ [SPI clock] / [USART receive]/ Timer 2 -channel 2*
9	PD0/TIM3_CH2/*[ADC1_TRIG]*(2)/ADC1_IN22	I/O		**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22
8	V_{DD} / V_{DDA} / V_{REF+}	S								Digital supply voltage / ADC1 positive voltage reference	
7	V_{SS} / V_{REF-} / V_{SSA}									Ground voltage / ADC1 negative voltage reference / Analog ground voltage	
3	PA0(5)/*[USART_CK]*(2)/ SWIM/BEEP/IR_TIM (6)	I/O		X	**X**	X	HS (6)	X	X	**Port A0**	*[USART1 synchronous clock]*(2) / SWIM input and output / Beep output / Infrared Timer output

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15xxx and STM8L16xxx reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High Sink LED driver capability available on PA0.

Note: The slope control of all GPIO pins, except true open drain pins, can be programmed. By default, the slope control is limited to 2 MHz.

4.1 System configuration options

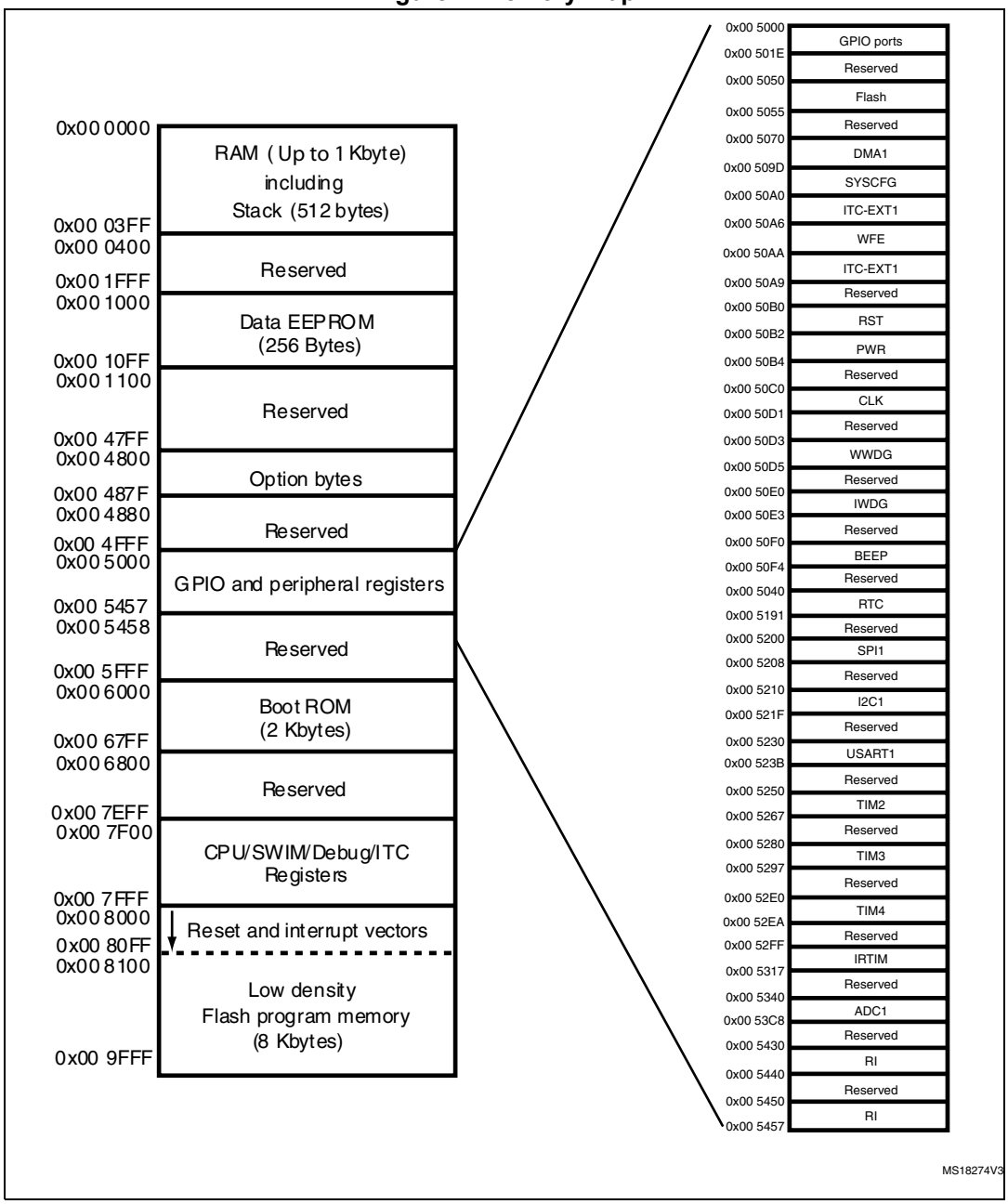
As shown in *Table 4: Low density value line STM8L05xxx pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in the STM8L15xx and STM8L16xx reference manual (RM0031).

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 4*.

Figure 4. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 507D to 0x00 507E	DMA1	Reserved area (2 bytes)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00
0x00 5084		Reserved area (1 byte)		
0x00 5085		DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088		Reserved area (2 bytes)		
0x00 5089		DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5098	DMA1	DMA_C3M0EAR	DMA channel 3 memory 0 extended address register	0x00
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509C		Reserved area (3 bytes)		
0x00 509D	SYSCFG	SYSCFG_RMPCR3	Remapping register 3	0x00
0x00 509E		SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9		WFE_CR4	WFE control register 4	0x00
0x00 50AA	ITC - EXTI	EXTI_CR4	External interrupt control register 4	0x00
0x00 50AB		EXTI_CONF2	External interrupt port select register 2	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_CKDIVR	CLK Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	CLK Clock RTC register	0x00(1)
0x00 50C2		CLK_ICKCR	CLK Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	CLK Peripheral clock gating register 1	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C4	CLK	CLK_PCKENR2	CLK Peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	CLK Configurable clock control register	0x00
0x00 50C6		CLK_ECKCR	CLK External clock control register	0x00
0x00 50C7		CLK_SCSR	CLK System clock status register	0x01
0x00 50C8		CLK_SWR	CLK System clock switch register	0x01
0x00 50C9		CLK_SWCR	CLK Clock switch control register	0xX0
0x00 50CA		CLK_CSSR	CLK Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	CLK Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	CLK HSI calibration register	0xXX
0x00 50CD		CLK_HSITRIMR	CLK HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	CLK HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	CLK Main regulator control status register	0bxx11 1 00X
0x00 50D0		CLK_PCKENR3	CLK Peripheral clock gating register 3	0x00
0x00 50D1 to 0x00 50D2	Reserved area (2 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0x01
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to0x00 513F	Reserved area (76 bytes)			
0x00 5140	RTC	RTC_TR1	RTC Time register 1	0x00
0x00 5141		RTC_TR2	RTC Time register 2	0x00
0x00 5142		RTC_TR3	RTC Time register 3	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5166	RTC	RTC_ALRMASSMSKR	RTC Alarm A masking register	0x00(1)
0x00 5167 to 0x00 5169		Reserved area (3 bytes)		
0x00 516A		RTC_CALRH	RTC Calibration register high	0x00(1)
0x00 516B		RTC_CALRL	RTC Calibration register low	0x00(1)
0x00 516C		RTC_TCR1	RTC Tamper control register 1	0x00(1)
0x00 516D		RTC_TCR2	RTC Tamper control register 2	0x00(1)
0x00 516E to 0x00 518A		Reserved area (36 bytes)		
0x00 5190		CSSLSE_CSR	CSS on LSE control and status register	0x00(1)
0x00 519A to 0x00 51FF	Reserved area (111 bytes)			
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		I2C1_OAR2	I2C1 own address register for dual mode	0x00
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0X
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53C8 to 0x00 542F	Reserved area(104 bytes)			
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	RI Timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	RI Timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	RI I/O input register 1	0xXX
0x00 5434		RI_IOIR2	RI I/O input register 2	0xXX
0x00 5435		RI_IOIR3	RI I/O input register 3	0xXX
0x00 5436		RI_IOCMR1	RI I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	RI I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	RI I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	RI I/O switch register 1	0x00
0x00 543A		RI_IOSR2	RI I/O switch register 2	0x00
0x00 543B		RI_IOSR3	RI I/O switch register 3	0x00
0x00 543C		RI_IOGCR	RI I/O group control register	0xFF
0x00 543D		RI_ASCR1	Analog switch register 1	0x00
0x00 543E		RI_ASCR2	RI Analog switch register 2	0x00
0x00 543F		RI_RCR	RI Resistor control register	0x00
0x00 5440 to 0x00 544F	Reserved area (16 bytes)			
0x00 5450	RI	RI_CR	RI I/O control register	0x00
0x00 5451		RI_MASKR1	RI I/O mask register 1	0x00
0x00 5452		RI_MASKR2	RI I/O mask register 2	0x00
0x00 5453		RI_MASKR3	RI I/O mask register 3	0x00
0x00 5454		RI_MASKR4	RI I/O mask register 4	0x00
0x00 5455		RI_IOIR4	RI I/O input register 4	0xXX
0x00 5456		RI_IOCMR4	RI I/O control mode register 4	0x00
0x00 5457		RI_IOSR4	RI I/O switch register 4	0x00

1. These registers are not impacted by a system reset. They are reset at power-on.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 10* for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L05x/15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 10. Option byte addresses

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x00
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

Table 17. Total current consumption in Run mode

Symbol	Para meter	Conditions(1)			Typ	Max		Unit
						55 °C	85 °C	
$I_{DD(RUN)}$	Supply current in run mode(2)	All peripherals OFF, code executed from RAM, V_{DD} from 1.8 V to 3.6 V	HSI RC osc. (16 MHz)(3)	f_{CPU} = 125 kHz	0.39	0.47	0.49	mA
				f_{CPU} = 1 MHz	0.48	0.56	0.58	
				f_{CPU} = 4 MHz	0.75	0.84	0.86	
				f_{CPU} = 8 MHz	1.10	1.20	1.25	
				f_{CPU} = 16 MHz	1.85	1.93	2.12(5)	
			HSE external clock (f_{CPU}=f_{HSE})(4)	f_{CPU} = 125 kHz	0.05	0.06	0.09	
				f_{CPU} = 1 MHz	0.18	0.19	0.20	
				f_{CPU} = 4 MHz	0.55	0.62	0.64	
				f_{CPU} = 8 MHz	0.99	1.20	1.21	
				f_{CPU} = 16 MHz	1.90	2.22	2.23(5)	
			LSI RC osc. (typ. 38 kHz)	f_{CPU} = f_{LSI}	0.040	0.045	0.046	
			LSE external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.035	0.040	0.048(5)	
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.8 V to 3.6 V	HSI RC osc.(6)	f_{CPU} = 125 kHz	0.43	0.55	0.56	mA
				f_{CPU} = 1 MHz	0.60	0.77	0.80	
				f_{CPU} = 4 MHz	1.11	1.34	1.37	
				f_{CPU} = 8 MHz	1.90	2.20	2.23	
				f_{CPU} = 16 MHz	3.8	4.60	4.75	
			HSE external clock (f_{CPU}=f_{HSE}) (4)	f_{CPU} = 125 kHz	0.30	0.36	0.39	
				f_{CPU} = 1 MHz	0.40	0.50	0.52	
				f_{CPU} = 4 MHz	1.15	1.31	1.40	
				f_{CPU} = 8 MHz	2.17	2.33	2.44	
				f_{CPU} = 16 MHz	4.0	4.46	4.52	
			LSI RC osc.	f_{CPU} = f_{LSI}	0.110	0.123	0.130	
			LSE ext. clock (32.768 kHz)(7)	f_{CPU} = f_{LSE}	0.100	0.101	0.104	

1. All peripherals OFF, V_{DD} from 1.8 V to 3.6 V, HSI internal RC osc. , f_{CPU}=f_{SYSCLK}
2. CPU executing typical data processing
3. The run from RAM consumption can be approximated with the linear formula: I_{DD}(run_from_RAM) = Freq * 90 µA/MHz + 380 µA

HSE crystal/ceramic resonator oscillator

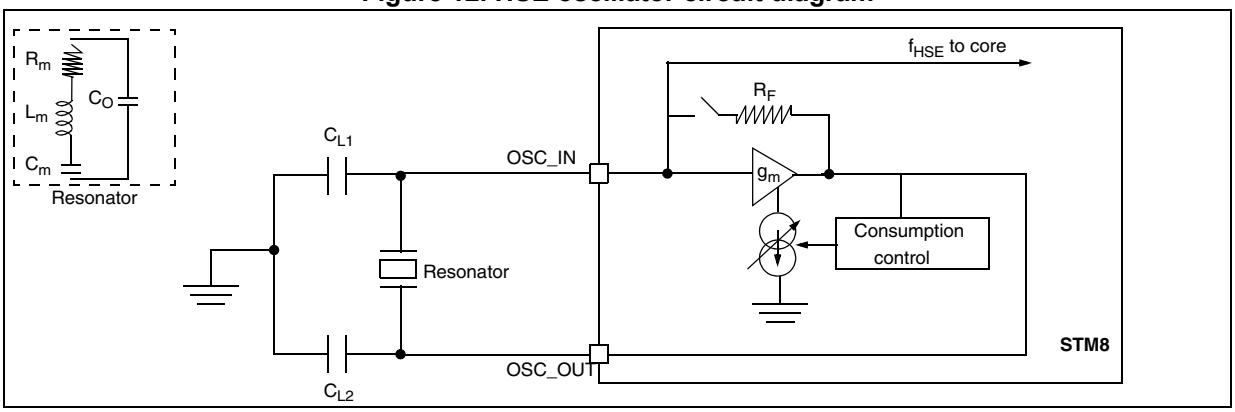
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 28. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High speed external oscillator frequency		1		16	MHz
R_F	Feedback resistor			200		kΩ
$C^{(1)}$	Recommended load capacitance (2)			20		pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz			2.5 (startup) 0.7 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz			2.5 (startup) 0.46 (stabilized)(3)	
g_m	Oscillator transconductance		3.5(3)			mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized		1		ms

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data guaranteed by Design. Not tested in production.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 12. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification), C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification), $C_{L1}=C_{L2}=C$: Grounded external capacitance
$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 29. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency			32.768		kHz
R_F	Feedback resistor	ΔV = 200 mV		1.2		MΩ
$C^{(1)}$	Recommended load capacitance (2)			8		pF
$I_{DD(LSE)}$	LSE oscillator power consumption				1.4(3)	µA
		V_{DD} = 1.8 V		450		nA
		V_{DD} = 3 V		600		
		V_{DD} = 3.6 V		750		
g_m	Oscillator transconductance		3(3)			µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized		1		s

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Data guaranteed by Design. Not tested in production.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 13. LSE oscillator circuit diagram

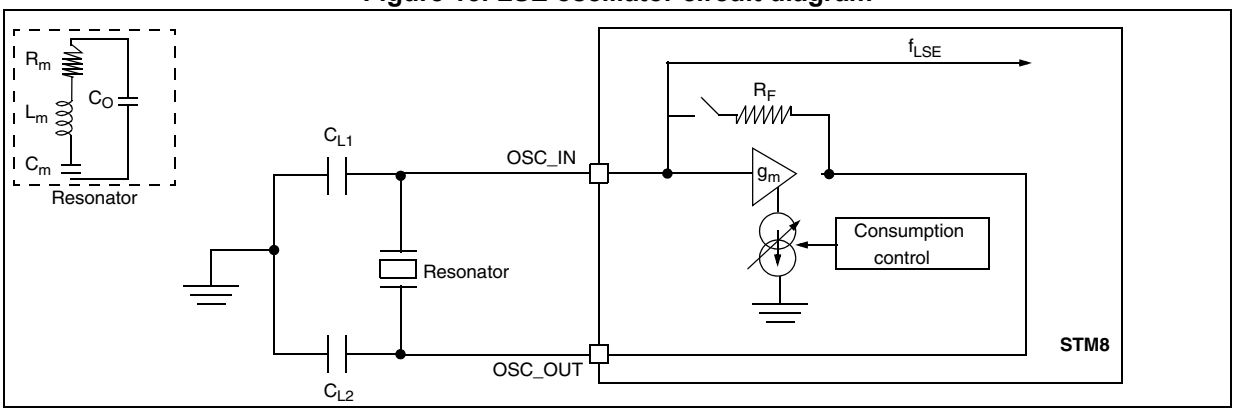


Figure 16. Typical V_{IL} and V_{IH} vs V_{DD} (high sink I/Os)

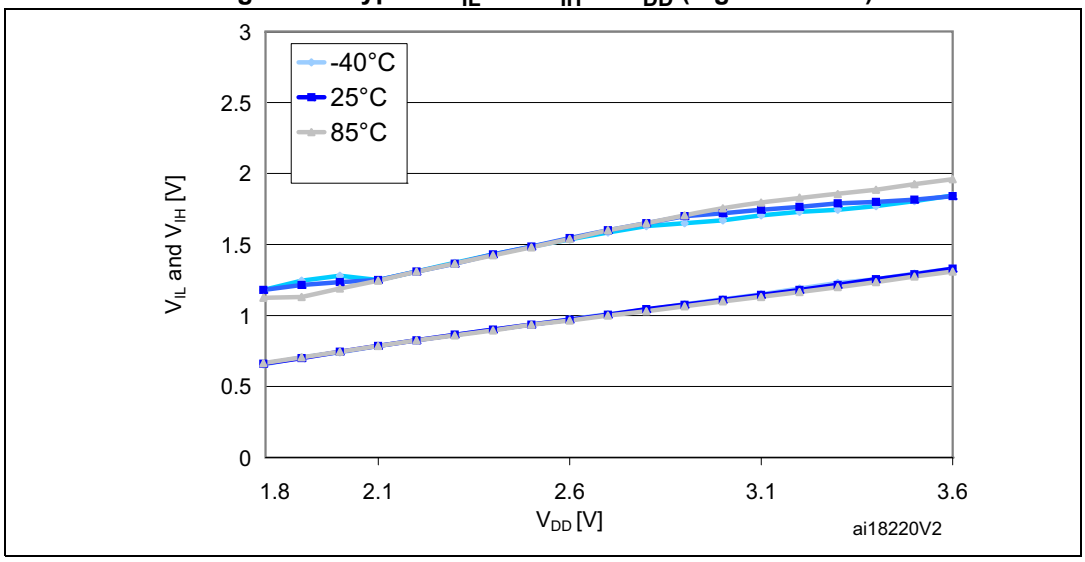


Figure 17. Typical V_{IL} and V_{IH} vs V_{DD} (true open drain I/Os)

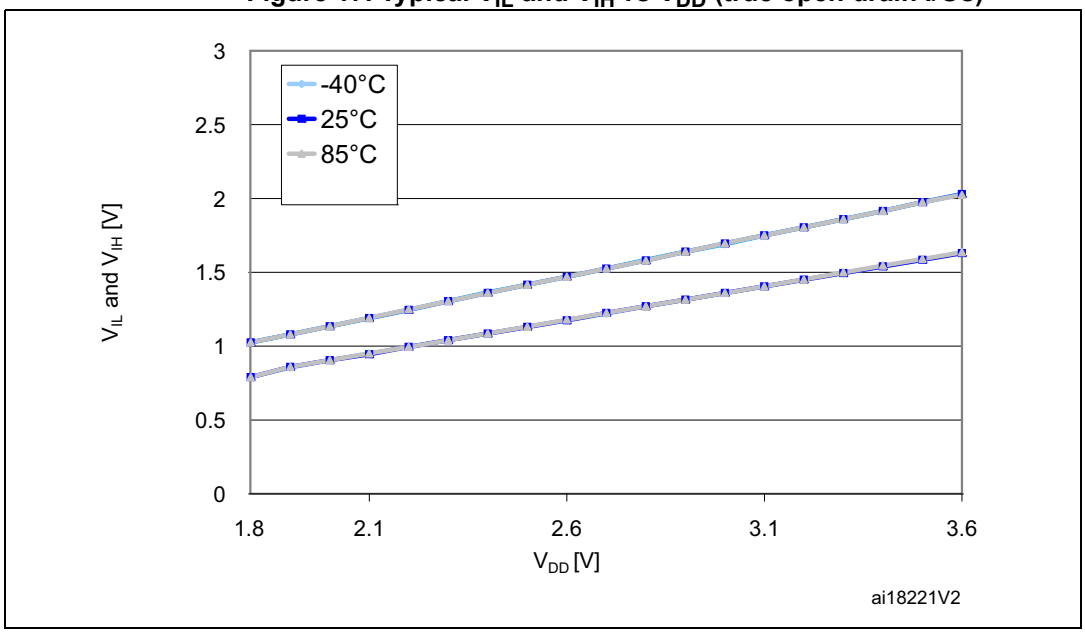


Table 43. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	V_{AIN} on PF0 fast channel V_{DDA} < 2.4 V	0.43(4)(5)			µs
		V_{AIN} on PF0 fast channel 2.4 V ≤V_{DDA}≤ 3.6 V	0.22(4)(5)			µs
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(4)(5)			µs
		V_{AIN} on slow channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.41(4)(5)			µs
t_{conv}	12-bit conversion time		12 + t_S			$1/f_{ADC}$
		16 MHz	1(4)			µs
t_{WKUP}	Wakeup time from OFF state				3	µs
t_{IDLE}(6)	Time before a new conversion	T_A = +25 °C			1(7)	s
		T_A = +70 °C			20(7)	ms
$t_{VREFINT}$	Internal reference voltage startup time				refer to *Table 42*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} or V_{DDA} must be tied to ground.
3. Guaranteed by design, not tested in production.
4. Minimum sampling and conversion time is reached for maximum Rext = 0.5 kΩ
5. Value obtained for continuous conversion on fast channel.
6. The time between 2 conversions, or between ADC ON and the first conversion must be lower than t_{IDLE}.
7. The t_{IDLE} maximum value is ∞on the “Z” revision code of the device.

In the following three tables, data is guaranteed by characterization result, not tested in production.

Table 44. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	LSB
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

Table 45. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

Table 46. ADC1 accuracy with V_{DDA} = V_{REF+} = 1.8 V to 2.4 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

9.2 Package mechanical data

9.2.1 20-lead thin shrink small package (TSSOP20)

Figure 38. TSSOP20 20-lead thin shrink small package outline

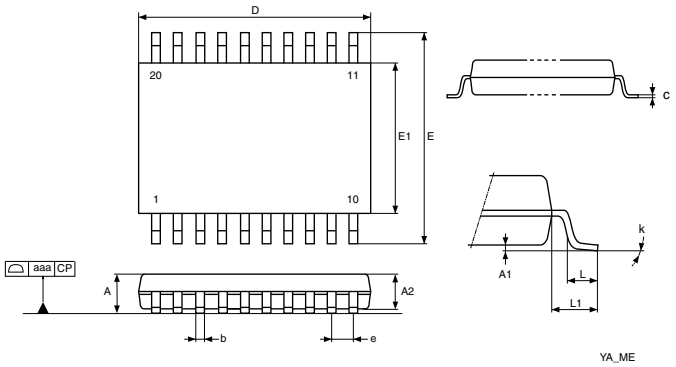
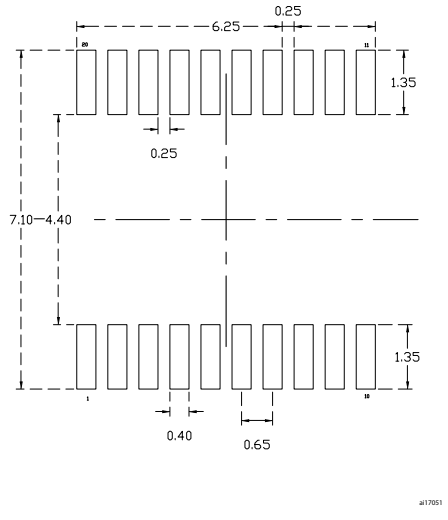


Figure 39. TSSOP20 recommended footprint



1. Drawing is not to scale
2. Dimensions are in millimeters

Table 52. TSSOP20 20-lead thin shrink small package, mechanical data

Dim.	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	-	-	1.200	-	-	0.0472
A1	-	0.050	0.150	-	0.0020	0.0059
A2	1	0.800	0.050	0.0394	0.0315	0.0413
b	-	0.190	0.300	-	0.0075	0.0118
c	-	0.090	0.200	-	0.0035	0.0079
D[2]	6.500	6.400	6.600	0.2559	0.2520	0.2598
E	6.400	6.200	6.600	0.252	0.2441	0.2598
E1[3]	4.400	4.300	4.500	0.1732	0.1693	0.1772
e	0.650	-	-	0.0256		-
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000	-	-	0.0394	-	-
k	-	0.0°	8.0°	-	0.0°	8.0°
aaa	-	-	0.1	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

9.3 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 15: General operating conditions on page 48*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 53. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20	110	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.