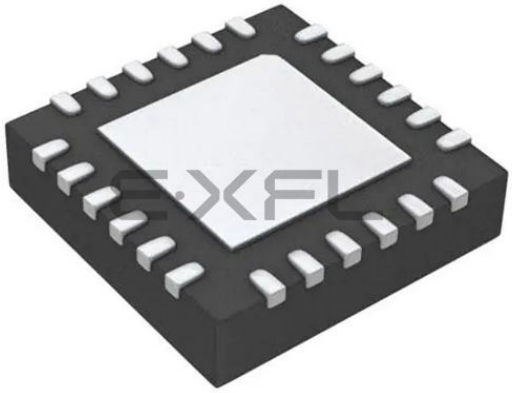

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb20f16g-a-qfn24

2. Ordering Information

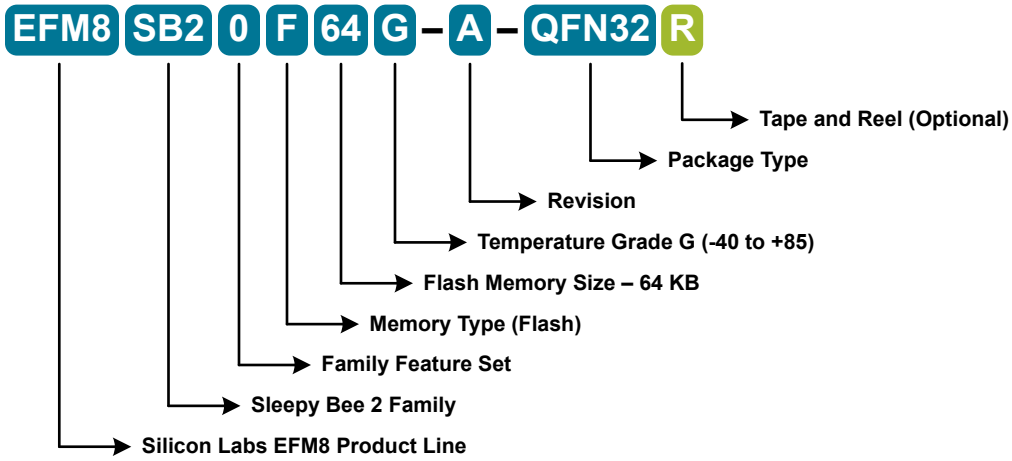

Figure 2.1. EFM8SB2 Part Numbering

All EFM8SB2 family members have the following features:

- CIP-51 Core running up to 25 MHz
- Three Internal Oscillators (24.5 MHz, 20 MHz, and 16 kHz)
- SMBus / I2C
- 2 x SPI
- UART
- 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 6-bit programmable current reference
- 10-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- Low-current 32 kHz oscillator and Real Time Clock
- 16-bit CRC Unit
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8SB2 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC Channels	Comparator Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8SB20F64G-A-QFN32	64	4352	24	23	12	Yes	-40 to +85 C	QFN32
EFM8SB20F64G-A-QFP32	64	4352	24	23	12	Yes	-40 to +85 C	QFP32
EFM8SB20F64G-A-QFN24	64	4352	16	15	8	Yes	-40 to +85 C	QFN24
EFM8SB20F32G-A-QFN32	32	4352	24	23	12	Yes	-40 to +85 C	QFN32
EFM8SB20F32G-A-QFP32	32	4352	24	23	12	Yes	-40 to +85 C	QFP32
EFM8SB20F32G-A-QFN24	32	4352	16	15	8	Yes	-40 to +85 C	QFN24

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC Channels	Comparator Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8SB20F16G-A-QFN24	16	4352	16	15	8	Yes	-40 to +85 C	QFN24

3. System Overview

3.1 Introduction

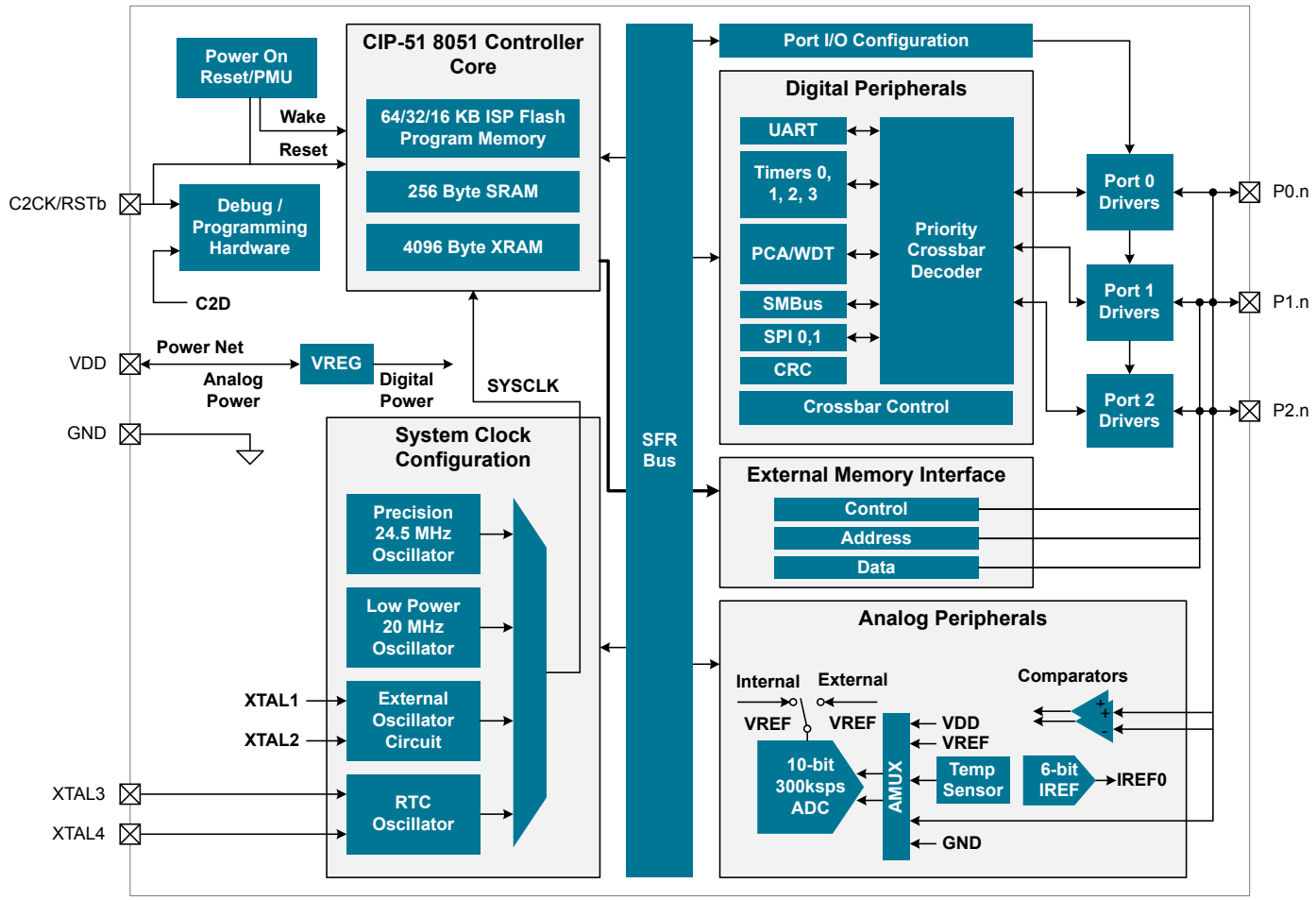

Figure 3.1. Detailed EFM8SB2 Block Diagram

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 8- or 9-bit data
- Automatic start and stop generation

Serial Peripheral Interface (SPI0 and SPI1)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to SYSCLK / 2 in master mode and SYSCLK / 10 in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock clock rate generator.
- Support for multiple masters on the same data lines.

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 10- and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 22 external inputs.
- Single-ended 10-bit mode.
- Supports an output update rate of 300 ksps samples per second.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal 1.65 V fast-settling reference and support for external reference.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 12 external positive inputs.
- Up to 11 external negative inputs.
- Additional input options:
  - Capacitive Sense Comparator output.
  - VDD.
  - VDD divided by 2.
  - Internal connection to LDO output.
  - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and +/-20 mV.
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 11, unless stated otherwise.

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	2.4	3.6	V
Minimum RAM Data Retention Voltage on VDD[1]	V_{RAM}	Not in Sleep Mode	—	1.4	—	V
		Sleep Mode	—	0.3	0.5	V
System Clock Frequency	f_{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C

Note:
1. All voltages with respect to GND.

Table 4.2. Power Consumption

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Digital Supply Current						
Normal Mode supply current - Full speed with code executing from flash [3, 4, 5]	I_{DD}	V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 24.5 MHz	—	4.1	5.0	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 20 MHz	—	3.5	—	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 32.768 kHz	—	90	—	µA
Normal Mode supply current frequency sensitivity[1, 3, 5]	I_{DDFREQ}	V_{DD} = 1.8–3.6 V, T = 25 °C, f_{SYSCLK} < 14 MHz	—	226	—	µA/MHz
		V_{DD} = 1.8–3.6 V, T = 25 °C, f_{SYSCLK} > 14 MHz	—	120	—	µA/MHz
Idle Mode supply current - Core halted with peripherals running[4, 6]	I_{DD}	V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 24.5 MHz	—	2.5	3.0	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 20 MHz	—	1.8	—	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 32.768 kHz	—	84	—	µA
Idle Mode Supply Current Frequency Sensitivity[1, 6]	I_{DDFREQ}	V_{DD} = 1.8–3.6 V, T = 25 °C	—	95	—	µA/MHz
Suspend Mode Supply Current	I_{DD}	V_{DD} = 1.8–3.6 V	—	77	—	µA
Sleep Mode Supply Current with RTC running from 32.768 kHz crystal	I_{DD}	1.8 V, T = 25 °C	—	0.60	—	µA
		3.6 V, T = 25 °C	—	0.85	—	µA
		1.8 V, T = 85 °C	—	1.30	—	µA
		3.6 V, T = 85 °C	—	1.90	—	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Units

Note:

1. Based on device characterization data; Not production tested.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp $” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 128-byte flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 128-byte address boundaries.
4. Includes supply current from regulator and oscillator source (24.5 MHz high-frequency oscillator, 20 MHz low-power oscillator, or 32.768 kHz RTC oscillator).
5. IDD can be estimated for frequencies < 10 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 90 µA. When using these numbers to estimate I_{DD} for > 10 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 4.1 mA – (25 MHz – 20 MHz) x 0.120 mA/MHz = 3.5 mA assuming the same oscillator setting.
6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 2.5 mA – (25 MHz – 5 MHz) x 0.095 mA/MHz = 0.6 mA.
7. ADC0 always-on power excludes internal reference supply current.
8. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
9. IREF0 supply current only. Does not include current sourced or sunk from IREF0 output pin.

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}	Reset Trigger	1.7	1.75	1.8	V
	V_{WARN}	Early Warning	1.8	1.85	1.9	V
VDD Supply Monitor Turn-On Time	t_{MON}		—	300	—	ns
Power-On Reset (POR) Monitor Threshold	V_{POR}	Initial Power-On (Rising Voltage on V_{DD})	—	0.75	—	V
		Falling Voltage on V_{DD}	0.7	0.8	0.9	V
		Brownout Recovery (Rising Voltage on V_{DD})	—	0.95	—	V
V_{DD} Ramp Time	t_{RMP}	Time to V_{DD} ≥ 1.8 V	—	—	3	ms
Reset Delay	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} > 1 MHz	100	650	1000	µs
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7	10	kHz

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1]	t_{WRITE}	One Byte	57	64	71	µs
Erase Time[1]	t_{ERASE}	One Page	28	32	36	ms

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}			10		Bits
Throughput Rate	f_S		—	—	300	ksps
Tracking Time	t_{TRK}		1.5	—	—	µs
Power-On Time	t_{PWR}		1.5	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode,	—	—	8.33	MHz
Conversion Time	T_{CNV}		13	—	—	Clocks
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	30	—	pF
		Gain = 0.5	—	28	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	5	—	kΩ
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	2 x V_{REF}	V
Power Supply Rejection Ratio	$PSRR_{ADC}$	Internal High Speed VREF	—	67	—	dB
		External VREF	—	74	—	dB
DC Performance						
Integral Nonlinearity	INL		—	±0.5	±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Offset Error	E_{OFF}	VREF = 1.65 V	–2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M		—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput						
Signal-to-Noise	SNR		54	58	—	dB
Signal-to-Noise Plus Distortion	SNDR		54	58	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD		—	-73	—	dB
Spurious-Free Dynamic Range	SFDR		—	75	—	dB

Note:
1. Absolute input pin voltage is limited by the V_{DD} supply.

Table 4.10. Voltage References

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}		1.60	1.65	1.70	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{VREFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-chip Precision Reference						
Output Voltage	V_{REFP}		1.645	1.68	1.715	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 µF tantalum + 0.1 µF ceramic bypass on VREF pin	—	15	—	ms
		0.1 µF ceramic bypass on VREF pin	—	300	—	µs
		No bypass on VREF pin	—	25	—	µs
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to GND	—	400	—	µV / µA
Short-circuit current	ISC_{VREFP}		—	3.5	—	mA
Power Supply Rejection	$PSRR_{VREFP}$		—	140	—	ppm/V
External Reference						
Input Voltage	V_{EXTREF}		1	—	V_{DD}	V
Input Current	I_{EXTREF}	Sample Rate = 300 ksps; VREF = 3.0 V	—	5.25	—	µA

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	940	—	mV
Offset Error[1]	E_{OFF}	T_A = 0 °C	—	18	—	mV
Slope	M		—	3.40	—	mV/°C
Slope Error[1]	E_M		—	40	—	µV/°C
Linearity			—	±1	—	°C
Turn-on Time	t_{PWR}		—	1.8	—	µs

Note:
1. Represents one standard deviation from the mean.

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	130	—	ns
		–100 mV Differential	—	200	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.75	—	µs
		–100 mV Differential	—	6.2	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysterisis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysterisis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	–8	—	mV
		CPHYN = 10	—	–16	—	mV
		CPHYN = 11	—	–32	—	mV
Positive Hysterisis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysterisis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	–6	—	mV
		CPHYN = 10	—	–12	—	mV
		CPHYN = 11	—	–24	—	mV
Positive Hysterisis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysterisis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	–4.5	—	mV
		CPHYN = 10	—	–9	—	mV
		CPHYN = 11	—	–18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	–4	—	mV
		CPHYN = 10	—	–8	—	mV
		CPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		-0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}		—	12	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P1.5	Multifunction I/O	Yes	P1MAT.5 EMIF_AD5	ADC0.13 CMP0N.6 CMP1N.6
20	P1.4	Multifunction I/O	Yes	P1MAT.4 EMIF_AD4	ADC0.12 CMP0P.6 CMP1P.6
21	P1.3	Multifunction I/O	Yes	P1MAT.3 SPI1_NSS EMIF_AD3	ADC0.11 CMP0N.5 CMP1N.5
22	P1.2	Multifunction I/O	Yes	P1MAT.2 SPI1_MOSI EMIF_AD2	ADC0.10 CMP0P.5 CMP1P.5
23	P1.1	Multifunction I/O	Yes	P1MAT.1 SPI1_MISO EMIF_AD1	ADC0.9 CMP0N.4 CMP1N.4
24	P1.0	Multifunction I/O	Yes	P1MAT.0 SPI1_SCK EMIF_AD0	ADC0.8 CMP0P.4 CMP1P.4
25	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 IREF0 CMP0N.3 CMP1N.3
26	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.3 CMP1P.3
27	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0N.2 CMP1N.2
28	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.2 CMP1P.2
29	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 XTAL2 CMP0N.1 CMP1N.1

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0N.2 CMP1N.2
20	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.2 CMP1P.2
21	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 XTAL2 CMP0N.1 CMP1N.1
22	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.1 CMP1P.1 XTAL1
23	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 AGND CMP0N.0 CMP1N.0
24	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP1P.0 VREF
Center	GND	Ground			

6.3 EFM8SB2x-QFP32 Pin Definitions

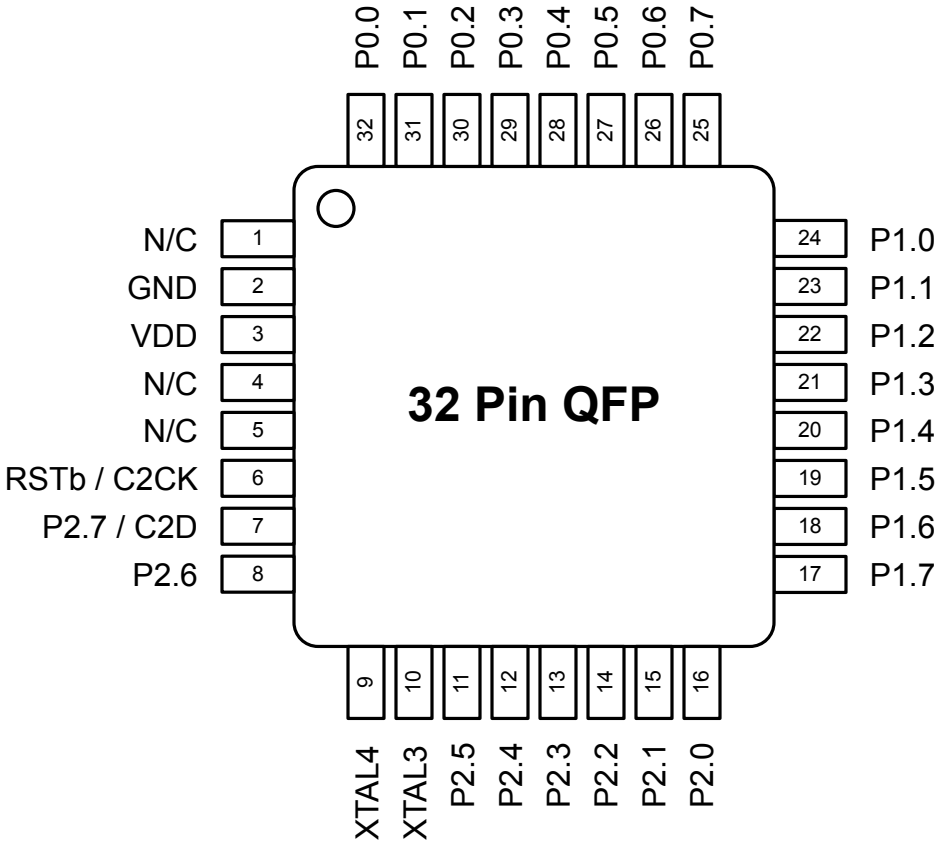

Figure 6.3. EFM8SB2x-QFP32 Pinout

Table 6.3. Pin Definitions for EFM8SB2x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	GND	Ground			
3	VDD	Supply Power Input			
4	N/C	No Connection			
5	N/C	No Connection			
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
8	P2.6	Multifunction I/O	Yes	EMIF_WRb	ADC0.22 CMP0P.11 CMP1P.11
9	XTAL4	RTC Crystal			XTAL4
10	XTAL3	RTC Crystal			XTAL3
11	P2.5	Multifunction I/O	Yes	EMIF_RDb	ADC0.21 CMP0N.10 CMP1N.10
12	P2.4	Multifunction I/O	Yes	EMIF_ALE	ADC0.20 CMP0P.10 CMP1P.10
13	P2.3	Multifunction I/O	Yes	EMIF_A11	ADC0.19 CMP0N.9 CMP1N.9
14	P2.2	Multifunction I/O	Yes	EMIF_A10	ADC0.18 CMP0P.9 CMP1P.9
15	P2.1	Multifunction I/O	Yes	EMIF_A9	ADC0.17 CMP0N.8 CMP1N.8
16	P2.0	Multifunction I/O	Yes	EMIF_A8	ADC0.16 CMP0P.8 CMP1P.8
17	P1.7	Multifunction I/O	Yes	P1MAT.7 EMIF_AD7	ADC0.15 CMP0N.7 CMP1N.7
18	P1.6	Multifunction I/O	Yes	P1MAT.6 EMIF_AD6	ADC0.14 CMP0P.7 CMP1P.7
19	P1.5	Multifunction I/O	Yes	P1MAT.5 EMIF_AD5	ADC0.13 CMP0N.6 CMP1N.6
20	P1.4	Multifunction I/O	Yes	P1MAT.4 EMIF_AD4	ADC0.12 CMP0P.6 CMP1P.6

7.2 QFN32 PCB Land Pattern

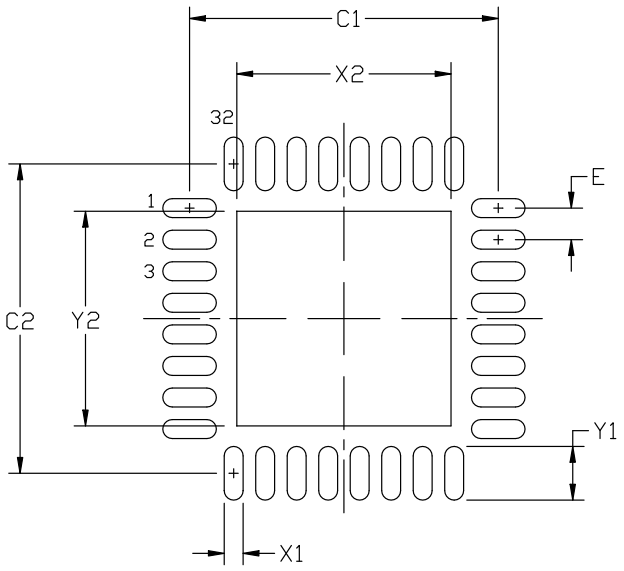

Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.3 QFN32 Package Marking

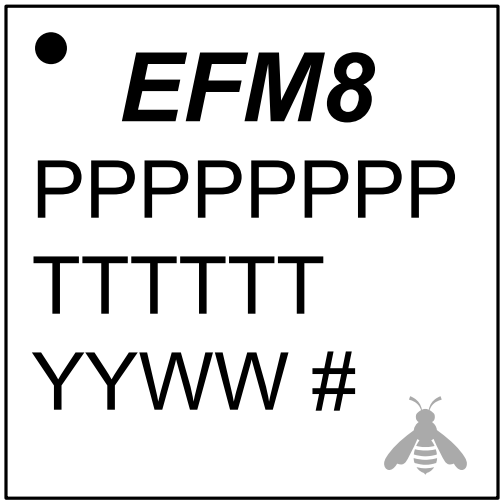

Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
Z	—	0.24	—
Y	—	0.18	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 QFN24 Package Marking

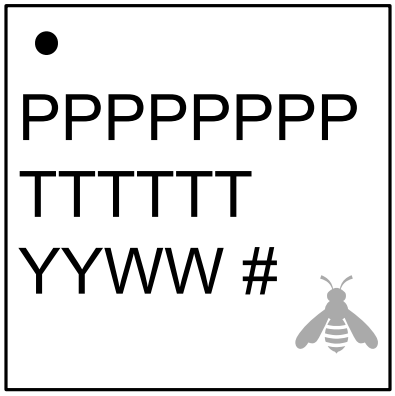

Figure 8.3. QFN24 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Typ	Max
bbb		0.20	
ccc		0.10	
ddd		0.20	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.3 QFP32 Package Marking

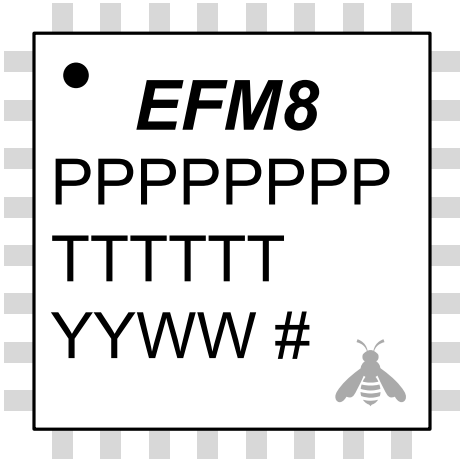

Figure 9.3. QFP32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).