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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 23x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb20f32g-a-qfn32

3. System Overview

3.1 Introduction

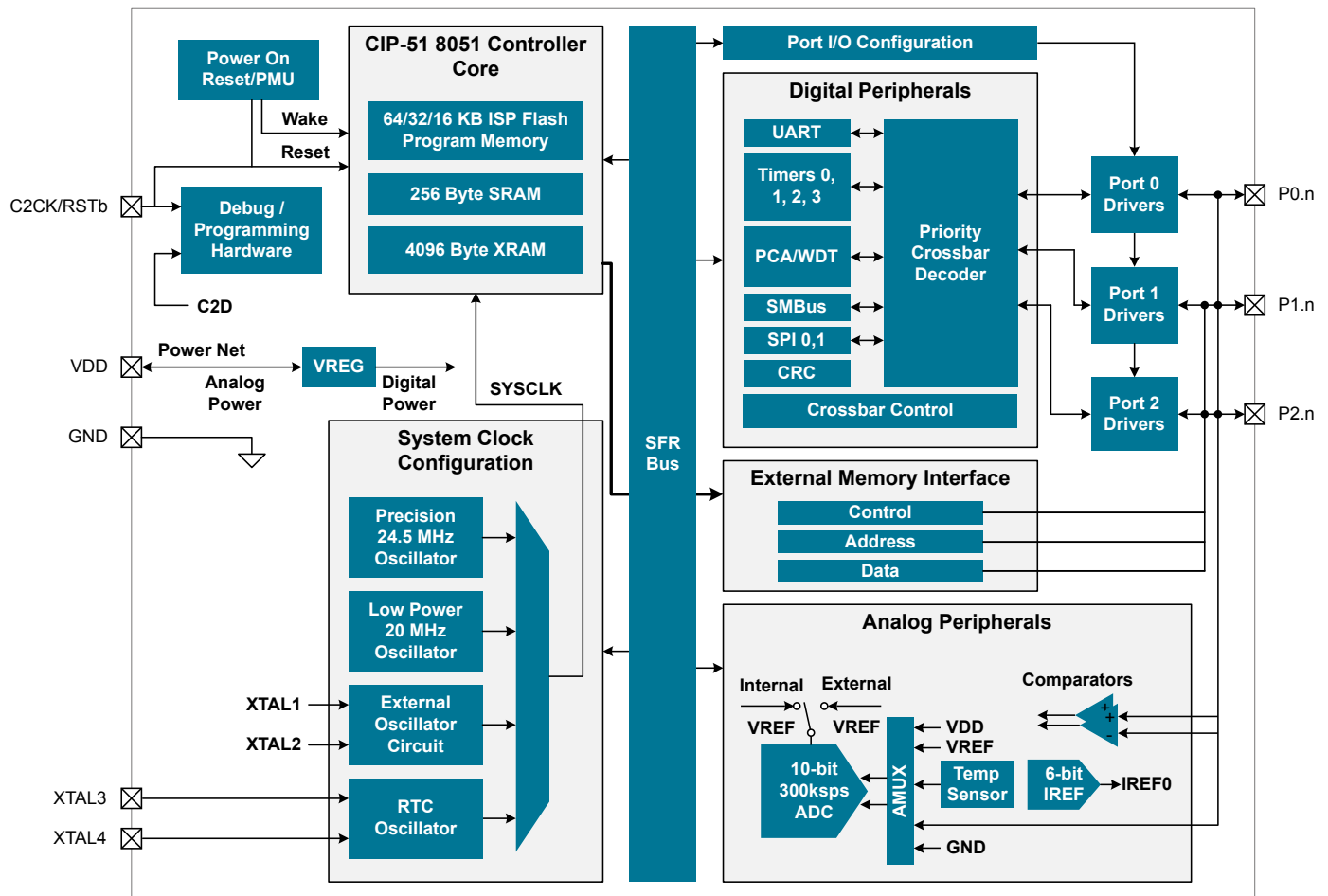


Figure 3.1. Detailed EFM8SB2 Block Diagram

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	- Core halted - All peripherals clocked and fully operational - Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	- Core and digital peripherals halted - Internal oscillators disabled - Code resumes execution on wake event	- Switch SYSCLK to HFOSC0 or LPOSC0 - Set SUSPEND bit in PMU0CF	- RTC0 Alarm Event - RTC0 Fail Event - Port Match Event - Comparator 0 Rising Edge
Sleep	- Most internal power nets shut down - Select circuits remain powered - Pins retain state - All RAM and SFRs retain state - Code resumes execution on wake event	- Disable unused analog peripherals - Set SLEEP bit in PMU0CF	- RTC0 Alarm Event - RTC0 Fail Event - Port Match Event - Comparator 0 Rising Edge

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.6 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pin P2.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.7.

- Up to 24 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each pin.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 20 MHz low power oscillator divided by 8.

- Provides clock to core and peripherals.
- 20 MHz low power oscillator (LPOSC0), accurate to +/- 10% over supply and temperature corners.
- 24.5 MHz internal oscillator (HFOSC0), accurate to +/- 2% over supply and temperature corners.
- External RTC 32 kHz crystal.
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

External Memory Interface (EMIF0)

The External Memory Interface (EMIF) enables access of off-chip memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) with the target address specified in either 8-bit or 16-bit formats.

- Supports multiplexed memory access.
- Four external memory modes:
 - Internal only.
 - Split mode without bank select.
 - Split mode with bank select.
 - External only
- Configurable ALE (address latch enable) timing.
- Configurable address setup and hold times.
- Configurable write and read pulse widths.

16/32-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit or 32-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module includes the following features:

- Support for CCITT-16 polynomial (0x1021).
- Support for CRC-32 polynomial (0x04C11DB7).
- Byte-level bit reversal.
- Automatic CRC of flash contents on one or more 1024-byte blocks.
- Initial seed selection of 0x0000/0x00000000 or 0xFFFF/0xFFFFFFFF.

3.7 Analog

Programmable Current Reference (IREF0)

The programmable current reference (IREF0) module enables current source or sink with two output current settings: Low Power Mode and High Current Mode. The maximum current output in Low Power Mode is 63 μA (1 μA steps) and the maximum current output in High Current Mode is 504 μA (8 μA steps).

The IREF module includes the following features:

- Capable of sourcing or sinking current in programmable steps.
- Two operational modes: Low Power Mode and High Current Mode.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sleep Mode Supply Current (RTC off)	I_{DD}	1.8 V, T = 25 °C	—	0.05	—	μA
		3.6 V, T = 25 °C	—	0.12	—	μA
		1.8 V, T = 85 °C	—	0.75	—	μA
		3.6 V, T = 85 °C	—	1.20	—	μA
V _{DD} Monitor Supply Current	I_{VMON}		—	7	—	μA
Oscillator Supply Current	I_{HFOSC0}	25 °C	—	300	—	μA
ADC0 Always-on Power Supply Current ⁷	I_{ADC}	300 ksp/s V _{DD} = 3.0 V	—	800	—	μA
		Tracking V _{DD} = 3.0 V	—	680	—	μA
Comparator 0 (CMP0) Supply Current	I_{CMP}	CPMD = 11	—	0.4	—	μA
		CPMD = 10	—	2.6	—	μA
		CPMD = 01	—	8.8	—	μA
		CPMD = 00	—	23	—	μA
Internal Fast-settling 1.65V ADC0 Reference, Always-on ⁸	I_{VREFFS}		—	200	—	μA
On-chip Precision Reference	I_{VREFP}		—	15	—	μA
Temp sensor Supply Current	I_{TSENSE}		—	35	—	μA
Programmable Current Reference (IREF0) Supply Current ⁹	I_{IREF}	Current Source, Either Power Mode, Any Output Code	—	10	—	μA
		Low Power Mode, Current Sink IREF0DAT = 000001	—	1	—	μA
		Low Power Mode, Current Sink IREF0DAT = 111111	—	11	—	μA
		High Current Mode, Current Sink IREF0DAT = 000001	—	12	—	μA
		High Current Mode, Current Sink IREF0DAT = 111111	—	81	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Endurance (Write/Erase Cycles)	N_{WE}		1 k	30 k	—	Cycles
Note: 1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles. 2. Data Retention Information is published in the Quarterly Quality and Reliability Report.						

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{SUS-PENDWK}$	CLKDIV = 0x00 Precision Osc.	—	400	—	ns
		CLKDIV = 0x00 Low Power Osc.	—	1.3	—	μ s
Sleep Mode Wake-up Time	$t_{SLEEPWK}$		—	2	—	μ s

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Low Power Oscillator (20 MHz)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	18	20	22	MHz
RTC in Self-Oscillate Mode						
Oscillator Frequency	f_{LFOSC}	Bias Off	—	12 $\pm$ 5	—	kHz
		Bias On	—	25 $\pm$ 10	—	kHz

Table 4.7. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	-	25	MHz

Table 4.8. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		18	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		18	—	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Offset Tempco	TC_{OFF}		—	3.5	—	$\mu V/^{\circ}C$

Table 4.13. Programmable Current Reference (IREF0)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Performance						
Resolution	N_{bits}		6			bits
Output Compliance Range	V_{IOUT}	Low Power Mode, Source	0	—	$V_{DD} - 0.4$	V
		High Current Mode, Source	0	—	$V_{DD} - 0.8$	V
		Low Power Mode, Sink	0.3	—	V_{DD}	V
		High Current Mode, Sink	0.8	—	V_{DD}	V
Integral Nonlinearity	INL		—	$<\pm 0.2$	± 1.0	LSB
Differential Nonlinearity	DNL		—	$<\pm 0.2$	± 1.0	LSB
Offset Error	E_{OFF}		—	$<\pm 0.1$	± 0.5	LSB
Full Scale Error	E_{FS}	Low Power Mode, Source	—	—	± 5	%
		High Current Mode, Source	—	—	± 6	%
		Low Power Mode, Sink	—	—	± 8	%
		High Current Mode, Sink	—	—	± 8	%
Absolute Current Error	E_{ABS}	Low Power Mode Sourcing 20 μA	—	$<\pm 1$	± 3	%
Dynamic Performance						
Output Settling Time to 1/2 LSB	t_{SETTLE}		—	300	—	ns
Startup Time	t_{PWR}		—	1	—	μs
Note: 1. The PCA block may be used to improve IREF0 resolution by PWMing the two LSBs.						

Table 4.14. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	$I_{OH} = -3 \text{ mA}$	$V_{DD} - 0.7$	—	—	V
Output Low Voltage (High Drive)	V_{OL}	$I_{OL} = 8.5 \text{ mA}$	—	—	0.6	V
Output High Voltage (Low Drive)	V_{OH}	$I_{OH} = -1 \text{ mA}$	$V_{DD} - 0.7$	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	$I_{OL} = 1.4 \text{ mA}$	—	—	0.6	V
Input High Voltage	V_{IH}	$V_{DD} = 2.0 \text{ to } 3.6 \text{ V}$	$V_{DD} - 0.6$	—	—	V
		$V_{DD} = 1.8 \text{ to } 2.0 \text{ V}$	$0.7 \times V_{DD}$	—	—	V
Input Low Voltage	V_{IL}	$V_{DD} = 2.0 \text{ to } 3.6 \text{ V}$	—	—	0.6	V
		$V_{DD} = 1.8 \text{ to } 2.0 \text{ V}$	—	—	$0.3 \times V_{DD}$	V

4.4 Typical Performance Curves

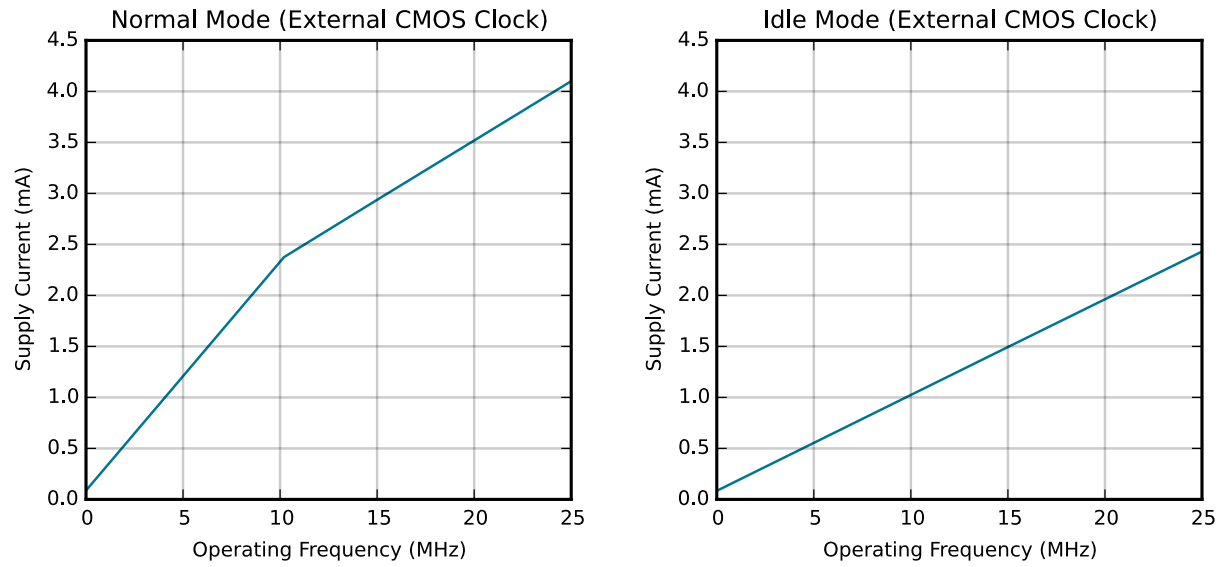


Figure 4.1. Typical Operating Supply Current (full supply voltage range)

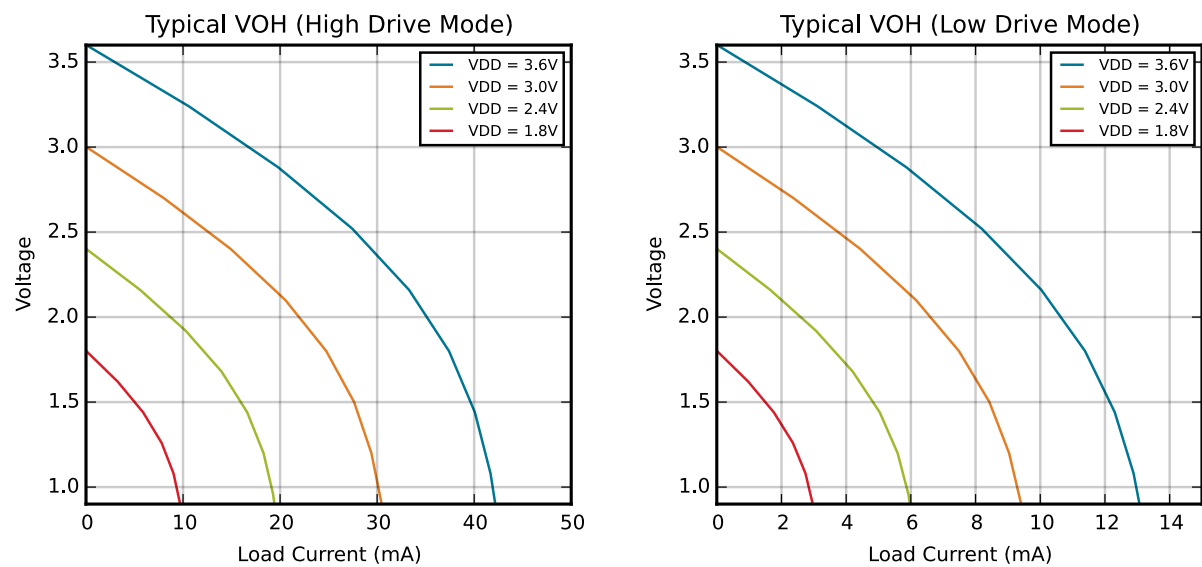


Figure 4.2. Typical V_{OH} Curves

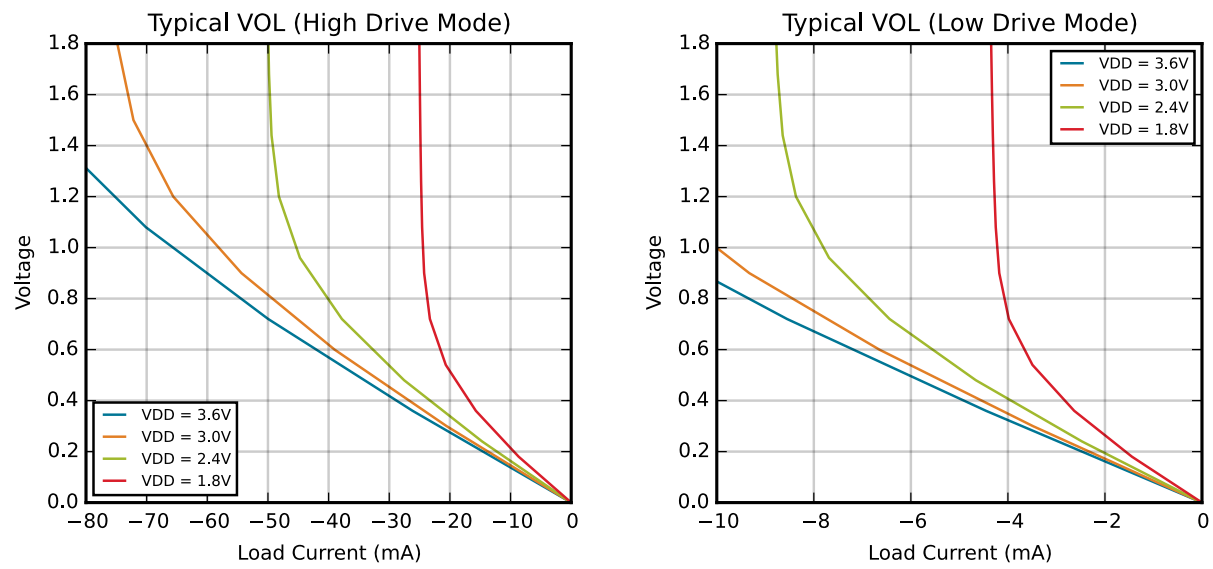


Figure 4.3. Typical V_{OL} Curves

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
5	N/C	No Connection			
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
8	P2.6	Multifunction I/O	Yes	EMIF_WRb	ADC0.22 CMP0P.11 CMP1P.11
9	XTAL4	RTC Crystal			XTAL4
10	XTAL3	RTC Crystal			XTAL3
11	P2.5	Multifunction I/O	Yes	EMIF_RDb	ADC0.21 CMP0N.10 CMP1N.10
12	P2.4	Multifunction I/O	Yes	EMIF_ALE	ADC0.20 CMP0P.10 CMP1P.10
13	P2.3	Multifunction I/O	Yes	EMIF_A11	ADC0.19 CMP0N.9 CMP1N.9
14	P2.2	Multifunction I/O	Yes	EMIF_A10	ADC0.18 CMP0P.9 CMP1P.9
15	P2.1	Multifunction I/O	Yes	EMIF_A9	ADC0.17 CMP0N.8 CMP1N.8
16	P2.0	Multifunction I/O	Yes	EMIF_A8	ADC0.16 CMP0P.8 CMP1P.8
17	P1.7	Multifunction I/O	Yes	P1MAT.7 EMIF_AD7	ADC0.15 CMP0N.7 CMP1N.7
18	P1.6	Multifunction I/O	Yes	P1MAT.6 EMIF_AD6	ADC0.14 CMP0P.7 CMP1P.7

6.2 EFM8SB2x-QFN24 Pin Definitions

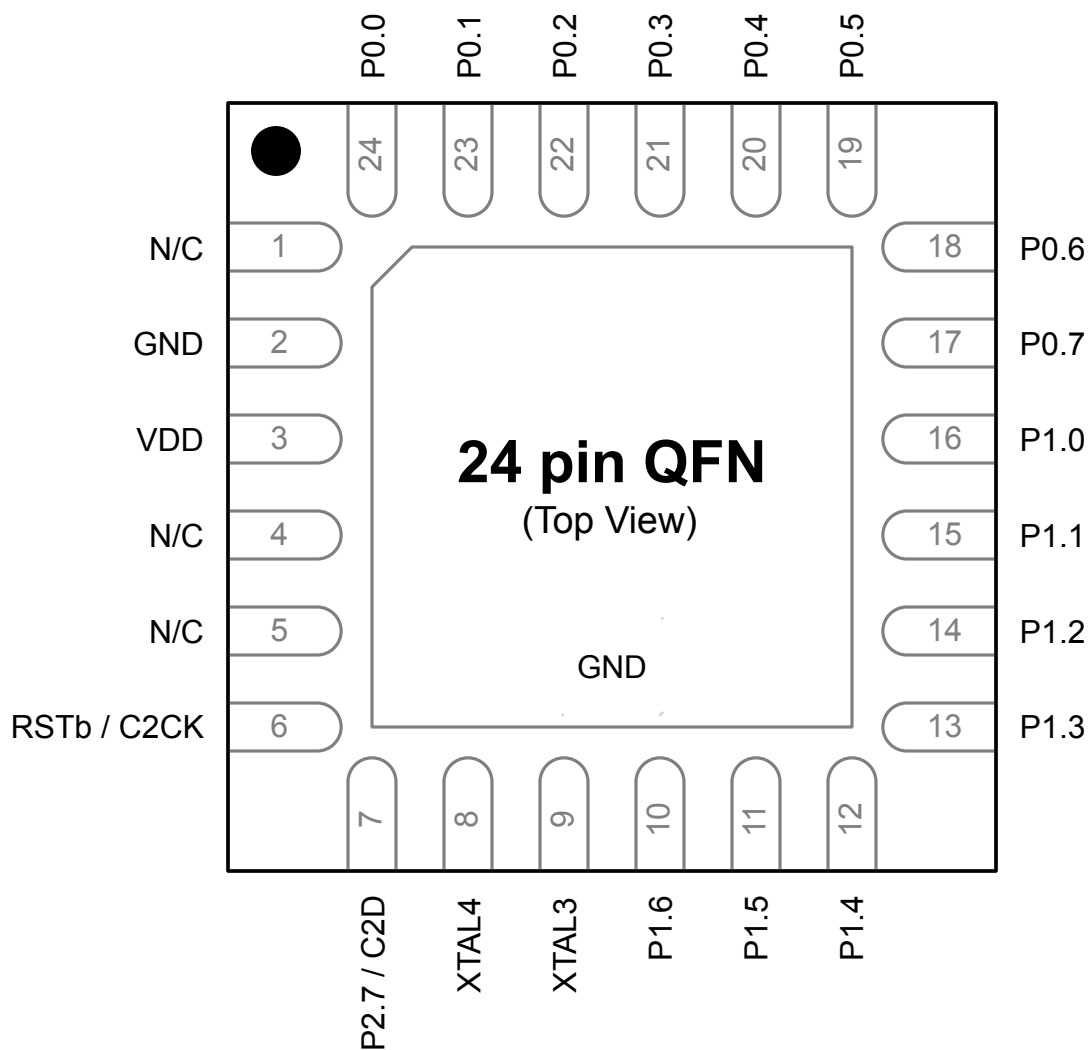


Figure 6.2. EFM8SB2x-QFN24 Pinout

Table 6.2. Pin Definitions for EFM8SB2x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	GND	Ground			
3	VDD	Supply Power Input			
4	N/C	No Connection			
5	N/C	No Connection			

6.3 EFM8SB2x-QFP32 Pin Definitions

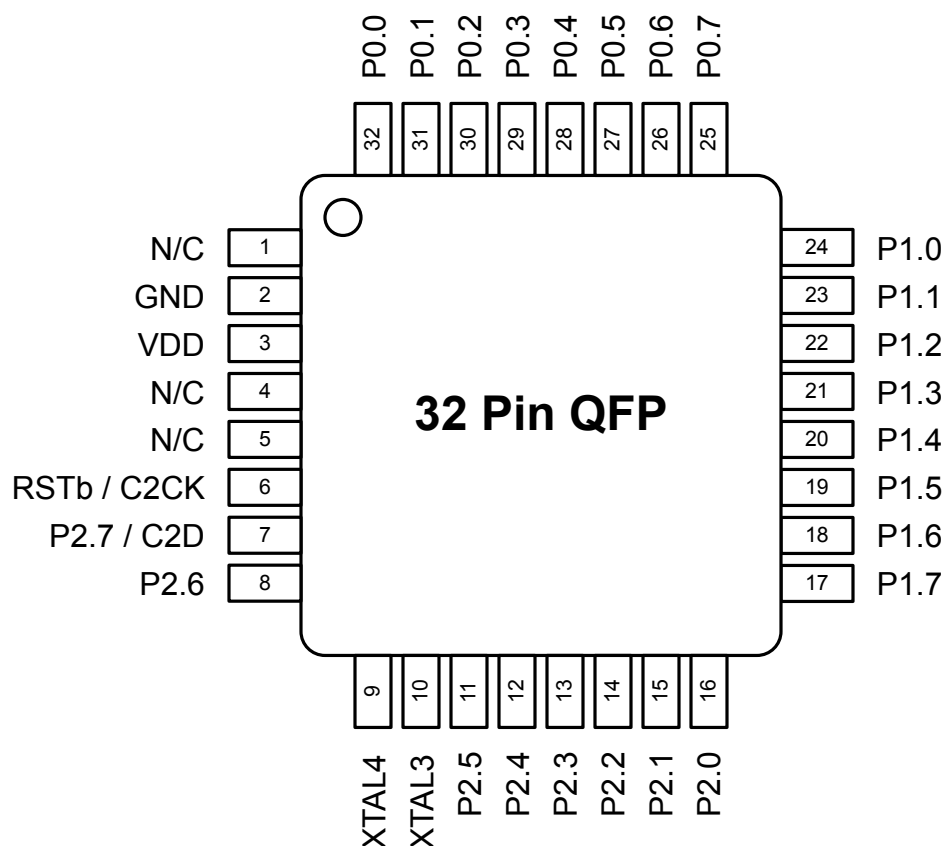


Figure 6.3. EFM8SB2x-QFP32 Pinout

Table 6.3. Pin Definitions for EFM8SB2x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	GND	Ground			
3	VDD	Supply Power Input			
4	N/C	No Connection			
5	N/C	No Connection			
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
21	P1.3	Multifunction I/O	Yes	P1MAT.3 SPI1_NSS EMIF_AD3	ADC0.11 CMP0N.5 CMP1N.5
22	P1.2	Multifunction I/O	Yes	P1MAT.2 SPI1_MOSI EMIF_AD2	ADC0.10 CMP0P.5 CMP1P.5
23	P1.1	Multifunction I/O	Yes	P1MAT.1 SPI1_MISO EMIF_AD1	ADC0.9 CMP0N.4 CMP1N.4
24	P1.0	Multifunction I/O	Yes	P1MAT.0 SPI1_SCK EMIF_AD0	ADC0.8 CMP0P.4 CMP1P.4
25	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 IREF0 CMP0N.3 CMP1N.3
26	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.3 CMP1P.3
27	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0N.2 CMP1N.2
28	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.2 CMP1P.2
29	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 XTAL2 CMP0N.1 CMP1N.1
30	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.1 CMP1P.1 XTAL1

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
31	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 AGND CMP0N.0 CMP1N.0
32	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP1P.0 VREF

7.2 QFN32 PCB Land Pattern

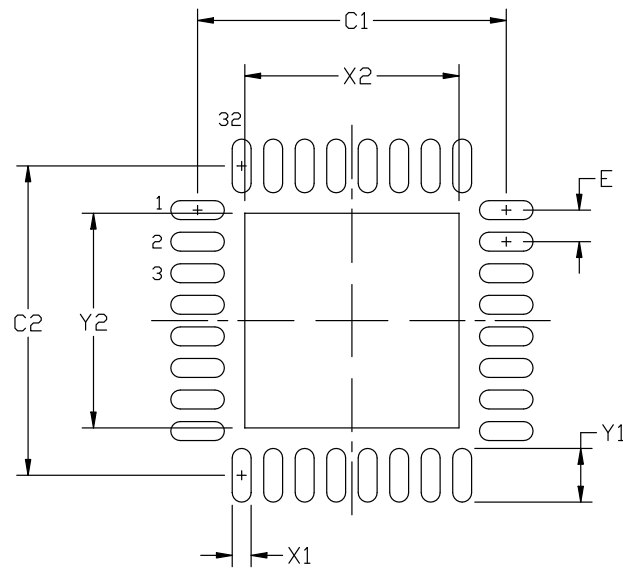


Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
Z	—	0.24	—
Y	—	0.18	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 5. The stencil thickness should be 0.125 mm (5 mils). 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 7. A 2 x 2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad. 8. A No-Clean, Type-3 solder paste is recommended. 9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

8.3 QFN24 Package Marking



Figure 8.3. QFN24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9. QFP32 Package Specifications

9.1 QFP32 Package Dimensions

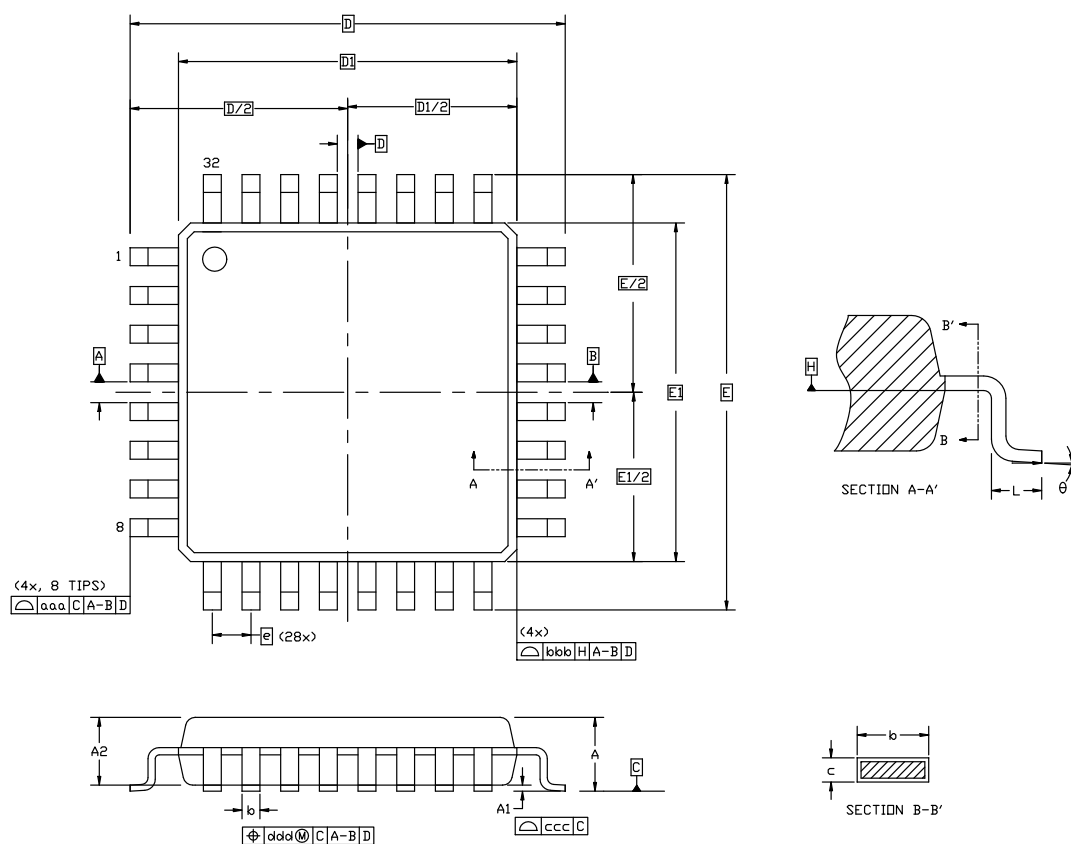


Figure 9.1. QFP32 Package Drawing

Table 9.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
aaa	0.20		

Dimension	Min	Typ	Max
bbb	0.20		
ccc	0.10		
ddd	0.20		
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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