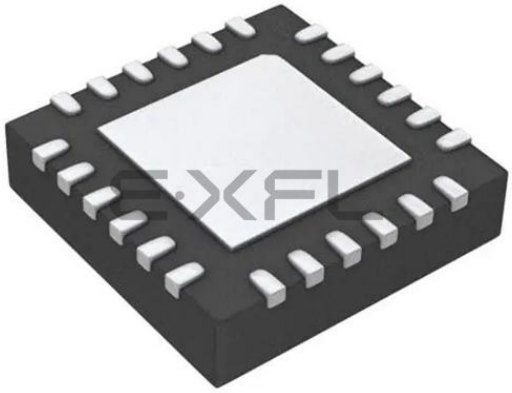

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb20f64g-a-qfn24

3. System Overview

3.1 Introduction

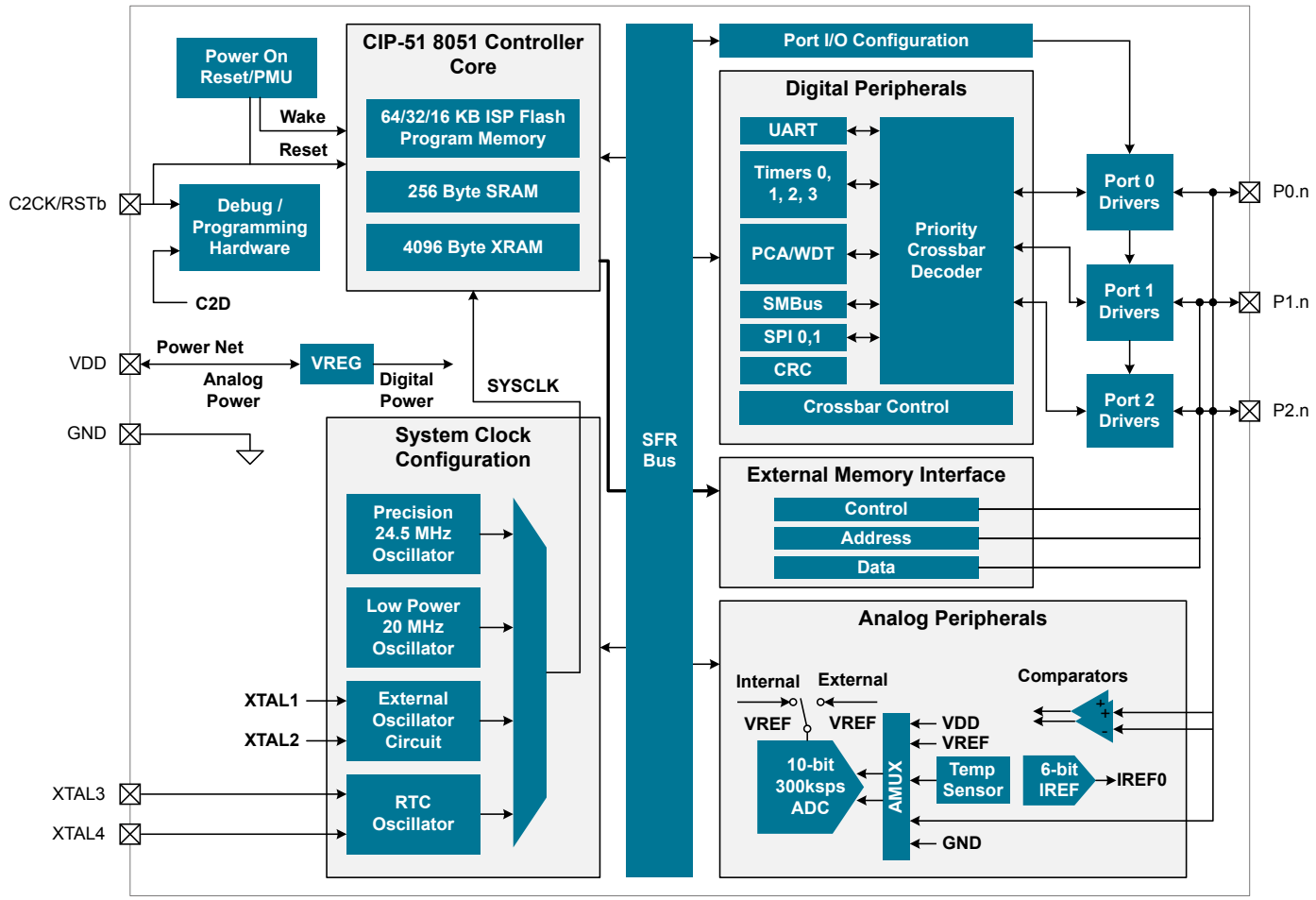

Figure 3.1. Detailed EFM8SB2 Block Diagram

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and digital peripherals halted • Internal oscillators disabled • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 or LPOSC0 2. Set SUSPEND bit in PMU0CF	• RTC0 Alarm Event • RTC0 Fail Event • Port Match Event • Comparator 0 Rising Edge
Sleep	• Most internal power nets shut down • Select circuits remain powered • Pins retain state • All RAM and SFRs retain state • Code resumes execution on wake event	1. Disable unused analog peripherals 2. Set SLEEP bit in PMU0CF	• RTC0 Alarm Event • RTC0 Fail Event • Port Match Event • Comparator 0 Rising Edge

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.6 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pin P2.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.7.

- Up to 24 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each pin.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 20 MHz low power oscillator divided by 8.

- Provides clock to core and peripherals.
- 20 MHz low power oscillator (LPOSC0), accurate to +/- 10% over supply and temperature corners.
- 24.5 MHz internal oscillator (HFOSC0), accurate to +/- 2% over supply and temperature corners.
- External RTC 32 kHz crystal.
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

3.5 Counters/Timers and PWM

Real Time Clock (RTC0)

The RTC is an ultra low power, 36 hour 32-bit independent time-keeping Real Time Clock with alarm. The RTC has a dedicated 32 kHz oscillator. No external resistor or loading capacitors are required, and a missing clock detector features alerts the system if the external crystal fails. The on-chip loading capacitors are programmable to 16 discrete levels allowing compatibility with a wide range of crystals.

The RTC module includes the following features:

- Up to 36 hours (32-bit) of independent time keeping.
- Support for external 32 kHz crystal or internal self-oscillate mode.
- Internal crystal loading capacitors with 16 levels.
- Operation in the lowest power mode and across the full supported voltage range.
- Alarm and oscillator failure events to wake from the lowest power mode or reset the device.

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (edge-aligned operation).
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Integrated watchdog timer.

Timers (Timer 0, Timer 1, Timer 2, and Timer 3)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2 and Timer 3 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- Comparator 0 or RTC0 capture (Timer 2)
- Comparator 1 or EXTCLK/8 capture (Timer 3)

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 8- or 9-bit data
- Automatic start and stop generation

Serial Peripheral Interface (SPI0 and SPI1)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to SYSCLK / 2 in master mode and SYSCLK / 10 in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock clock rate generator.
- Support for multiple masters on the same data lines.

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Endurance (Write/Erase Cycles)	N_{WE}		1 k	30 k	—	Cycles

Note:
1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{SUS-PENDWK}$	CLKDIV = 0x00 Precision Osc.	—	400	—	ns
		CLKDIV = 0x00 Low Power Osc.	—	1.3	—	µs
Sleep Mode Wake-up Time	$t_{SLEEPWK}$		—	2	—	µs

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Low Power Oscillator (20 MHz)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	18	20	22	MHz
RTC in Self-Oscillate Mode						
Oscillator Frequency	f_{LFOSC}	Bias Off	—	12 ± 5	—	kHz
		Bias On	—	25 ± 10	—	kHz

Table 4.7. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	-	25	MHz

Table 4.8. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		18	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		18	—	—	ns

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}			10		Bits
Throughput Rate	f_S		—	—	300	ksps
Tracking Time	t_{TRK}		1.5	—	—	µs
Power-On Time	t_{PWR}		1.5	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode,	—	—	8.33	MHz
Conversion Time	T_{CNV}		13	—	—	Clocks
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	30	—	pF
		Gain = 0.5	—	28	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	5	—	kΩ
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	2 x V_{REF}	V
Power Supply Rejection Ratio	$PSRR_{ADC}$	Internal High Speed VREF	—	67	—	dB
		External VREF	—	74	—	dB
DC Performance						
Integral Nonlinearity	INL		—	±0.5	±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Offset Error	E_{OFF}	VREF = 1.65 V	–2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M		—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput						
Signal-to-Noise	SNR		54	58	—	dB
Signal-to-Noise Plus Distortion	SNDR		54	58	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD		—	-73	—	dB
Spurious-Free Dynamic Range	SFDR		—	75	—	dB

Note:
1. Absolute input pin voltage is limited by the V_{DD} supply.

Table 4.10. Voltage References

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}		1.60	1.65	1.70	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{VREFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-chip Precision Reference						
Output Voltage	V_{REFP}		1.645	1.68	1.715	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 µF tantalum + 0.1 µF ceramic bypass on VREF pin	—	15	—	ms
		0.1 µF ceramic bypass on VREF pin	—	300	—	µs
		No bypass on VREF pin	—	25	—	µs
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to GND	—	400	—	µV / µA
Short-circuit current	ISC_{VREFP}		—	3.5	—	mA
Power Supply Rejection	$PSRR_{VREFP}$		—	140	—	ppm/V
External Reference						
Input Voltage	V_{EXTREF}		1	—	V_{DD}	V
Input Current	I_{EXTREF}	Sample Rate = 300 ksps; VREF = 3.0 V	—	5.25	—	µA

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	940	—	mV
Offset Error[1]	E_{OFF}	T_A = 0 °C	—	18	—	mV
Slope	M		—	3.40	—	mV/°C
Slope Error[1]	E_M		—	40	—	µV/°C
Linearity			—	±1	—	°C
Turn-on Time	t_{PWR}		—	1.8	—	µs

Note:
1. Represents one standard deviation from the mean.

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	130	—	ns
		–100 mV Differential	—	200	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.75	—	µs
		–100 mV Differential	—	6.2	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C

Table 4.13. Programmable Current Reference (IREF0)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Performance						
Resolution	N_{bits}			6		bits
Output Compliance Range	V_{IOUT}	Low Power Mode, Source	0	—	V_{DD} – 0.4	V
		High Current Mode, Source	0	—	V_{DD} – 0.8	V
		Low Power Mode, Sink	0.3	—	V_{DD}	V
		High Current Mode, Sink	0.8	—	V_{DD}	V
Integral Nonlinearity	INL		—	<±0.2	±1.0	LSB
Differential Nonlinearity	DNL		—	<±0.2	±1.0	LSB
Offset Error	E_{OFF}		—	<±0.1	±0.5	LSB
Full Scale Error	E_{FS}	Low Power Mode, Source	—	—	±5	%
		High Current Mode, Source	—	—	±6	%
		Low Power Mode, Sink	—	—	±8	%
		High Current Mode, Sink	—	—	±8	%
Absolute Current Error	E_{ABS}	Low Power Mode Sourcing 20 µA	—	<±1	±3	%
Dynamic Performance						
Output Settling Time to 1/2 LSB	t_{SETTLE}		—	300	—	ns
Startup Time	t_{PWR}		—	1	—	µs

Note:
1. The PCA block may be used to improve IREF0 resolution by PWMing the two LSBs.

Table 4.14. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = –3 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 1.4 mA	—	—	0.6	V
Input High Voltage	V_{IH}	V_{DD} = 2.0 to 3.6 V	V_{DD} – 0.6	—	—	V
		V_{DD} = 1.8 to 2.0 V	0.7 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}	V_{DD} = 2.0 to 3.6 V	—	—	0.6	V
		V_{DD} = 1.8 to 2.0 V	—	—	0.3 x V_{DD}	V

4.4 Typical Performance Curves

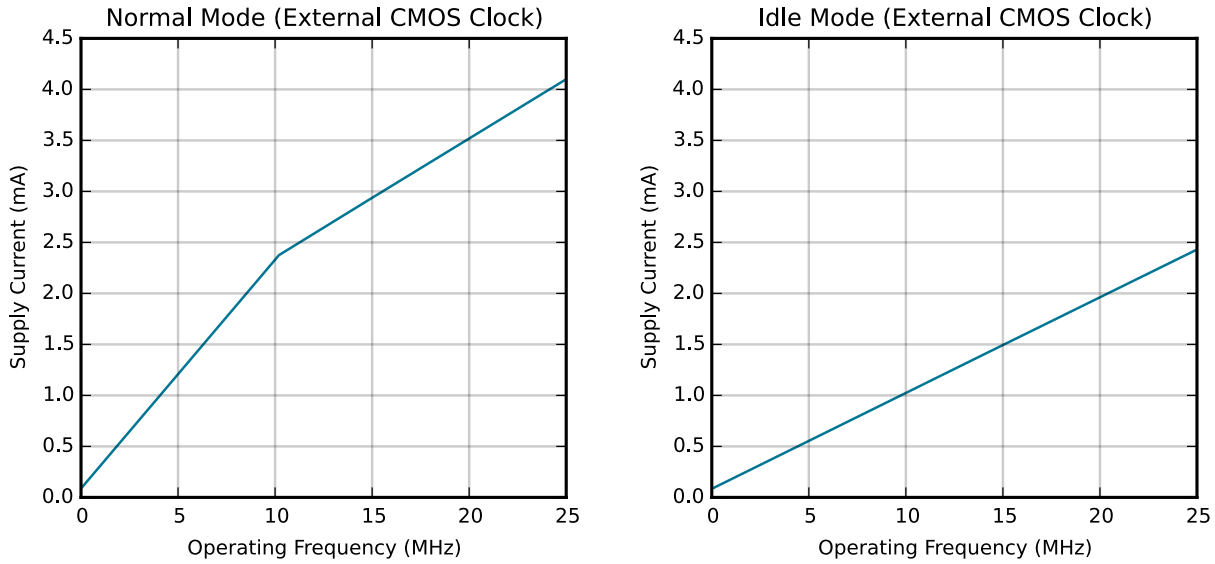

Figure 4.1. Typical Operating Supply Current (full supply voltage range)

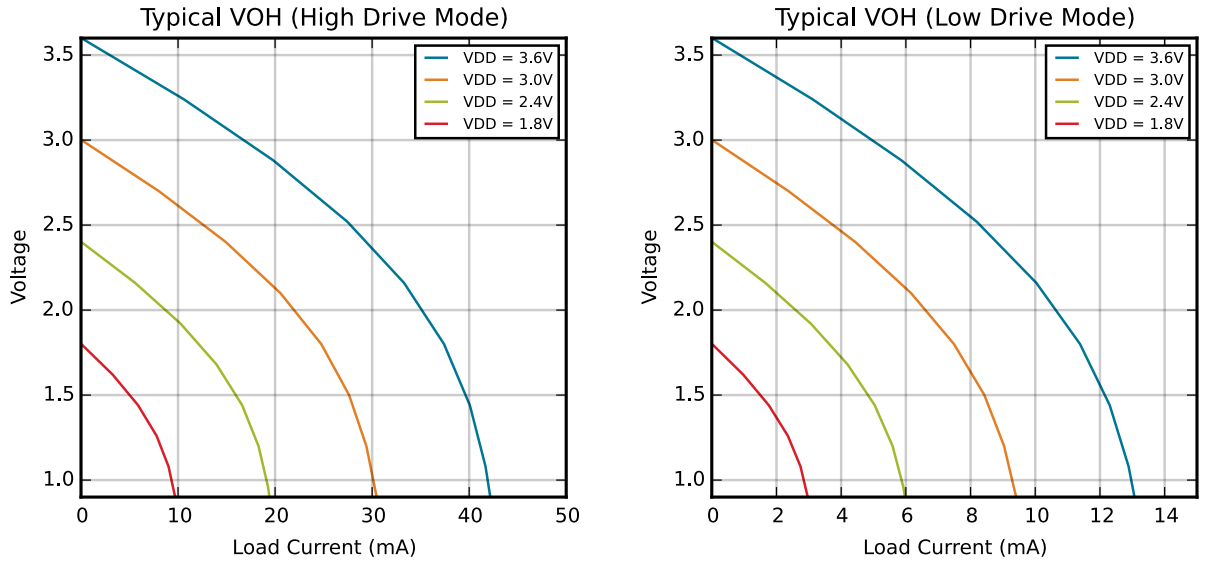

Figure 4.2. Typical V_{OH} Curves

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
8	XTAL4	RTC Crystal			XTAL4
9	XTAL3	RTC Crystal			XTAL3
10	P1.6	Multifunction I/O	Yes		ADC0.14 CMP0P.7 CMP1P.7
11	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP0N.6 CMP1N.6
12	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP0P.6 CMP1P.6
13	P1.3	Multifunction I/O	Yes	P1MAT.3 SPI1_NSS	ADC0.11 CMP0N.5 CMP1N.5
14	P1.2	Multifunction I/O	Yes	P1MAT.2 SPI1_MOSI	ADC0.10 CMP0P.5 CMP1P.5
15	P1.1	Multifunction I/O	Yes	P1MAT.1 SPI1_MISO	ADC0.9 CMP0N.4 CMP1N.4
16	P1.0	Multifunction I/O	Yes	P1MAT.0 SPI1_SCK	ADC0.8 CMP0P.4 CMP1P.4
17	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 IREF0 CMP0N.3 CMP1N.3
18	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.3 CMP1P.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0N.2 CMP1N.2
20	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.2 CMP1P.2
21	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 XTAL2 CMP0N.1 CMP1N.1
22	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.1 CMP1P.1 XTAL1
23	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 AGND CMP0N.0 CMP1N.0
24	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP1P.0 VREF
Center	GND	Ground			

6.3 EFM8SB2x-QFP32 Pin Definitions

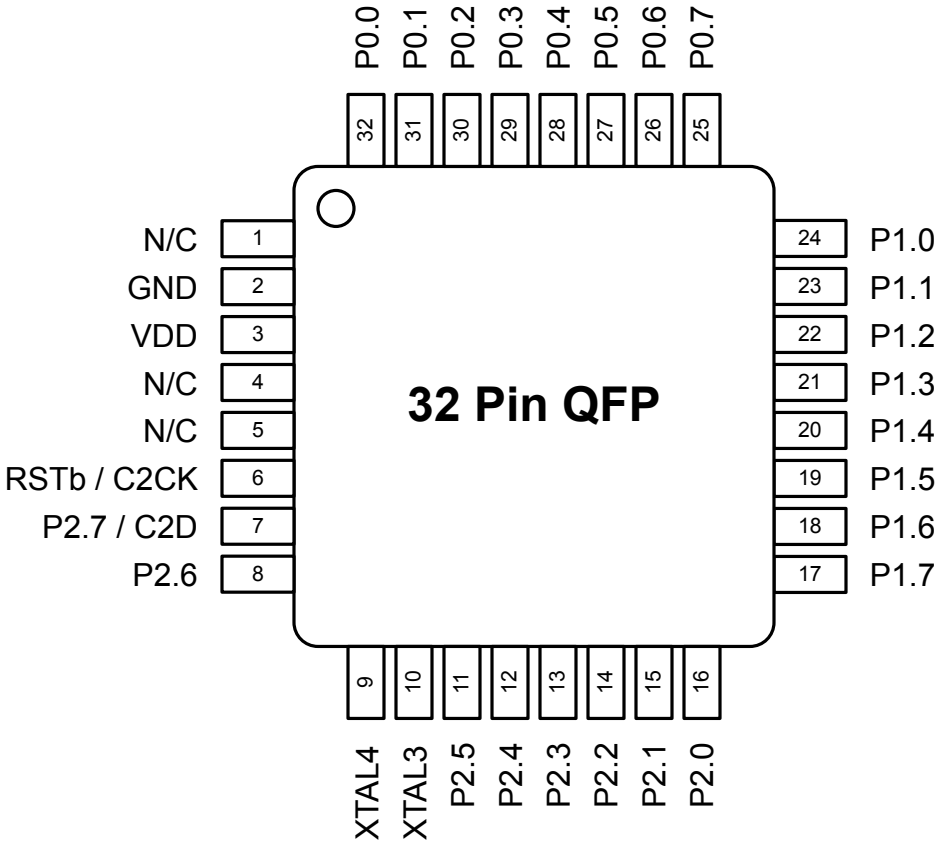

Figure 6.3. EFM8SB2x-QFP32 Pinout

Table 6.3. Pin Definitions for EFM8SB2x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	GND	Ground			
3	VDD	Supply Power Input			
4	N/C	No Connection			
5	N/C	No Connection			
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2 QFN32 PCB Land Pattern

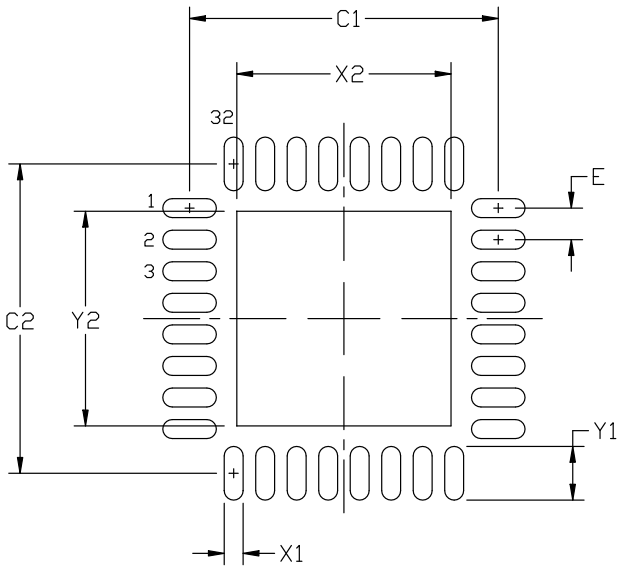

Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.3 QFN32 Package Marking

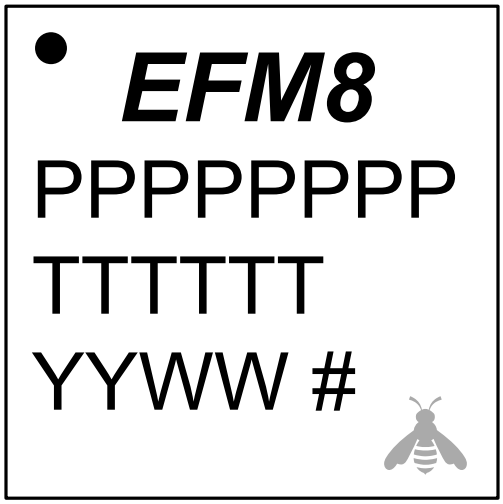

Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

8. QFN24 Package Specifications

8.1 QFN24 Package Dimensions

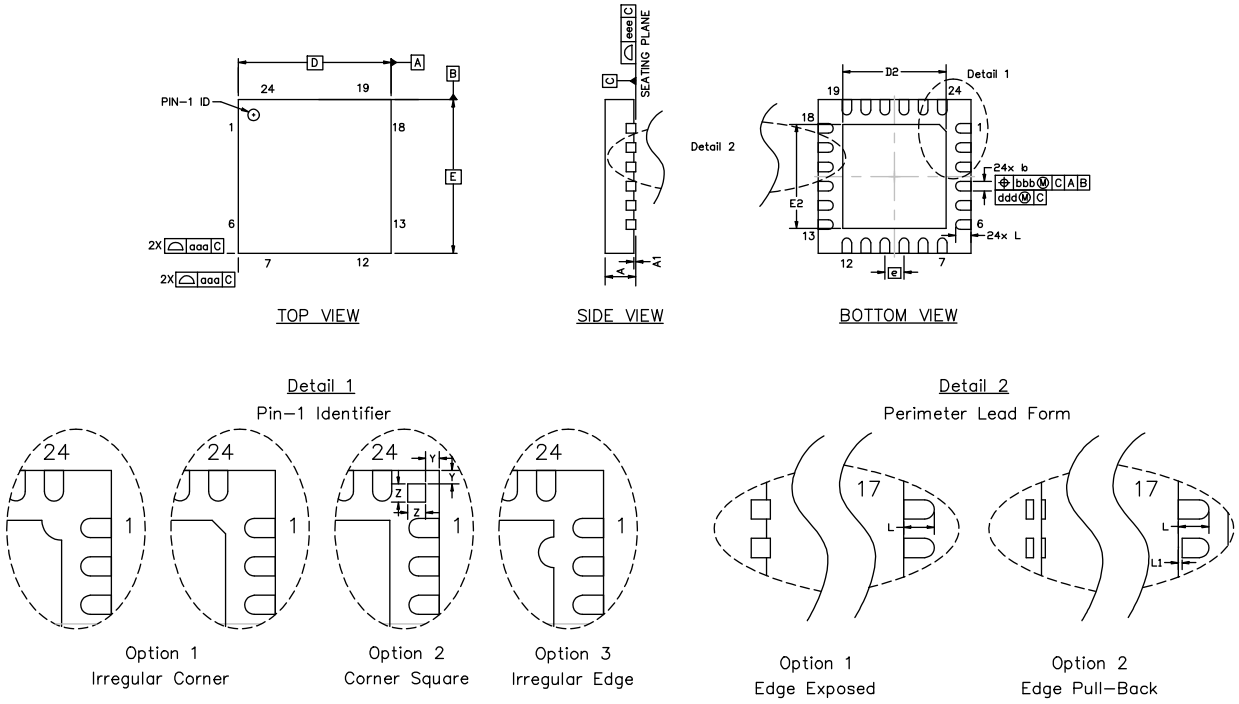

Figure 8.1. QFN24 Package Drawing

Table 8.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.55	2.70	2.80
e		0.50 BSC	
E		4.00 BSC	
E2	2.55	2.70	2.80
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15

Dimension	Min	Typ	Max
bbb		0.20	
ccc		0.10	
ddd		0.20	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.2 QFP32 PCB Land Pattern

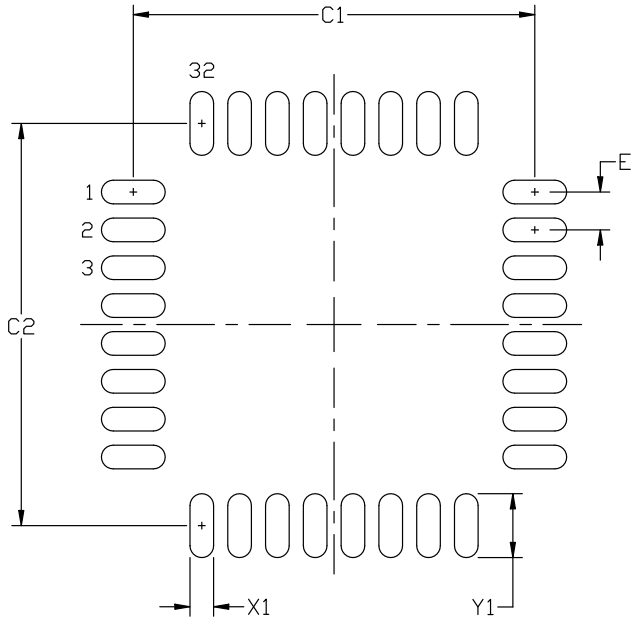

Figure 9.2. QFP32 PCB Land Pattern Drawing

Table 9.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.40	0.50
Y1	1.25	1.35

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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