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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	PWM, WDT
Number of I/O	70
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3024f25v

2.3 Address Space

Figure 2.2 shows a simple memory map for the H8/3024 Group. The H8/300H CPU can address a linear address space with a maximum size of 64 kbytes in normal mode, and 16 Mbytes in advanced mode. For further details see section 3.6, Memory Map in Each Operating Mode.

The 1-Mbyte operating modes use 20-bit addressing. The upper 4 bits of effective addresses are ignored.

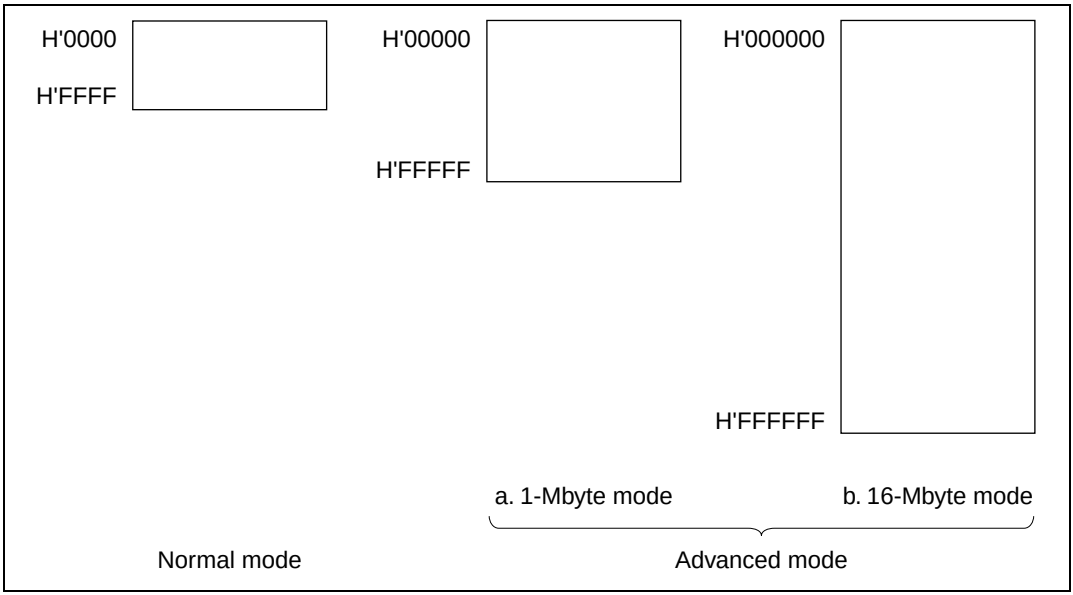


Figure 2.2 Memory Map

6.5.2 Pin States in Idle Cycle

Table 6.5 shows the pin states in an idle cycle.

Table 6.5 Pin States in Idle Cycle

Pins	Pin State
A_{23} to A_0	Next cycle address value
D_{15} to D_0	High-impedance
$\overline{CS}$n	High
$\overline{AS}$	High
$\overline{RD}$	High
$\overline{HWR}$	High
$\overline{LWR}$	High

6.6 Bus Arbiter

The bus controller has a built-in bus arbiter that arbitrates between different bus masters. The bus master can be either the CPU or an external bus master. When a bus master has the bus right it can carry out read and write operations. Each bus master uses a bus request signal to request the bus right. At fixed times the bus arbiter determines priority and uses a bus acknowledge signal to grant the bus to a bus master, which can the operate using the bus.

The bus arbiter checks whether the bus request signal from a bus master is active or inactive, and returns an acknowledge signal to the bus master. When two or more bus masters request the bus, the highest-priority bus master receives an acknowledge signal. The bus master that receives an acknowledge signal can continue to use the bus until the acknowledge signal is deactivated.

The bus master priority order is:

(High) External bus master > CPU (Low)

The bus arbiter samples the bus request signals and determines priority at all times, but it does not always grant the bus immediately, even when it receives a bus request from a bus master with higher priority than the current bus master. Each bus master has certain times at which it can release the bus to a higher-priority bus master.

6.7 Register and Pin Input Timing

6.7.1 Register Write Timing

ABWCR, ASTCR, WCRH, and WCRL Write Timing: Data written to ABWCR, ASTCR, WCRH, and WCRL takes effect starting from the next bus cycle. Figure 6.21 shows the timing when an instruction fetched from area 0 changes area 0 from three-state access to two-state access.

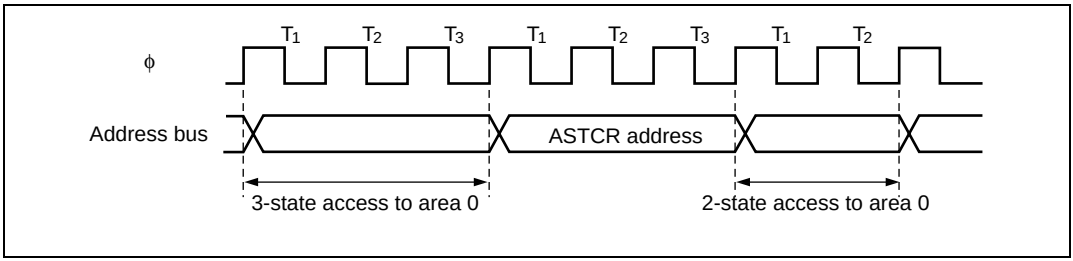


Figure 6.21 ASTCR Write Timing

DDR and CSCR Write Timing: Data written to DDR or CSCR for the port corresponding to the $\overline{CS}$n pin to switch between $\overline{CS}$n output and generic input takes effect starting from the T_3 state of the DDR write cycle. Figure 6.22 shows the timing when the $\overline{CS}_1$ pin is changed from generic input to $\overline{CS}_1$ output.

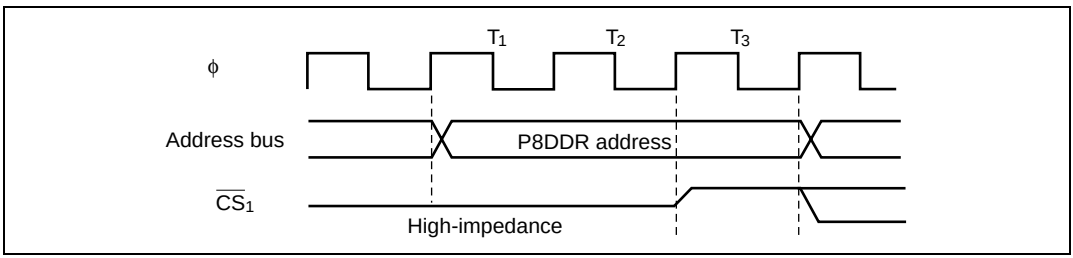
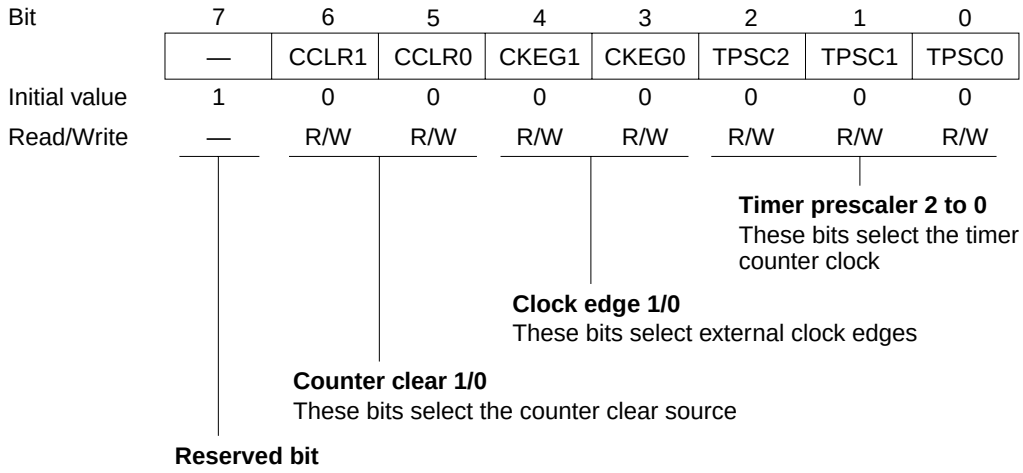


Figure 6.22 DDR Write Timing

8.2.9 Timer Control Registers (16TCR)

16TCR is an 8-bit register. The 16-bit timer has three 16TCRs, one in each channel.

Channel	Abbreviation	Function
0	16TCR0	16TCR controls the timer counter. The 16TCRs in all channels are functionally identical. When phase counting mode is selected in channel 2, the settings of bits CKEG1 and CKEG0 and TPSC2 to TPSC0 in 16TCR2 are ignored.
1	16TCR1	
2	16TCR2	



Each 16TCR is an 8-bit readable/writable register that selects the timer counter clock source, selects the edge or edges of external clock sources, and selects how the counter is cleared.

16TCR is initialized to H'80 by a reset and in standby mode.

Bit 7—Reserved: This bit cannot be modified and is always read as 1.

Bits 6 and 5—Counter Clear 1 and 0 (CCLR1, CCLR0): These bits select how 16TCNT is cleared.

Bits 4 and 3—Counter Clear 1 and 0 (CCLR1, CCLR0): These bits specify the 8TCNT clearing source. Compare match A or B, or input capture B, can be selected as the clearing source.

Bit 4 CCLR1	Bit 3 CCLR0	Description	
0	0	Clearing is disabled	(Initial value)
	1	Cleared by compare match A	
1	0	Cleared by compare match B/input capture B	
	1	Cleared by input capture B	

Note: When input capture B is set as the 8TCNT1 and 8TCNT3 counter clear source, 8TCNT0 and 8TCNT2 are not cleared by compare match B.

Bits 2 to 0—Clock Select 2 to 0 (CSK2 to CSK0): These bits select whether the clock input to 8TCNT is an internal or external clock.

Three internal clocks can be selected, all divided from the system clock (ϕ): ϕ/8, ϕ/64, and ϕ/8192. The rising edge of the selected internal clock triggers the count.

When use of an external clock is selected, three types of count can be selected: at the rising edge, the falling edge, and both rising and falling edges.

When CKS2, CKS1, CKS0 = 1, 0, 0, channels 0 and 1 and channels 2 and 3 are cascaded.

The incrementing clock source is different when 8TCR0 and 8TCR2 are set, and when 8TCR1 and 8TCR3 are set.

9.3 CPU Interface

9.3.1 8-Bit Registers

8TCNT, TCORA, TCORB, 8TCR, and 8TCSR are 8-bit registers. These registers are connected to the CPU by an internal 16-bit data bus and can be read and written a word at a time or a byte at a time.

Figures 9.2 and 9.3 show the operation in word read and write accesses to 8TCNT.

Figures 9.4 to 9.7 show the operation in byte read and write accesses to 8TCNT0 and 8TCNT1.

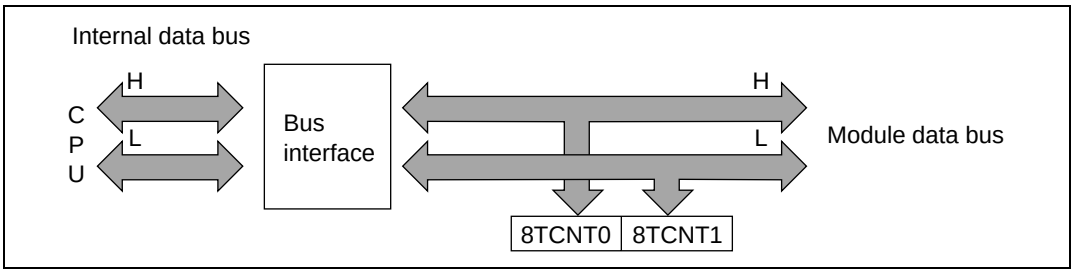


Figure 9.2 8TCNT Access Operation (CPU Writes to 8TCNT, Word)

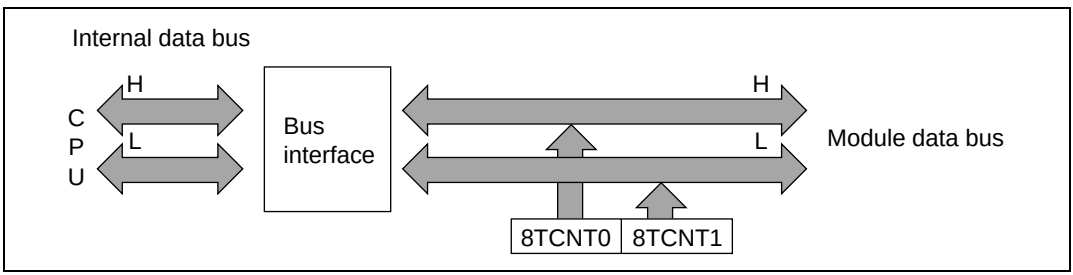
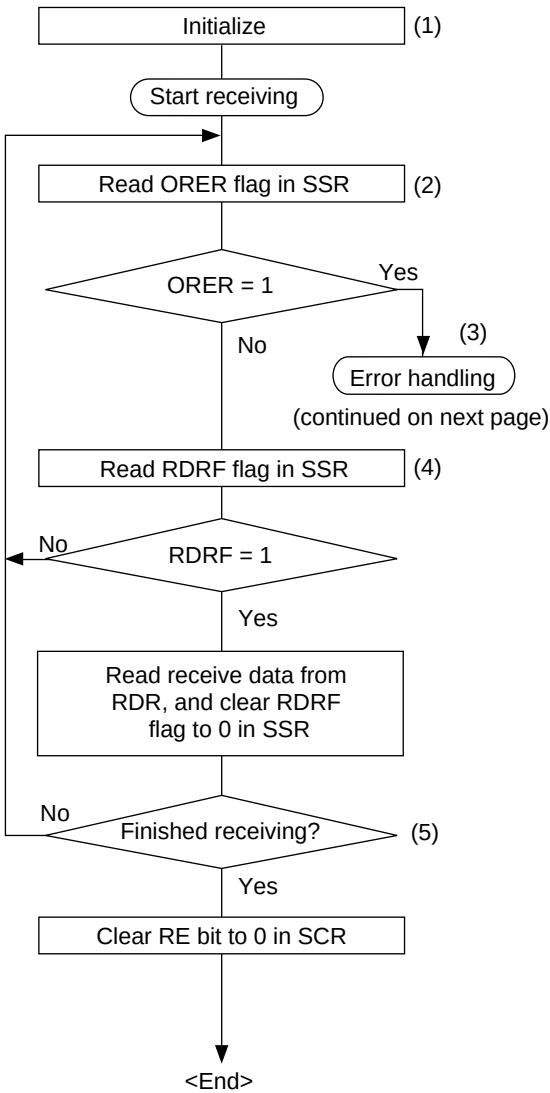


Figure 9.3 8TCNT Access Operation (CPU Reads 8TCNT, Word)

PER flag is set to 1 the RDRF flag will not be set and both transmitting and receiving will be disabled.



(1) SCI initialization: the receive data input function of the RxD pin is selected automatically.

(2)(3) Receive error handling: if a receive error occurs, read the ORER flag in SSR, then after executing the necessary error handling, clear the ORER flag to 0. Neither transmitting nor receiving can resume while the ORER flag remains set to 1.

(4) SCI status check and receive data read: read SSR, check that the RDRF flag is set to 1, then read receive data from RDR and clear the RDRF flag to 0. Notification that the RDRF flag has changed from 0 to 1 can also be given by the RXI interrupt.

(5) To continue receiving serial data: check the RDRF flag, read RDR, and clear the RDRF flag to 0 before the MSB (bit 7) of the current frame is received.

Figure 12.18 Sample Flowchart for Serial Receiving

13.2.2 Serial Status Register (SSR)

The function of SSR bit 4 is modified in smart card interface mode. This change also causes a modification to the setting conditions for bit 2 (TEND).

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Transmit end
Status flag indicating end of transmission

Error signal status (ERS)
Status flag indicating that an error signal has been received

Note: * Only 0 can be written, to clear the flag.

Bits 7 to 5: These bits operate as in normal serial communication. For details see section 12.2.7, Serial Status Register (SSR).

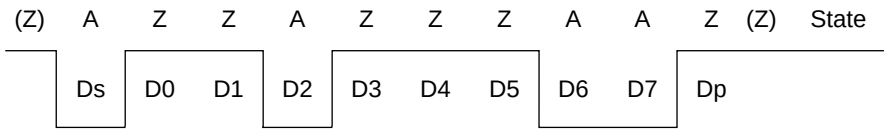
Bit 4—Error Signal Status (ERS): In smart card interface mode, this flag indicates the status of the error signal sent from the receiving device to the transmitting device. The smart card interface does not detection framing errors.

Bit 4 ERS	Description
0	Indicates normal transmission, with no error signal returned (Initial value) [Clearing conditions] • The chip is reset, or enters standby mode or module stop mode • Software reads ERS while it is set to 1, then writes 0.
1	Indicates that the receiving device sent an error signal reporting a parity error [Setting condition] A low error signal was sampled.

Note: Clearing the TE bit to 0 in SCR does not affect the ERS flag, which retains its previous value.

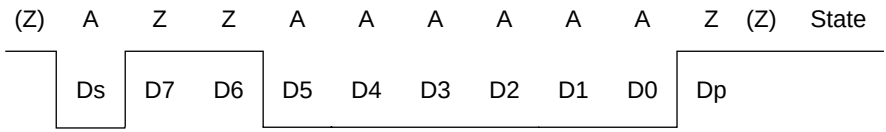
The register settings and examples of starting character waveforms are shown below for two smart cards, one following the direct convention and one the inverse convention.

1. Direct Convention (SDIR = SINV = O/$\overline{E}$ = 0)



With the direct convention type, the logic 1 level corresponds to state Z and the logic 0 level to state A, and transfer is performed in LSB-first order. In the example above, the first character data is H'3B. The parity bit is 1, following the even parity rule designated for smart cards.

2. Inverse Convention (SDIR = SINV = O/$\overline{E}$ = 1)



With the inverse convention type, the logic 1 level corresponds to state A and the logic 0 level to state Z, and transfer is performed in MSB-first order. In the example above, the first character data is H'3F. The parity bit is 0, corresponding to state Z, following the even parity rule designated for smart cards.

In the H8/3024 Group, inversion specified by the SINV bit applies only to the data bits, D7 to D0. For parity bit inversion, the O/$\overline{E}$ bit in SMR must be set to odd parity mode. This applies to both transmission and reception.

18.3.3 Erase Block Register (EBR)

EBR is an 8-bit register that designates the flash memory block for erasure. EBR is initialized to H'00 by a reset, in hardware standby mode or software standby mode, when a high level is not input to the FWE pin, or when the SWE bit in FLMCR1 is 0 when a high level is applied to the FWE pin. When a bit is set in EBR, the corresponding block can be erased. Other blocks are erase-protected. The blocks are erased block by block. Therefore, set only one bit in EBR; do not set bits in EBR to erase two or more blocks at the same time.

Each bit in EBR cannot be set until the SWE bit in FLMCR1 is set. The flash memory block configuration is shown in table 18.4. To erase all the blocks, erase each block sequentially.

The H8/3024F-ZTAT version does not support the on-board programming mode in mode 6, so bits in this register cannot be set to 1 in mode 6.

	Bit	7	6	5	4	3	2	1	0
		EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Modes 1 to 4, and 6	Initial value	0	0	0	0	0	0	0	0
	Read/Write	R	R	R	R	R	R	R	R
Modes 5 and 7	Initial value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 to 0—Block 7 to Block 0 (EB7 to EB0): Setting one of these bits specifies the corresponding block (EB7 to EB0) for erasure.

Bits 7–0 EB7–EB0	Description	
0	Corresponding block (EB7 to EB0) not selected	(Initial value)
1	Corresponding block (EB7 to EB0) selected	

Note: When not performing an erase, clear all EBR bits to 0.

Table 19.3 (1) Clock Timing for On-Chip Flash Memory Versions

		V_{CC} = 3.0 V to 3.6 V				
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**	
External clock input low pulse width	t_{EXL}	t_{cyc} / 2 - 5	—	ns	ϕ > 8 MHz	Figure 19.6
		55	—	ns	$\phi \leq$ 8 MHz	
External clock input high pulse width	t_{EXH}	t_{cyc} / 2 - 5	—	ns	ϕ > 8 MHz	
		55	—	ns	$\phi \leq$ 8 MHz	
External clock rise time	t_{EXr}	—	8	ns		
External clock fall time	t_{EXf}	—	8	ns		
Clock low pulse width	t_{CL}	0.4	0.6	t_{cyc}	$\phi \geq$ 5 MHz	Figure 21.11
		80	—	ns	ϕ < 5 MHz	
Clock high pulse width	t_{CH}	0.4	0.6	t_{cyc}	$\phi \geq$ 5 MHz	
		80	—	ns	ϕ < 5 MHz	
External clock output settling delay time	t_{DEXT}*	500	—	µs	Figure 19.7	

Note: * t_{DEXT} includes a $\overline{RES}$ pulse width (t_{RESW}). t_{RESW} = 20 t_{cyc}

Table 19.3 (2) Clock Timing for On-Chip Mask ROM Versions

		V_{CC} = 3.0 V to 3.6 V				
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**	
External clock input low pulse width	t_{EXL}	t_{cyc} / 2 - 5	—	ns	ϕ > 8 MHz	Figure 19.6
		55	—	ns	$\phi \leq$ 8 MHz	
External clock input high pulse width	t_{EXH}	t_{cyc} / 2 - 5	—	ns	ϕ > 8 MHz	
		55	—	ns	$\phi \leq$ 8 MHz	
External clock rise time	t_{EXr}	—	8	ns		
External clock fall time	t_{EXf}	—	8	ns		
Clock low pulse width	t_{CL}	0.4	0.6	t_{cyc}	$\phi \geq$ 5 MHz	Figure 21.11
		80	—	ns	ϕ < 5 MHz	
Clock high pulse width	t_{CH}	0.4	0.6	t_{cyc}	$\phi \geq$ 5 MHz	
		80	—	ns	ϕ < 5 MHz	
External clock output settling delay time	t_{DEXT}*	500	—	µs	Figure 19.7	

Note: * t_{DEXT} includes the $\overline{RES}$ pulse width (t_{RESW}). t_{RESW} = 20 t_{cyc}.

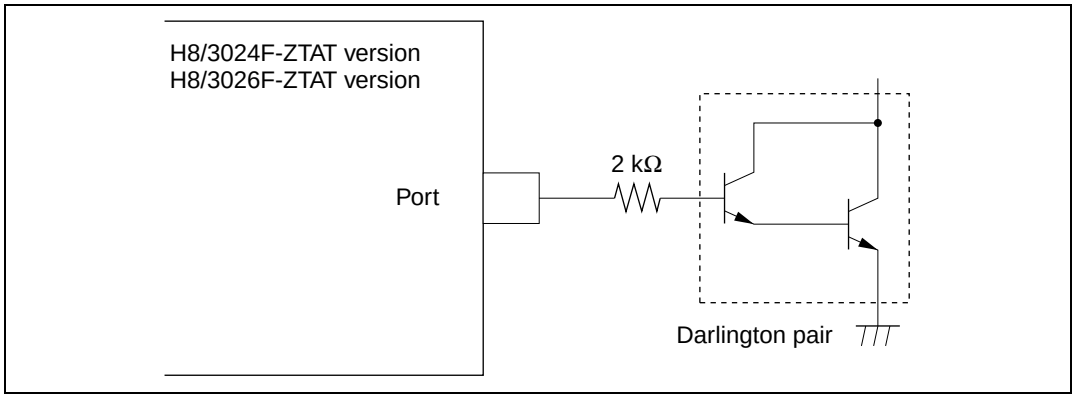


Figure 21.4 Darlington Pair Drive Circuit (Example)

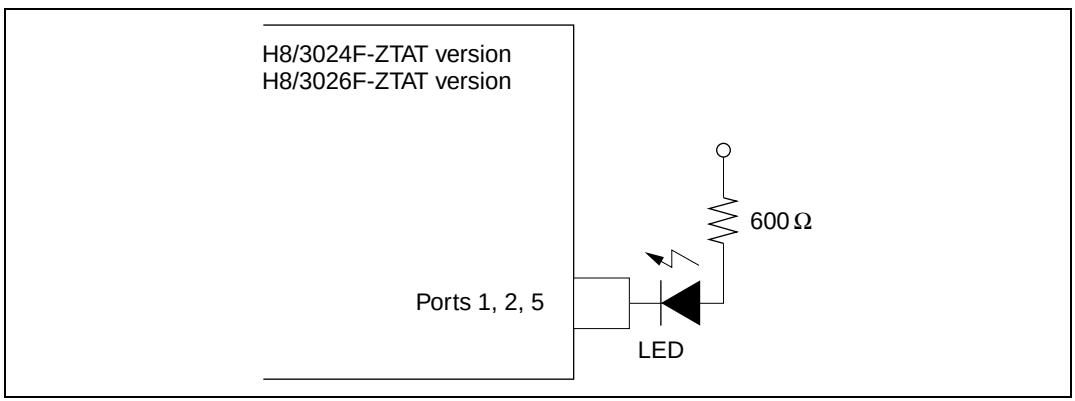


Figure 21.5 Sample LED Circuit

21.2.3 AC Characteristics

Clock timing parameters are listed in table 21.13, control signal timing parameters in table 21.14, and bus timing parameters in table 21.15. Timing parameters of the on-chip supporting modules are listed in table 21.16.

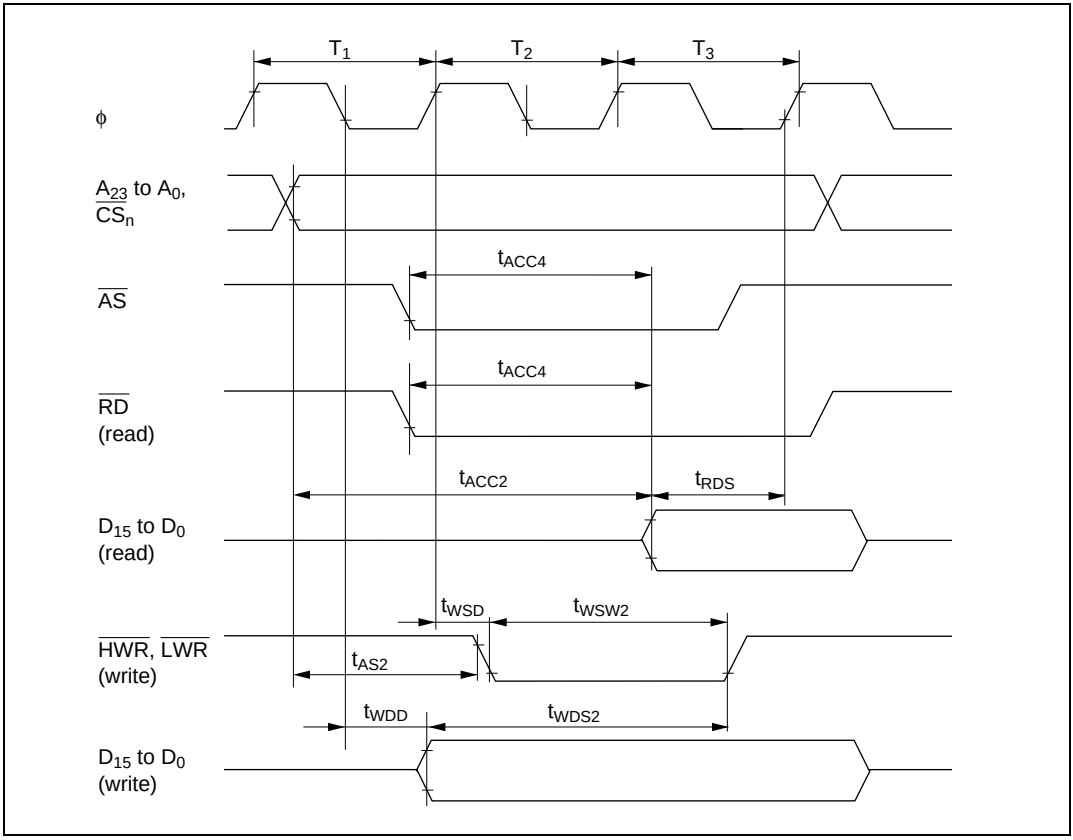
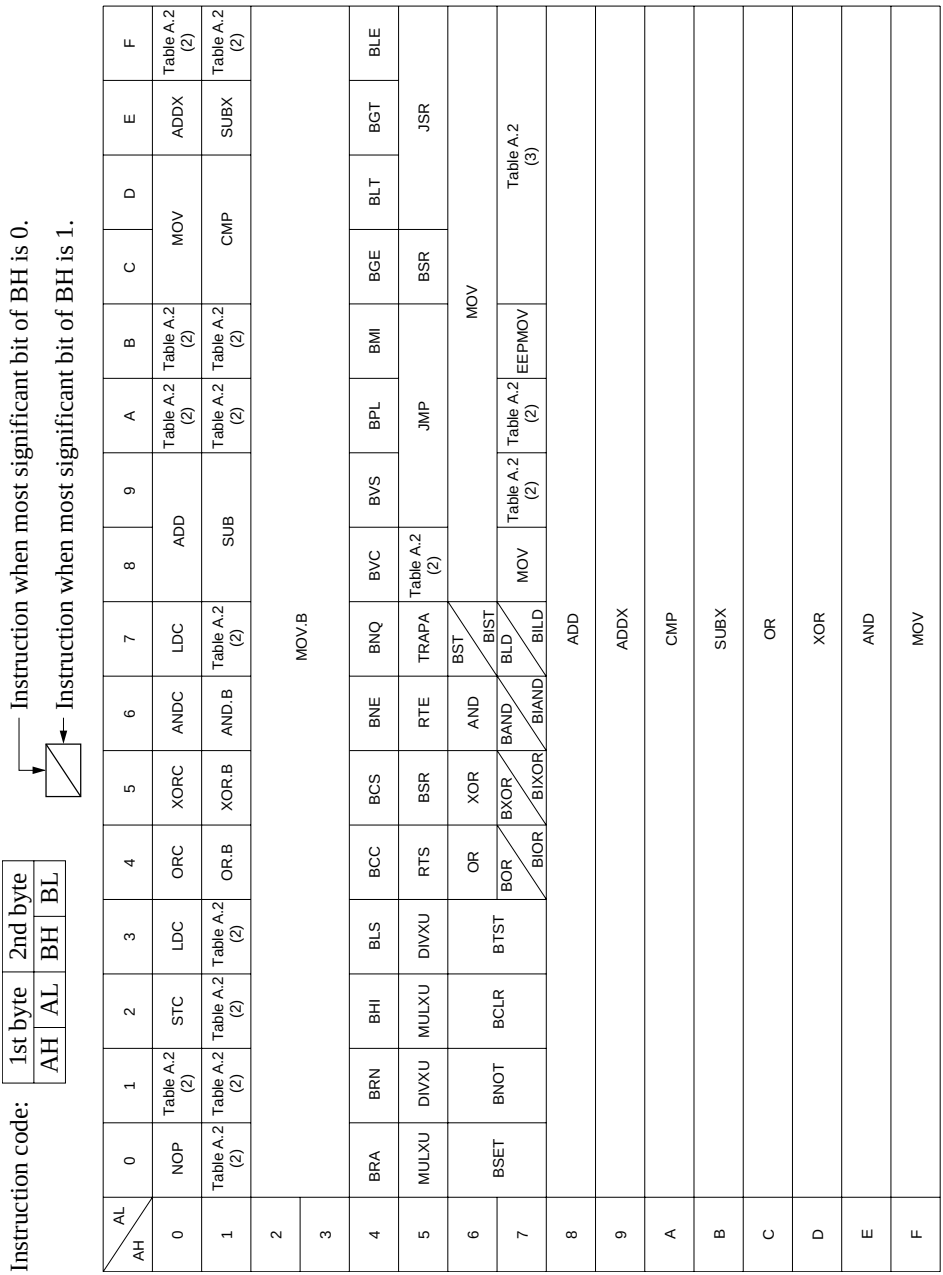


Figure 21.12 Basic Bus Cycle: Three-State Access

A.2 Operation Code Maps

Table A.2 Operation Code Map (1)



GRA2 H/L—General Register A2 H/L H'FFF7C, H'FFF7D 16-bit timer channel 2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

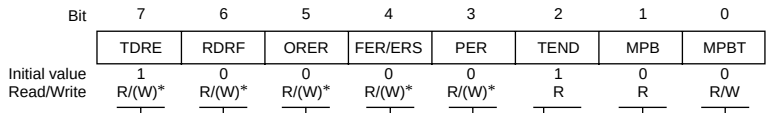
Note: Bit functions are the same as for 16-bit timer channel 0.

GRB2 H/L—General Register B2 H/L H'FFF7E, H'FFF7F 16-bit timer channel 2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for 16-bit timer channel 0.

SSR—Serial Status Register H'FFFB4 SCI0



Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER/ERS	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor bit transfer

0	Multiprocessor bit value in transmit data is 0
1	Multiprocessor bit value in transmit data is 1

Multiprocessor bit

0	Multiprocessor bit value in receive data is 0
1	Multiprocessor bit value in receive data is 1

Transmit end (for serial communication interface)

0	[Clearing condition] Read TDRE when TDRE = 1, then write 0 in TDRE.
1	[Setting conditions] • Reset or transition to standby mode • TE is cleared to 0 in SCR. • TDRE is 1 when last bit of 1-byte serial character is transmitted.

Transmit end (for smart card interface)

0	[Clearing condition] Read TDRE when TDRE = 1, then write 0 in TDRE.
1	[Setting conditions] • Reset or transition to standby mode • TE is cleared to 0 in SCR and FER/ERS is cleared to 0. • TDRE is 1 and FER/ERS is 0 (normal transmission) 2.5 etu* (when GM = 0) or 1.0 etu (when GM = 1) after 1-byte serial character is transmitted.

Note: * etu: Elementary time unit (time required to transmit one bit)

Parity error

0	[Clearing conditions]	• Reset or transition to standby mode • Read PER when PER = 1, then write 0 in PER.
1	[Setting condition]	Parity error (parity of receive data does not match parity setting of O/E bit in SMR)

Framing error (for serial communication interface)

0	[Clearing conditions]	• Reset or transition to standby mode • Read FER when FER = 1, then write 0 in FER.
1	[Setting condition]	Framing error (stop bit is 0)

Error signal status (for smart card interface)

0	[Clearing conditions]	• Reset or transition to standby mode • Read ERS when ERS = 1, then write 0 in ERS.
1	[Setting condition]	A low error signal is received.

Overrun error

0	[Clearing conditions]	• Reset or transition to standby mode • Read ORER when ORER = 1, then write 0 in ORER.
1	[Setting condition]	Overrun error (reception of the next serial data ends when RDRF = 1)

Receive data register full

0	[Clearing conditions]	• Reset or transition to standby mode • Read RDRF when RDRF = 1, then write 0 in RDRF.
1	[Setting condition]	Serial data is received normally and transferred from RSR to RDR.

Transmit data register empty

0	[Clearing condition]	• Read TDRE when TDRE = 1, then write 0 in TDRE.
1	[Setting conditions]	• Reset or transition to standby mode • TE is 0 in SCR. • Data is transferred from TDR to TSR, enabling new data to be written in TDR

Note: * Only 0 can be written, to clear the flag.

P3DR—Port 3 Data Register **H'FFFD2** **Port 3**

Bit	7	6	5	4	3	2	1	0
	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 3 pins

P4DR—Port 4 Data Register **H'FFFD3** **Port 4**

Bit	7	6	5	4	3	2	1	0
	$P4_7$	$P4_6$	$P4_5$	$P4_4$	$P4_3$	$P4_2$	$P4_1$	$P4_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 4 pins

P5DR—Port 5 Data Register **H'FFFD4** **Port 5**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Data for port 5 pins

P6DR—Port 6 Data Register **H'FFFD5** **Port 6**

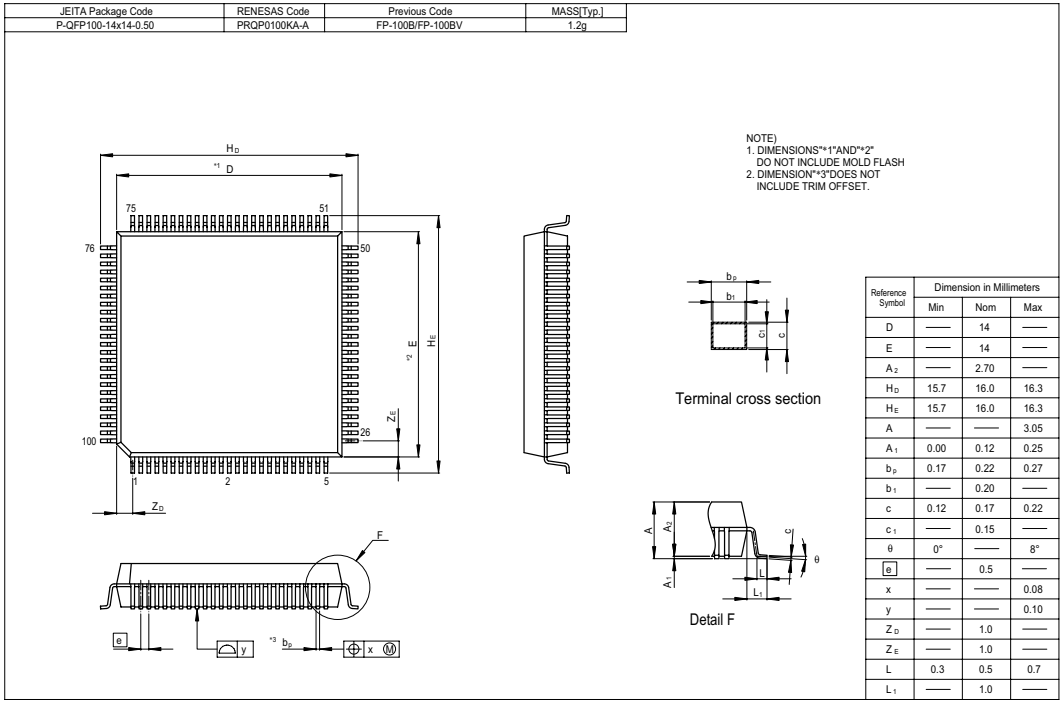
Bit	7	6	5	4	3	2	1	0
	$P6_7$	$P6_6$	$P6_5$	$P6_4$	$P6_3$	$P6_2$	$P6_1$	$P6_0$
Initial value	1	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 6 pins

Appendix G Package Dimensions

Figure G.1 shows the FP-100B package dimensions of the H8/3024 Group. Figure G.2 shows the TFP-100B package dimensions. Figure G.3 shows the FP-100A package dimensions.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x14-0.50	PRQP0100KA-A	FP-100B/FP-100BV	1.2g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	14	——
E	——	14	——
A_2	——	2.70	——
H_D	15.7	16.0	16.3
H_E	15.7	16.0	16.3
A	——	——	3.05
A_1	0.00	0.12	0.25
b_p	0.17	0.22	0.27
b_1	——	0.20	——
c	0.12	0.17	0.22
c_1	——	0.15	——
θ	0°	——	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.10
Z_D	——	1.0	——
Z_E	——	1.0	——
L	0.3	0.5	0.7
L_1	——	1.0	——

Figure G.1 Package Dimensions (FP-100B)

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