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18.10.1 Socket Adapters and Memory Map 571
18.10.2 Notes on Use of PROM Mode 572
18.11 Flash Memory Programming and Erasing Precautions 573
18.12 Notes when Converting the F-ZTAT Application Software to the Mask ROM Versions 579

Section 19 Clock Pulse Generator 581
19.1 Overview 581
19.1.1 Block Diagram 582
19.2 Oscillator Circuit 583
19.2.1 Connecting a Crystal Resonator 583
19.2.2 External Clock Input 585
19.3 Duty Adjustment Circuit 587
19.4 Prescalers 587
19.5 Frequency Divider 588
19.5.1 Register Configuration 588
19.5.2 Division Control Register (DIVCR) 588
19.5.3 Usage Notes 589

Section 20 Power-Down State 591
20.1 Overview 591
20.2 Register Configuration 593
20.2.1 System Control Register (SYSCR) 593
20.2.2 Module Standby Control Register H (MSTCRH) 595
20.2.3 Module Standby Control Register L (MSTCRL) 596
20.3 Sleep Mode 598
20.3.1 Transition to Sleep Mode 598
20.3.2 Exit from Sleep Mode 598
20.4 Software Standby Mode 598
20.4.1 Transition to Software Standby Mode 598
20.4.2 Exit from Software Standby Mode 599
20.4.3 Selection of Waiting Time for Exit from Software Standby Mode 599
20.4.4 Sample Application of Software Standby Mode 601
20.4.5 Usage Notes 601
20.5 Hardware Standby Mode 602
20.5.1 Transition to Hardware Standby Mode 602
20.5.2 Exit from Hardware Standby Mode 602
20.5.3 Timing for Hardware Standby Mode 603
20.6 Module Standby Function 604
20.6.1 Module Standby Timing 604
20.6.2 Read/Write in Module Standby 604
20.6.3 Usage Notes 604

Instruction	Size*	Function
BOR	B	C ∨ (<bit-No.> of <EAd>) → C ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BIOR	B	C ∨ [¬ (<bit-No.> of <EAd>)] → C ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C Exclusive-ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BIXOR	B	C ⊕ [¬ (<bit-No.> of <EAd>)] → C Exclusive-ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BLD	B	(<bit-No.> of <EAd>) → C Transfers a specified bit in a general register or memory operand to the carry flag. The bit number is specified by 3-bit immediate data.
BILD	B	¬ (<bit-No.> of <EAd>) → C Transfers the inverse of a specified bit in a general register or memory operand to the carry flag. The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>) Transfers the carry flag value to a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data.
BIST	B	C → ¬ (<bit-No.> of <EAd>) Transfers the inverse of the carry flag value to a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data.

Note: * Size refers to the operand size.
B: Byte

Bits 5 and 4—Area 6 Wait Control 1 and 0 (W61, W60): These bits select the number of program wait states when area 6 in external space is accessed while the AST6 bit in ASTCR is set to 1.

Bit 5 W61	Bit 4 W60	Description
0	0	Program wait not inserted when external space area 6 is accessed
	1	1 program wait state inserted when external space area 6 is accessed
1	0	2 program wait states inserted when external space area 6 is accessed
	1	3 program wait states inserted when external space area 6 is accessed (Initial value)

Bits 3 and 2—Area 5 Wait Control 1 and 0 (W51, W50): These bits select the number of program wait states when area 5 in external space is accessed while the AST5 bit in ASTCR is set to 1.

Bit 3 W51	Bit 2 W50	Description
0	0	Program wait not inserted when external space area 5 is accessed
	1	1 program wait state inserted when external space area 5 is accessed
1	0	2 program wait states inserted when external space area 5 is accessed
	1	3 program wait states inserted when external space area 5 is accessed (Initial value)

Bits 1 and 0—Area 4 Wait Control 1 and 0 (W41, W40): These bits select the number of program wait states when area 4 in external space is accessed while the AST4 bit in ASTCR is set to 1.

Bit 1 W41	Bit 0 W40	Description
0	0	Program wait not inserted when external space area 4 is accessed
	1	1 program wait state inserted when external space area 4 is accessed
1	0	2 program wait states inserted when external space area 4 is accessed
	1	3 program wait states inserted when external space area 4 is accessed (Initial value)

WCRL

Bit	7	6	5	4	3	2	1	0
	W31	W30	W21	W20	W11	W10	W01	W00
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 and 6—Area 3 Wait Control 1 and 0 (W31, W30): These bits select the number of program wait states when area 3 in external space is accessed while the AST3 bit in ASTCR is set to 1.

Bit 7 W31	Bit 6 W30	Description
0	0	Program wait not inserted when external space area 3 is accessed
	1	1 program wait state inserted when external space area 3 is accessed
1	0	2 program wait states inserted when external space area 3 is accessed
	1	3 program wait states inserted when external space area 3 is accessed (Initial value)

Bits 5 and 4—Area 2 Wait Control 1 and 0 (W21, W20): These bits select the number of program wait states when area 2 in external space is accessed while the AST2 bit in ASTCR is set to 1.

Bit 5 W21	Bit 4 W20	Description
0	0	Program wait not inserted when external space area 2 is accessed
	1	1 program wait state inserted when external space area 2 is accessed
1	0	2 program wait states inserted when external space area 2 is accessed
	1	3 program wait states inserted when external space area 2 is accessed (Initial value)

P1DDR is initialized to H'FF in modes 1 to 4, and to H'00 in modes 5 to 7, by a reset and in hardware standby mode. In sofware standby mode it retains its previous setting. Therefore, if a transition is made to software standby mode while port 1 is functioning as an input/output port and a P1DDR bit is set to 1, the corresponding pin maintains its output state.

Port 1 Data Register (P1DR): P1DR is an 8-bit readable/writable register that stores port 1 output data. When port 1 functions as an output port, the value of this register is output. When this register is read, the pin logic level is read for bits for which the P1DDR setting is 0, and the P1DR value is read for bits for which the P1DDR setting is 1.

Bit	7	6	5	4	3	2	1	0
	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 1 data 7 to 0
These bits store data for port 1 pins

P1DR is initialized to H'00 by a reset and in hardware standby mode. In software standby mode it retains its previous setting.

Port 3 Data Direction Register (P3DDR): P3DDR is an 8-bit write-only register that can select input or output for each pin in port 3.

Bit	7	6	5	4	3	2	1	0
	$P3_7DDR$	$P3_6DDR$	$P3_5DDR$	$P3_4DDR$	$P3_3DDR$	$P3_2DDR$	$P3_1DDR$	$P3_0DDR$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 3 data direction 7 to 0
These bits select input or output for port 3 pins

- Modes 1 to 5 (Expanded Modes)
  Port 3 functions as a data bus, regardless of the P3DDR settings.
- Modes 6 and 7 (Single-Chip Mode)
  Port 3 functions as an input/output port. A pin in port 3 becomes an output port if the corresponding P3DDR bit is set to 1, and an input port if this bit is cleared to 0.

P3DDR is a write-only register. Its value cannot be read. All bits return 1 when read.

P3DDR is initialized to H'00 by a reset and in hardware standby mode. In software standby mode it retains its previous setting. Therefore, if a transition is made to software standby mode while port 3 is functioning as an input/output port and a P3DDR bit is set to 1, the corresponding pin maintains its output state.

Port 3 Data Register (P3DR): P3DR is an 8-bit readable/writable register that stores output data for port 3. When port 3 functions as an output port, the value of this register is output. When a bit in P3DDR is set to 1, if port 3 is read the value of the corresponding P3DR bit is returned. When a bit in P3DDR is cleared to 0, if port 3 is read the corresponding pin logic level is read.

Bit	7	6	5	4	3	2	1	0
	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 3 data 7 to 0
These bits store data for port 3 pins

P3DR is initialized to H'00 by a reset and in hardware standby mode. In software standby mode it retains its previous setting.

Table 7.24 Port B Pin Functions (Modes 6 and 7)

Pin	Pin Functions and Selection Method

PB_7/TP_{15} Bit NDER15 in NDERB and bit PB_7DDR select the pin function as follows.

PB_7DDR	0	1	1
NDER15	—	0	1
Pin function	PB_7 input	PB_7 output	TP_{15} output

PB_6/TP_{14} Bit NDER14 in NDERB and bit PB_6DDR select the pin function as follows.

PB_6DDR	0	1	1
NDER14	—	0	1
Pin function	PB_6 input	PB_6 output	TP_{14} output

PB_5/TP_{13} Bit NDER13 in NDERB and bit PB_5DDR select the pin function as follows.

PB_5DDR	0	1	1
NDER13	—	0	1
Pin function	PB_5 input	PB_5 output	TP_{13} output

PB_4/TP_{12} Bit NDER12 in NDERB and bit PB_4DDR select the pin function as follows.

PB_4DDR	0	1	1
NDER12	—	0	1
Pin function	PB_4 input	PB_4 output	TP_{12} output

$PB_3/TP_{11}/TMIO_3$ Bits OIS3/2 and OS1/0 in 8TCSR3, bit NDER11 in NDERB, and bit PB_3DDR select the pin function as follows.

OIS3/2 and OS1/0	All 0			Not all 0
PB_3DDR	0	1	1	—
NDER11	—	0	1	—
Pin function	PB_3 input	PB_3 output	TP_{11} output	$TMIO_3$ output
	$TMIO_3$ input*			

Note: * $TMIO_3$ input when bit ICE = 1 in 8TCSR3.

Timing of Setting of Overflow Flag (OVF): OVF is set to 1 when 16TCNT overflows from H'FFFF to H'0000 or underflows from H'0000 to H'FFFF. Figure 8.35 shows the timing.

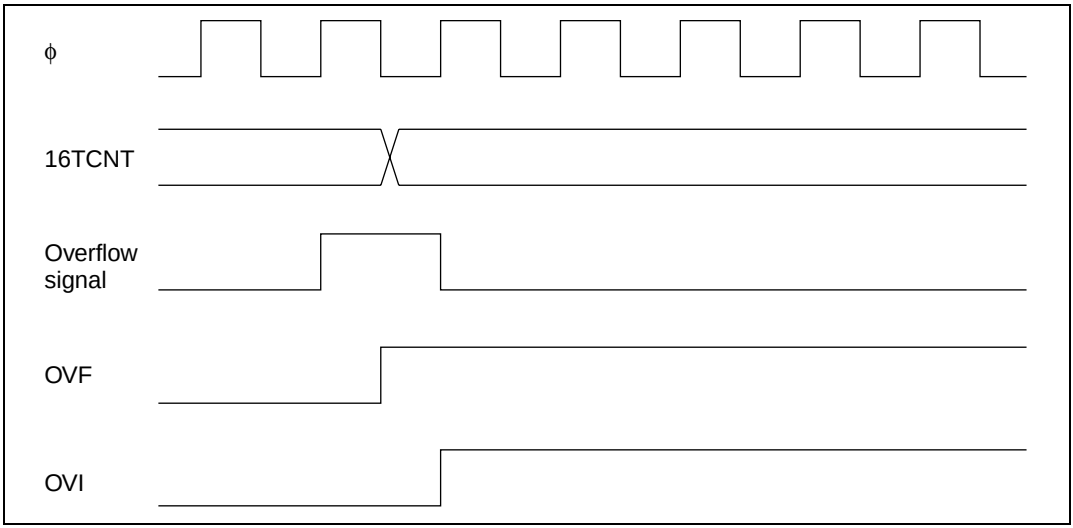


Figure 8.35 Timing of Setting of OVF

8.5.2 Timing of Clearing of Status Flags

If the CPU reads a status flag while it is set to 1, then writes 0 in the status flag, the status flag is cleared. Figure 8.36 shows the timing.

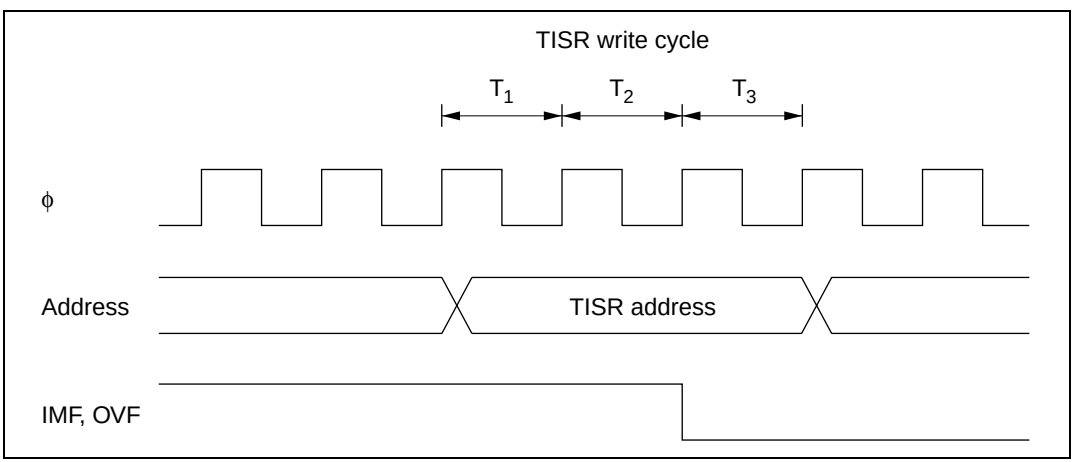


Figure 8.36 Timing of Clearing of Status Flags

9.3 CPU Interface

9.3.1 8-Bit Registers

8TCNT, TCORA, TCORB, 8TCR, and 8TCSR are 8-bit registers. These registers are connected to the CPU by an internal 16-bit data bus and can be read and written a word at a time or a byte at a time.

Figures 9.2 and 9.3 show the operation in word read and write accesses to 8TCNT.

Figures 9.4 to 9.7 show the operation in byte read and write accesses to 8TCNT0 and 8TCNT1.

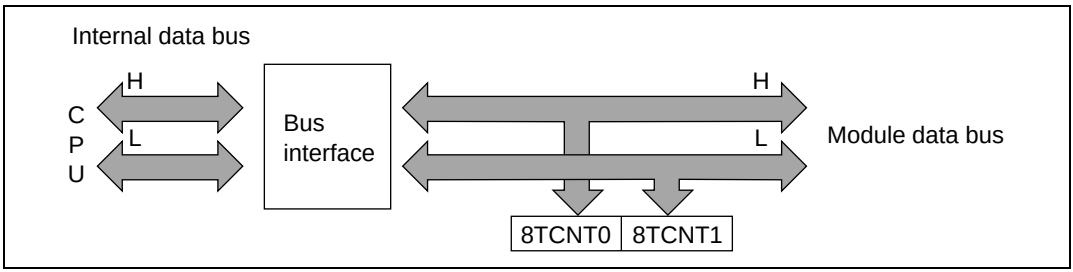


Figure 9.2 8TCNT Access Operation (CPU Writes to 8TCNT, Word)

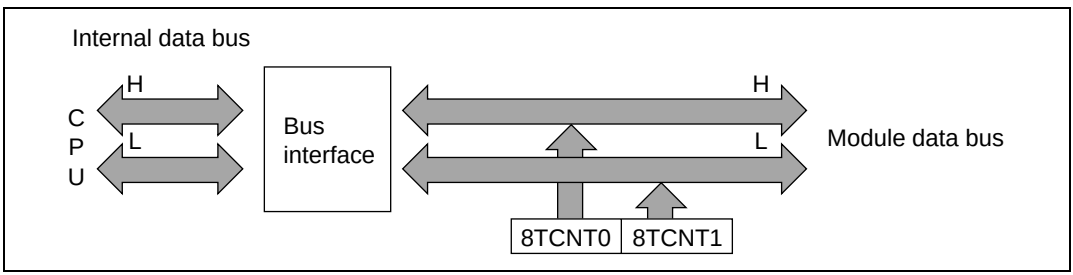


Figure 9.3 8TCNT Access Operation (CPU Reads 8TCNT, Word)

10.2.9 TPC Output Control Register (TPCR)

TPCR is an 8-bit readable/writable register that selects output trigger signals for TPC outputs on a group-by-group basis.

Bit	7	6	5	4	3	2	1	0
	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Group 3 compare match select 1 and 0
These bits select the compare match event that triggers TPC output group 3 (TP_{15} to TP_{12})

Group 2 compare match select 1 and 0
These bits select the compare match event that triggers TPC output group 2 (TP_{11} to TP_8)

Group 1 compare match select 1 and 0
These bits select the compare match event that triggers TPC output group 1 (TP_7 to TP_4)

Group 0 compare match select 1 and 0
These bits select the compare match event that triggers TPC output group 0 (TP_3 to TP_0)

TPCR is initialized to H'FF by a reset and in hardware standby mode. It is not initialized in software standby mode.

10.3.3 Normal TPC Output

Sample Setup Procedure for Normal TPC Output: Figure 10.4 shows a sample procedure for setting up normal TPC output.

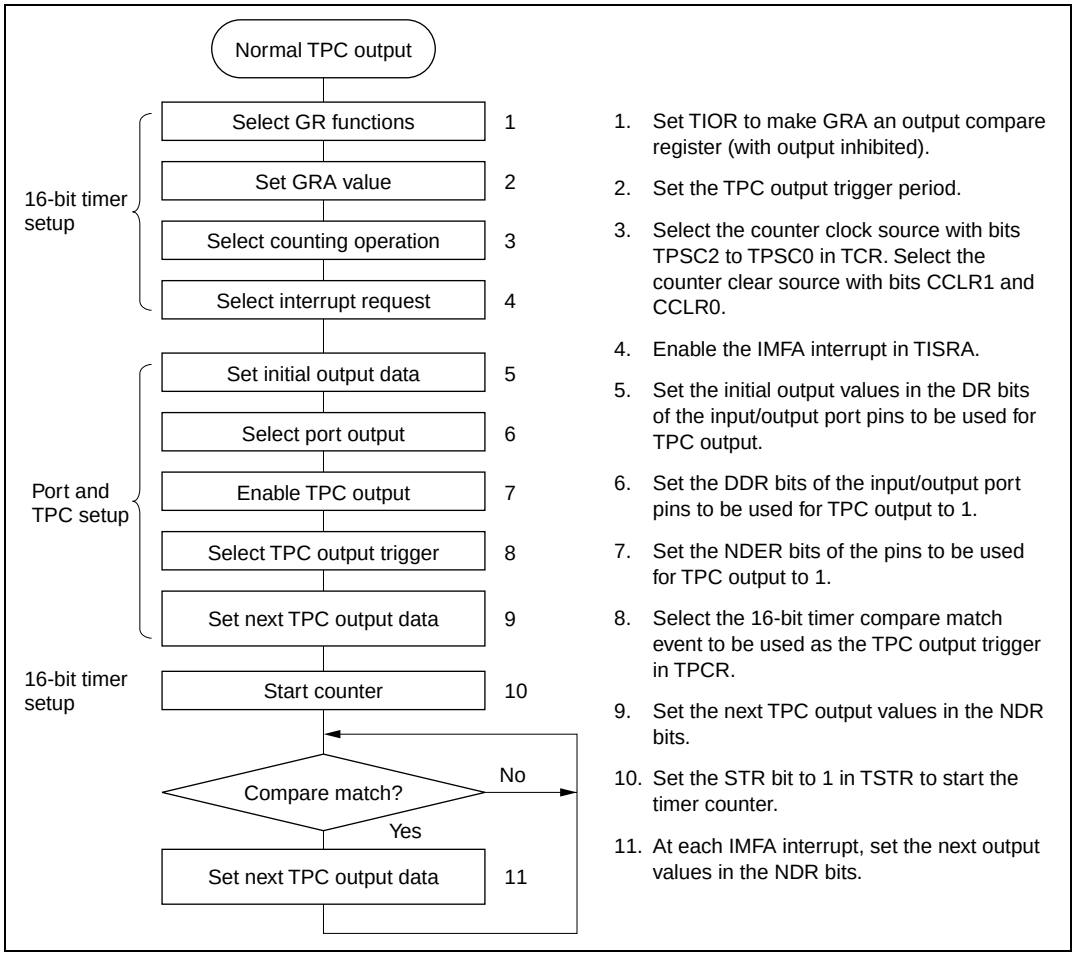
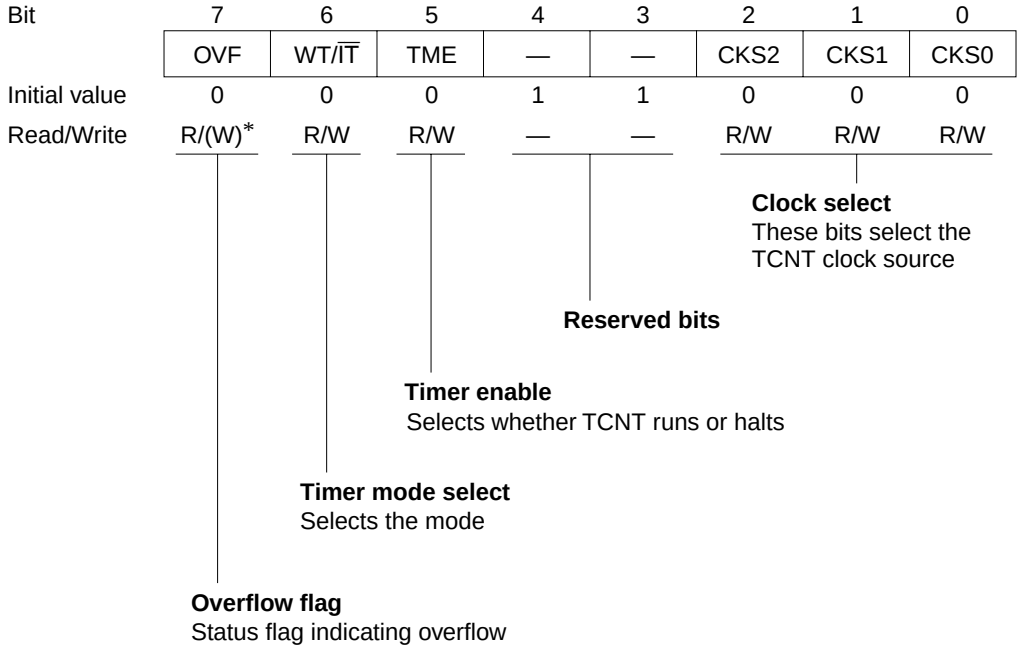


Figure 10.4 Setup Procedure for Normal TPC Output (Example)

11.2.2 Timer Control/Status Register (TCSR)

TCSR is an 8-bit readable and writable register. Its functions include selecting the timer mode and clock source.



Notes: The method for writing to TCSR is different from that for general registers to prevent inadvertent overwriting. For details see section 11.2.4, Notes on Register Access.

* Only 0 can be written, to clear the flag.

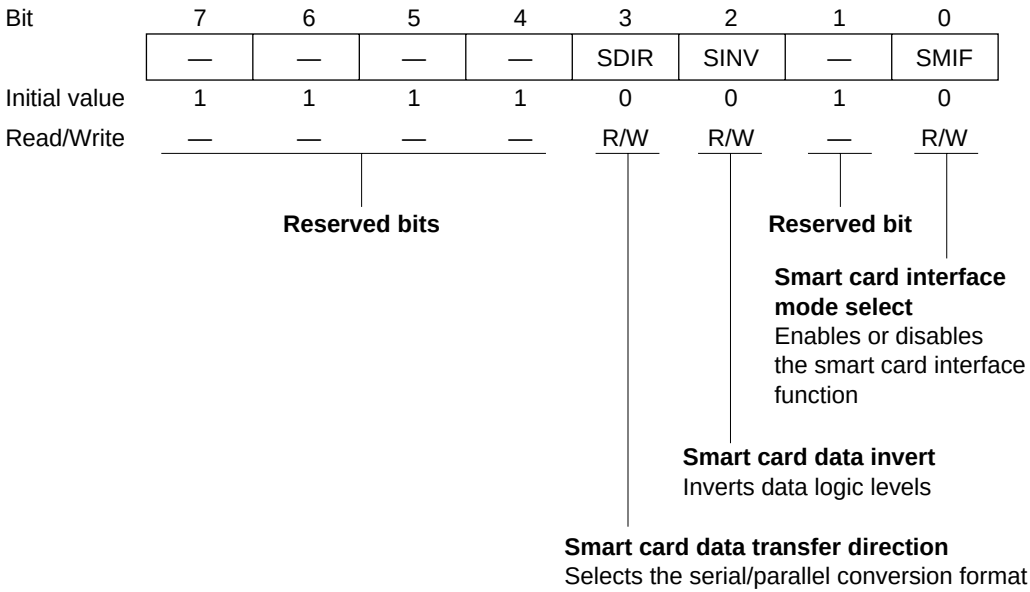
Bits 7 to 5 are initialized to 0 by a reset and in standby mode. Bits 2 to 0 are initialized to 0 by a reset. In software standby mode bits 2 to 0 are not initialized, but retain their previous values.

13.2 Register Descriptions

This section describes the new or modified registers and bit functions in the smart card interface.

13.2.1 Smart Card Mode Register (SCMR)

SCMR is an 8-bit readable/writable register that selects smart card interface functions.



SCMR is initialized to H'F2 by a reset and in standby mode.

Bits 7 to 4—Reserved: Read-only bits, always read as 1.

Bit 3—Smart Card Data Transfer Direction (SDIR): Selects the serial/parallel conversion format.*1

Bit 3 SDIR	Description	
0	TDR contents are transmitted LSB-first	(Initial value)
	Receive data is stored LSB-first in RDR	
1	TDR contents are transmitted MSB-first	
	Receive data is stored MSB-first in RDR	

Bit 7—Trigger Enable (TRGE): Enables or disables starting of A/D conversion by an external trigger or 8-bit timer compare match.

Bit 7 TRGE	Description
0	Starting of A/D conversion by an external trigger or 8-bit timer compare match is disabled (Initial value)
1	A/D conversion is started at the falling edge of the external trigger signal ($\overline{\text{ADTRG}}$) or by an 8-bit timer compare match

External trigger pin and 8-bit timer selection is performed by the 8-bit timer. For details, see section 9, 8-Bit Timers.

Bits 6 to 1—Reserved: These bits cannot be modified and are always read as 1.

Bit 0—Reserved: This bit can be read or written, but must not be set to 1.

14.3 CPU Interface

ADDRA to ADDRD are 16-bit registers, but they are connected to the CPU by an 8-bit data bus. Therefore, although the upper byte can be be accessed directly by the CPU, the lower byte is read through an 8-bit temporary register (TEMP).

An A/D data register is read as follows. When the upper byte is read, the upper-byte value is transferred directly to the CPU and the lower-byte value is transferred into TEMP. Next, when the lower byte is read, the TEMP contents are transferred to the CPU.

When reading an A/D data register, always read the upper byte before the lower byte. It is possible to read only the upper byte, but if only the lower byte is read, incorrect data may be obtained.

Figure 14.2 shows the data flow for access to an A/D data register.

Bit 1—Erase Mode (E): Selects erase mode transition or clearing. (Do not set the SWE, ESU, PSU, EV, PV, or P bit at the same time.)

Bit 1 E	Description	
0	Erase mode cleared	(Initial value)
1	Transition to erase mode [Setting condition] When FWE = 1, SWE = 1, and ESU = 1	

Note: Do not access the flash memory while the E bit is set.

Bit 0—Program (P): Selects program mode transition or clearing. (Do not set the SWE, ESU, PSU, EV, PV, or E bit at the same time.)

Bit 0 P	Description	
0	Program mode cleared	(Initial value)
1	Transition to program mode [Setting condition] When FWE = 1, SWE = 1, and PSU = 1	

Note: Do not access the flash memory while the P bit is set.

17.3.2 Flash Memory Control Register 2 (FLMCR2)

Bit	7	6	5	4	3	2	1	0
	FLER	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

FLMCR2 is an 8-bit register used for flash memory operating mode control. FLMCR2 is initialized to H'00 by a reset, and in hardware standby mode and software standby mode. When the on-chip flash memory is disabled, a read will return H'00.

Note: FLMCR2 is a read-only register, and should not be written to.

17.4 Overview of Operation

17.4.1 Mode Transitions

When the mode pins and the FWE pin are set in the reset state and a reset-start is executed, the H8/3026F-ZTAT version enters one of the operating modes shown in figure 17.2. In user mode, flash memory can be read but not programmed or erased.

Flash memory can be programmed and erased in boot mode, user program mode, and PROM mode.

Boot mode and user program mode cannot be used in the H8/3026F-ZTAT version's mode 6 (normal mode with on-chip ROM enabled).

3. FWE application/disconnection

FWE application should be carried out when MCU operation is in a stable condition. If MCU operation is not stable, fix the FWE pin low and set the protection state.

The following points must be observed concerning FWE application and disconnection to prevent unintentional programming or erasing of flash memory:

- Apply FWE when the V_{CC} voltage has stabilized within its rated voltage range.

  If FWE is applied when the MCU's V_{CC} power supply is not within its rated voltage range, MCU operation will be unstable and flash memory may be erroneously programmed or erased.
- Apply FWE when oscillation has stabilized (after the elapse of the oscillation settling time).

  When V_{CC} power is turned on, hold the $\overline{RES}$ pin low for the duration of the oscillation settling time before applying FWE. Do not apply FWE when oscillation has stopped or is unstable.
- In boot mode, apply and disconnect FWE during a reset.

  In a transition to boot mode, FWE = 1 input and MD_2–MD_0 setting should be performed while the $\overline{RES}$ input is low. FWE and MD_2–MD_0 pin input must satisfy the mode programming setup time (t_{MDS}) with respect to the reset release timing. When making a transition from boot mode to another mode, also, a mode programming setup time is necessary with respect to the reset release timing.

  In a reset during operation, the $\overline{RES}$ pin must be held low for a minimum of 20 system clock cycles.
- In user program mode, FWE can be switched between high and low level regardless of $\overline{RES}$ input.

  FWE input can also be switched during execution of a program in flash memory.
- Do not apply FWE if program runaway has occurred.

  During FWE application, the program execution state must be monitored using the watchdog timer or some other means.
- Disconnect FWE only when the SWE, ESU, PSU, EV, PV, E, and P bits in FLMCR1 are cleared.

  Make sure that the SWE, ESU, PSU, EV, PV, E, and P bits are not set by mistake when applying or disconnecting FWE.

2. Given current consumption values are when all the output pins are made to unloaded state and, furthermore, when the on-chip pull-up MOS is turned off under conditions that V_{IH} min = V_{CC} – 0.5 V and V_{IL} max = 0.5 V.
   Also, the aforesaid current consumption values are when V_{IH} min = $V_{CC} \times 0.9$ and V_{IL} max = 0.3 V under the condition of $V_{RAM} \leq V_{CC} < 3.0$ V.
3. I_{CC} max. (under normal operations) = 3.0 (mA) + 0.61 (mA/(MHz × V)) × V_{CC} × f
   I_{CC} max. (when using the sleeve) = 3.0 (mA) + 0.49 (mA/(MHz × V)) × V_{CC} x f
   I_{CC} max. (when the sleeve + module are standing by)
   = 3.0 (mA) + 0.38 (mA/(MHz × V)) × V_{CC} × f
   Also, the typ. values for current dissipation are reference values.

Table 21.12 Permissible Output Currents

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{REF} = 3.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, 2, and 5	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 20 pins in Ports 1, 2, and 5	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$\lvert -I_{OH} \rvert$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\lvert -\Sigma I_{OH} \rvert$	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 21.12.
2. When directly driving a darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 21.4 and 21.5.

16TCR2 Timer Control Register 2 H'FFF78 16-bit timer channel 2

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Notes: 1. Bit functions are the same as for 16-bit timer channel 0.
2. When phase counting mode is selected in channel 2, the settings of bits CKEG1 and CKEG0 and TPSC2 to TPSC0 in 16TCR2 are ignored.

TIOR2—Timer I/O Control Register 2 H'FFF79 16-bit timer channel 2

Bit	7	6	5	4	3	2	1	0
	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
Initial value	1	0	0	0	1	0	0	0
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Note: Bit functions are the same as for 16-bit timer channel 0.

16TCNT2 H/L—Timer Counter 2 H/L H'FFF7A, H'FFF7B 16-bit timer channel 2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Phase counting mode : up/down counter
Other mode : up-counter

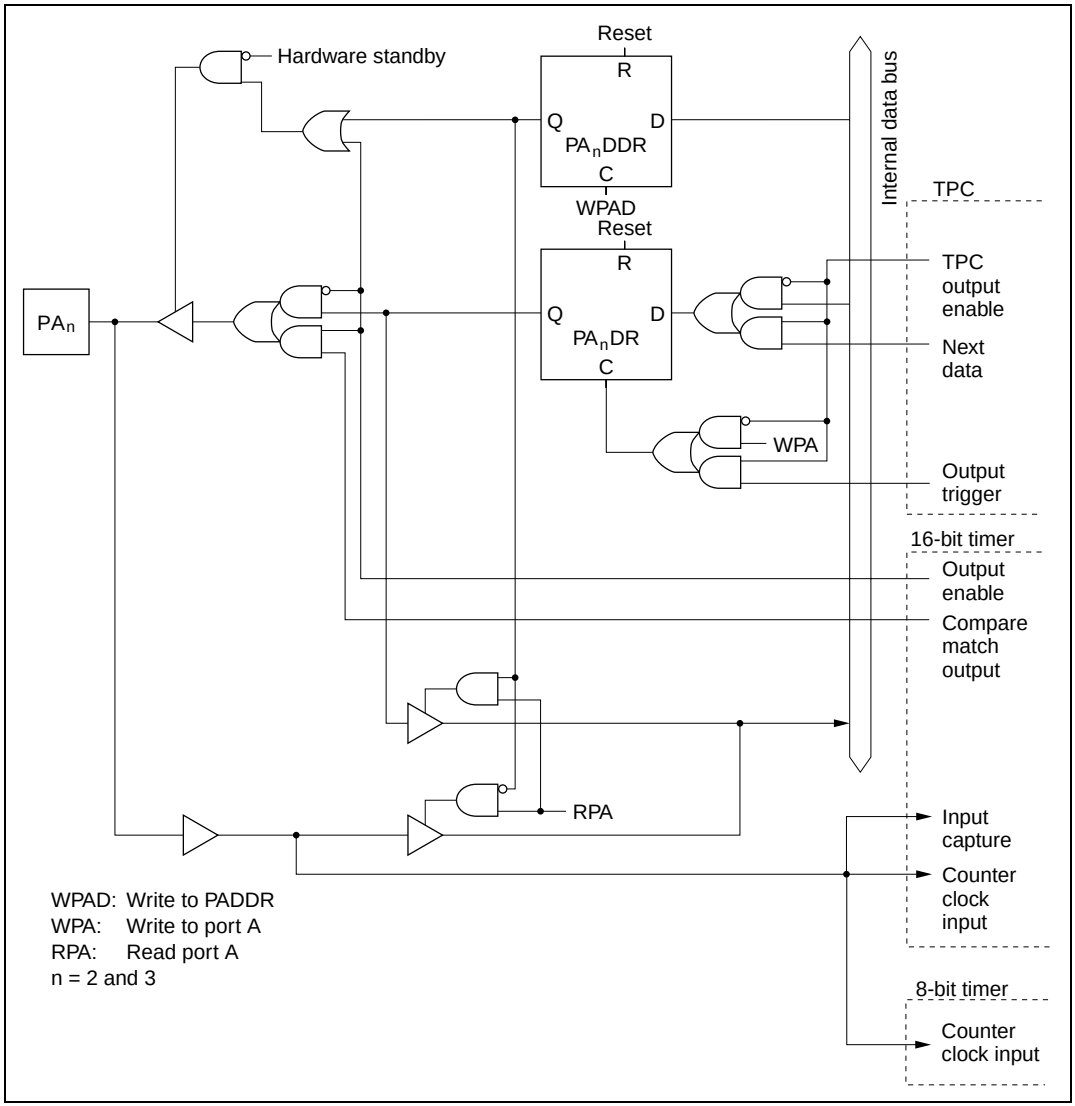


Figure C.10 (b) Port A Block Diagram (Pins PA_2 and PA_3)