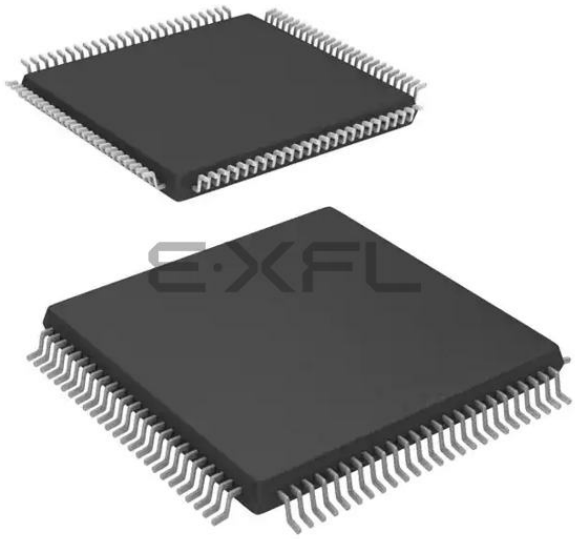

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	PWM, WDT
Number of I/O	70
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3026xbl25v

Section 1 Overview

1.1 Overview

The H8/3024 Group is a series of microcontrollers (MCUs) that integrate system supporting functions together with an H8/300H CPU core having an original Renesas Technology architecture.

The H8/300H CPU has a 32-bit internal architecture with sixteen 16-bit general registers, and a concise, optimized instruction set designed for speed. It can address a 16-Mbyte linear address space. Its instruction set is upward-compatible at the object-code level with the H8/300 CPU, enabling easy porting of software from the H8/300 Series.

The on-chip system supporting functions include ROM, RAM, a 16-bit timer, an 8-bit timer, a programmable timing pattern controller (TPC), a watchdog timer (WDT), a serial communication interface (SCI), an A/D converter, a D/A converter, I/O ports, and other facilities.

The four members of the H8/3024 Group are the H8/3024F-ZTAT, H8/3026F-ZTAT, H8/3024 (mask ROM version), and H8/3026 (mask ROM version).

Seven MCU operating modes offer a choice of bus width and address space size. The modes (modes 1 to 7) include two single-chip modes and five expanded modes.

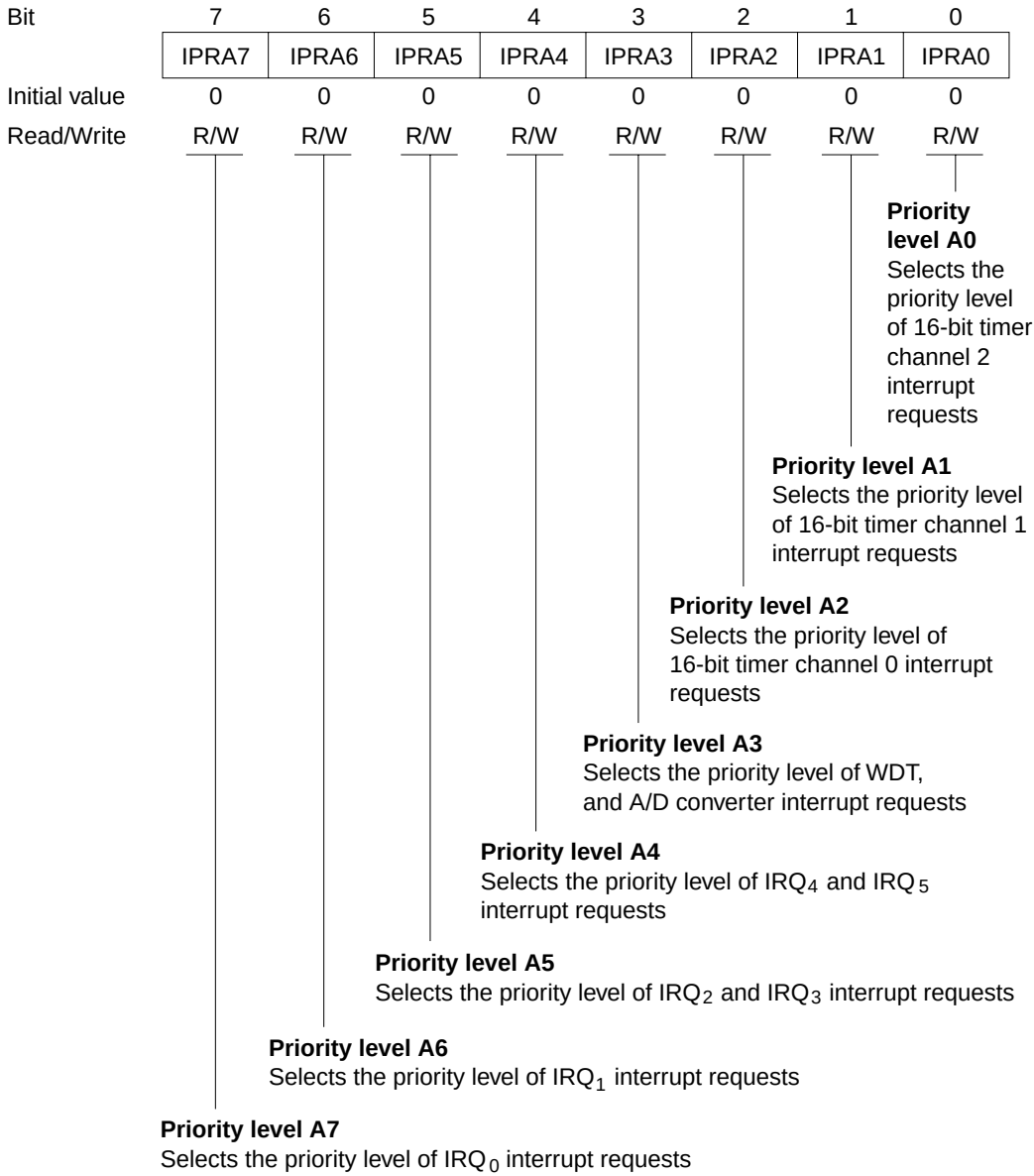
In addition to its mask ROM versions, the H8/3024 Group has F-ZTAT™* versions with on-chip flash memory that allows programs to be freely rewritten by the user. This version enables users to respond quickly and flexibly to changing application specifications, growing production volumes, and other conditions.

Table 1.1 summarizes the features of the H8/3024 Group.

Note: * F-ZTAT™ (Flexible ZTAT) is a trademark of Renesas Technology Corp.

Interrupt Priority Register A (IPRA)

IPRA is an 8-bit readable/writable register in which interrupt priority levels can be set.



IPRA is initialized to H'00 by a reset and in hardware standby mode.

Pin	Pin Functions and Selection Method
$PA_6/TP_6/TIOCA_2/A_{21}$	Bit PWM2 in TMDR, bits IOA2 to IOA0 in TIOR2, bit NDER6 in NDERA, bit A21E in BRCR, and bit PA_6DDR select the pin function as follows.

A21E	1				0
16-bit timer channel 2 settings	(1) in table below	(2) in table below			—
PA_6DDR	—	0	1	1	—
NDER6	—	—	0	1	—
Pin function	$TIOCA_2$ output	PA_6 input	PA_6 output	TP_6 output	A_{21} output
		$TIOCA_2$ input*			

Note: * $TIOCA_2$ input when IOA2 = 1.

16-bit timer channel 2 settings	(2)	(1)		(2)	(1)
PWM2	0				1
IOA2	0			1	—
IOA1	0	0	1	—	—
IOA0	0	1	—	—	—

$PA_5/TP_5/TIOCB_1/A_{22}$	Bit PWM1 in TMDR, bits IOB2 to IOB0 in TIOR1, bit NDER5 in NDERA, bit A22E in BRCR, and bit PA_5DDR select the pin function as follows.

A22E	1				0
16-bit timer channel 1 settings	(1) in table below	(2) in table below			—
PA_5DDR	—	0	1	1	—
NDER5	—	—	0	1	—
Pin function	$TIOCB_1$ output	PA_5 input	PA_5 output	TP_5 output	A_{22} output
		$TIOCB_1$ input*			

Note: * $TIOCB_1$ input when IOB2 = 1 and PWM1 = 0.

16-bit timer channel 1 settings	(2)	(1)		(2)
IOB2	0			1
IOB1	0	0	1	—
IOB0	0	1	—	—

Pin	Pin Functions and Selection Method
$PA_2/TP_2/TIOCA_0/TCLKC$	Bit PWM0 in TMDR, bits IOA2 to IOA0 in TIOR0, bits TPSC2 to TPSC0 in 16TCR2 to 16TCR0 of the 16-bit timer, bits CKS2 to CKS0 in 8TCR0 of the 8-bit timer, bit NDER2 in NDERA, and bit PA_2DDR select the pin function as follows.

16-bit timer channel 0 settings	(1) in table below	(2) in table below		
PA_2DDR	—	0	1	1
NDER2	—	—	0	1
Pin function	$TIOCA_0$ output	PA_2 input	PA_2 output	TP_2 output
		$TIOCA_0$ input*1		
	TCLKC input*2			

Notes: 1. $TIOCA_0$ input when IOA2 = 1.

2. TCLKC input when TPSC2 = TPSC1 = 1 and TPSC0 = 0 in any of 16TCR2 to 16TCR0, or bits CKS2 to CKS0 in 8TCR0 are as shown in (3) in the table below.

16-bit timer channel 0 settings	(2)	(1)		(2)	(1)
PWM0	0				1
IOA2	0			1	—
IOA1	0	0	1	—	—
IOA0	0	1	—	—	—

8-bit timer channel 0 settings	(4)	(3)		
CKS2	0	1		
CKS1	—	0		1
CKS0	—	0	1	—

7.12.2 Register Descriptions

Table 7.22 summarizes the registers of port B.

Table 7.22 Port B Registers

Address*	Name	Abbreviation	R/W	Initial Value
H'EE00A	Port B data direction register	PBDDR	W	H'00
H'FFFDA	Port B data register	PBDR	R/W	H'00

Note: * Lower 20 bits of the address in advanced mode.

Port B Data Direction Register (PBDDR): PBDDR is an 8-bit write-only register that can select input or output for each pin in port B. When pins are used for TPC output, the corresponding PBDDR bits must also be set.

Bit	7	6	5	4	3	2	1	0
	PB_7DDR	PB_6DDR	PB_5DDR	PB_4DDR	PB_3DDR	PB_2DDR	PB_1DDR	PB_0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port B data direction 7 to 0
These bits select input or output for port B pins

The pin functions that can be selected for port B differ between modes 1 to 5, and modes 6 and 7. For the method of selecting the pin functions, see tables 7.23 and 7.24.

When port B functions as an input/output port, a pin in port B becomes an output port if the corresponding PBDDR bit is set to 1, and an input port if this bit is cleared to 0.

PBDDR is a write-only register. Its value cannot be read. All bits return 1 when read.

PBDDR is initialized to H'00 by a reset and in hardware standby mode. In software standby mode it retains its previous setting. Therefore, if a transition is made to software standby mode while port B is functioning as an input/output port and a PBDDR bit is set to 1, the corresponding pin maintains its output state.

Section 9 8-Bit Timers

9.1 Overview

The H8/3024 Group has a built-in 8-bit timer module with four channels (TMR0, TMR1, TMR2, and TMR3), based on 8-bit counters. Each channel has an 8-bit timer counter (8TCNT) and two 8-bit time constant registers (TCORA and TCORB) that are constantly compared with the 8TCNT value to detect compare match events. The timers can be used as multifunctional timers in a variety of applications, including the generation of a rectangular-wave output with an arbitrary duty cycle.

9.1.1 Features

The features of the 8-bit timer module are listed below.

- Selection of four clock sources
  The counters can be driven by one of three internal clock signals (φ/8, φ/64, or φ/8192) or an external clock input (enabling use as an external event counter).
- Selection of three ways to clear the counters
  The counters can be cleared on compare match A or B, or input capture B.
- Timer output controlled by two compare match signals
  The timer output signal in each channel is controlled by two independent compare match signals, enabling the timer to generate output waveforms with an arbitrary duty cycle or PWM output.
- A/D converter can be activated by a compare match
- Two channels can be cascaded
  - Channels 0 and 1 can be operated as the upper and lower halves of a 16-bit timer (16-bit count mode).
  - Channels 2 and 3 can be operated as the upper and lower halves of a 16-bit timer (16-bit count mode).
  - Channel 1 can count channel 0 compare match events (compare match count mode).
  - Channel 3 can count channel 2 compare match events (compare match count mode).
- Input capture function can be set
  8-bit or 16-bit input capture operation is available.

Bits 3 and 2—Group 1 Compare Match Select 1 and 0 (G1CMS1, G1CMS0): These bits select the compare match event that triggers TPC output group 1 (TP_7 to TP_4).

Bit 3 G1CMS1	Bit 2 G1CMS0	Description
0	0	TPC output group 1 (TP_7 to TP_4) is triggered by compare match in 16-bit timer channel 0
	1	TPC output group 1 (TP_7 to TP_4) is triggered by compare match in 16-bit timer channel 1
1	0	TPC output group 1 (TP_7 to TP_4) is triggered by compare match in 16-bit timer channel 2
	1	TPC output group 1 (TP_7 to TP_4) is triggered by compare match in 16-bit timer channel 2 (Initial value)

Bits 1 and 0—Group 0 Compare Match Select 1 and 0 (G0CMS1, G0CMS0): These bits select the compare match event that triggers TPC output group 0 (TP_3 to TP_0).

Bit 1 G0CMS1	Bit 0 G0CMS0	Description
0	0	TPC output group 0 (TP_3 to TP_0) is triggered by compare match in 16-bit timer channel 0
	1	TPC output group 0 (TP_3 to TP_0) is triggered by compare match in 16-bit timer channel 1
1	0	TPC output group 0 (TP_3 to TP_0) is triggered by compare match in 16-bit timer channel 2
	1	TPC output group 0 (TP_3 to TP_0) is triggered by compare match in 16-bit timer channel 2 (Initial value)

10.3.3 Normal TPC Output

Sample Setup Procedure for Normal TPC Output: Figure 10.4 shows a sample procedure for setting up normal TPC output.

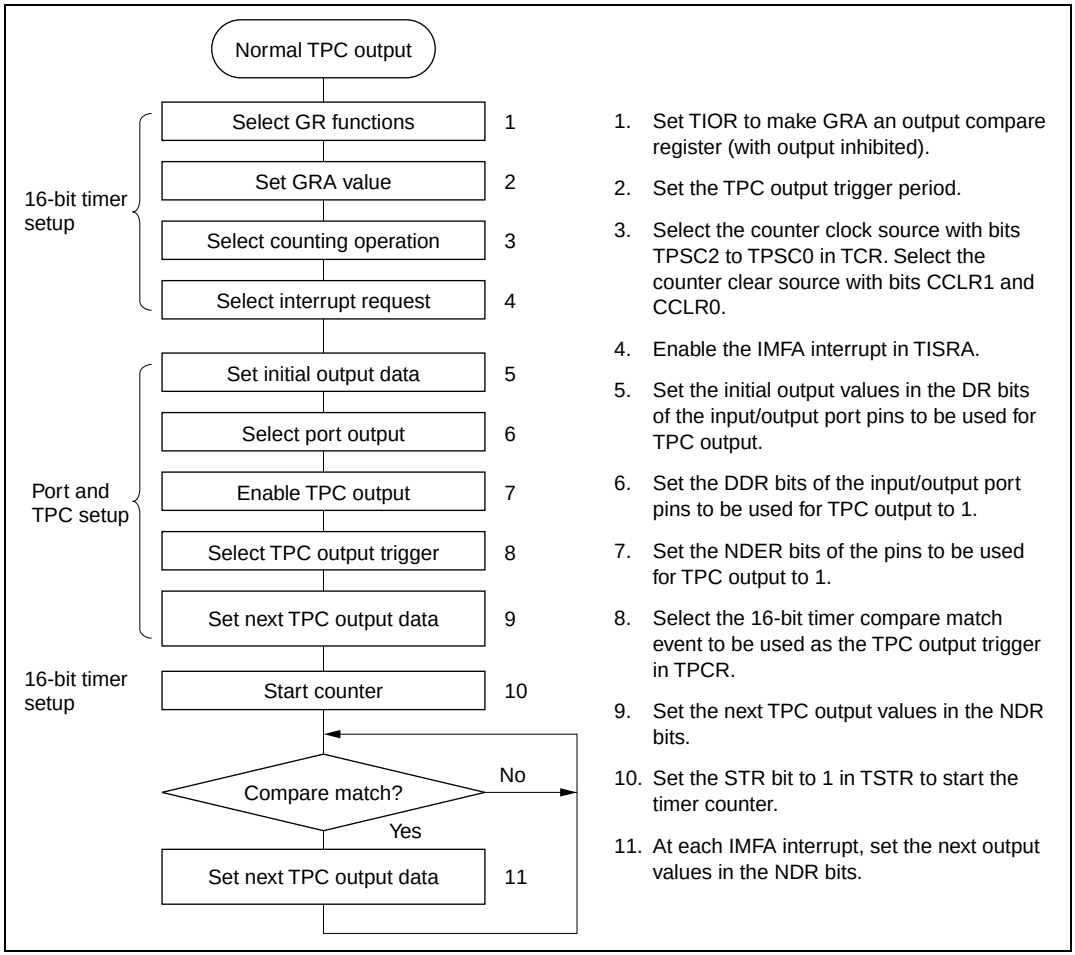


Figure 10.4 Setup Procedure for Normal TPC Output (Example)

Bit 4—Parity Mode (O/$\overline{E}$): Specifies whether even parity or odd parity is used for parity addition and checking. The O/$\overline{E}$ bit setting is only valid when the PE bit is set to 1, enabling parity bit addition and checking, in asynchronous mode. The O/$\overline{E}$ bit setting is ignored in synchronous mode, or when parity addition and checking is disabled in asynchronous mode.

Bit 4 O/$\overline{E}$	Description	
0	Even parity*1	(Initial value)
1	Odd parity*2	

Notes: 1. When even parity is selected, the parity bit added to transmit data makes an even number of 1s in the transmitted character and parity bit combined. Receive data must have an even number of 1s in the received character and parity bit combined.
2. When odd parity is selected, the parity bit added to transmit data makes an odd number of 1s in the transmitted character and parity bit combined. Receive data must have an odd number of 1s in the received character and parity bit combined.

Bit 3—Stop Bit Length (STOP): Selects one or two stop bits in asynchronous mode. This setting is used only in asynchronous mode. In synchronous mod no stop bit is added, so the STOP bit setting is ignored.

Bit 3 STOP	Description	
0	1 stop bit*1	(Initial value)
1	2 stop bits*2	

Notes: 1. One stop bit (with value 1) is added to the end of each transmitted character.
2. Two stop bits (with value 1) are added to the end of each transmitted character.

In receiving, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit. If the second stop bit is 0, it is treated as the start bit of the next incoming character.

13.3.6 Transmitting and Receiving Data

Initialization: Before transmitting or receiving data, the smart card interface must be initialized as described below. Initialization is also necessary when switching from transmit mode to receive mode, or vice versa.

1. Clear the TE and RE bits to 0 in the serial control register (SCR).
2. Clear error flags ERS, PER, and ORER to 0 in the serial status register (SSR).
3. Set the parity bit (O/$\overline{\text{E}}$) and baud rate generator select bits (CKS1 and CKS0) in the serial mode register (SMR). Clear the C/$\overline{\text{A}}$, CHR, and MP bits to 0, and set the STOP and PE bits to 1.
4. Set the SMIF, SDIR, and SINV bits in the smart card mode register (SCMR).
   When the SMIF bit is set to 1, the TxD pin and RxD pin are both switched from port to SCI pin functions and go to the high-impedance state.
5. Set a value corresponding to the desired bit rate in the bit rate register (BRR).
6. Set the CKE0 bit in SCR. Clear the TIE, RIE, TE, RE, MPIE, TEIE, and CKE1 bits to 0. If the CKE0 bit is set to 1, the clock is output from the SCK pin.
7. Wait at least one bit interval, then set the TIE, RIE, TE, and RE bits in SCR. Do not set the TE bit and RE bit at the same time, except for self-diagnosis.

Transmitting Serial Data: As data transmission in smart card mode involves error signal sampling and retransmission processing, the processing procedure is different from that for the normal SCI. Figure 13.5 shows a sample transmission processing flowchart.

1. Perform smart card interface mode initialization as described in Initialization above.
2. Check that the ERS error flag is cleared to 0 in SSR.
3. Repeat steps 2 and 3 until it can be confirmed that the TEND flag is set to 1 in SSR.
4. Write the transmit data in TDR, clear the TDRE flag to 0, and perform the transmit operation. The TEND flag is cleared to 0.
5. To continue transmitting data, go back to step 2.
6. To end transmission, clear the TE bit to 0.

The above processing may include interrupt handling.

If transmission ends and the TEND flag is set to 1 while the TIE bit is set to 1 and interrupt requests are enabled, a transmit-data-empty interrupt (TXI) will be requested. If an error occurs in transmission and the ERS flag is set to 1 while the RIE bit is set to 1 and interrupt requests are enabled, a transmit/receive-error interrupt (ERI) will be requested.

Bit 1—Erase Mode (E): Selects erase mode transition or clearing. (Do not set the SWE, ESU, PSU, EV, PV, or P bit at the same time.)

Bit 1 E	Description	
0	Erase mode cleared	(Initial value)
1	Transition to erase mode [Setting condition] When FWE = 1, SWE = 1, and ESU = 1	

Note: Do not access the flash memory while the E bit is set.

Bit 0—Program (P): Selects program mode transition or clearing. (Do not set the SWE, ESU, PSU, EV, PV, or E bit at the same time.)

Bit 0 P	Description	
0	Program mode cleared	(Initial value)
1	Transition to program mode [Setting condition] When FWE = 1, SWE = 1, and PSU = 1	

Note: Do not access the flash memory while the P bit is set.

18.3.2 Flash Memory Control Register 2 (FLMCR2)

Bit	7	6	5	4	3	2	1	0
	FLER	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

FLMCR2 is an 8-bit register used for flash memory operating mode control. FLMCR2 is initialized to H'00 by a reset, and in hardware standby mode and software standby mode. When the on-chip flash memory is disabled, a read will return H'00.

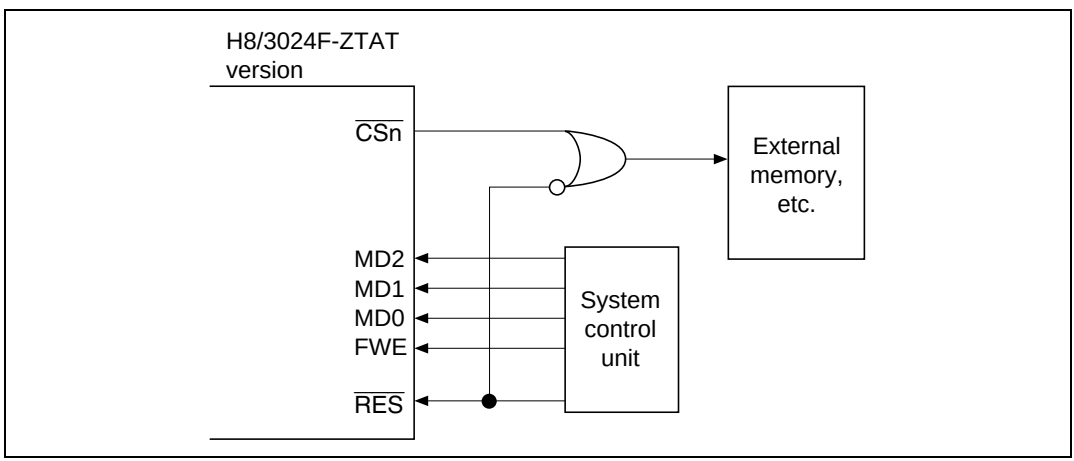
Note: FLMCR2 is a read-only register, and should not be written to.

(BRR). The transmit data output pin, TxD_1, goes to the high-level output state ($P9_1DDR$ = 1 in P9DDR, $P9_1DR$ = 1 in P9DR).

The contents of the CPU's internal general registers are undefined at this time, so these registers must be initialized immediately after branching to the user program. In particular, since the stack pointer (SP) is used implicitly in subroutine calls, etc., a stack area must be specified for use by the user program.

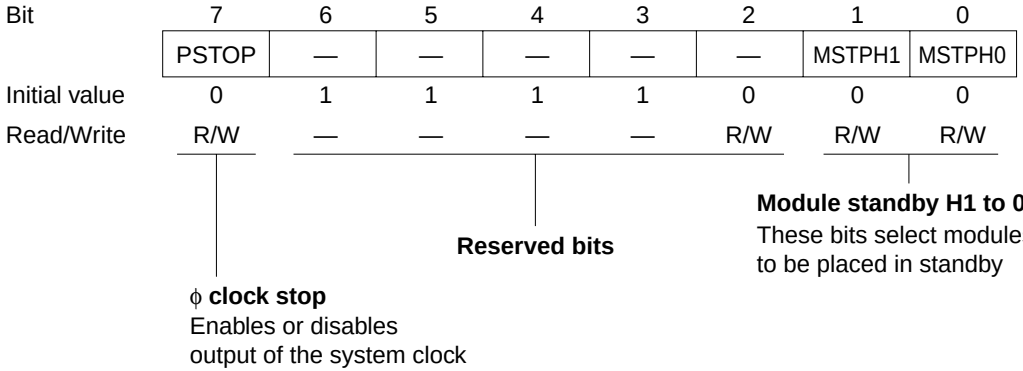
The initial values of other on-chip registers are not changed.

6. Boot mode can be entered by setting pins MD_0 to MD_2 and FWE in accordance with the mode setting conditions shown in table 18.6, and then executing a reset-start.
   a. When switching from boot mode to normal mode, the boot mode state within the chip must first be cleared by reset input via the $\overline{RES}$ pin*1. The $\overline{RES}$ pin must be held low for at least 20 system clock cycles.*2
   b. Do not change the input levels of the mode pins (MD_2 to MD_0) or the FWE pin in boot mode. To change the mode, the $\overline{RES}$ pin must first be driven low to set the reset state. Also, if a watchdog timer reset occurs in the boot mode state, the MCU's internal state will not be cleared, and the on-chip boot program will be restarted regardless of the mode pin states.
   c. The FWE pin must not be driven low while the boot program is running or flash memory is being programmed or erased.*3
7. If the mode pin input levels are changed (for example, from low to high) during a reset, the state of ports with multiplexed address functions and bus control output signals ($\overline{CSn}$, $\overline{AS}$, $\overline{RD}$, $\overline{LWR}$, $\overline{HWR}$) may also change according to the change in the MCU's operating mode. Therefore, care must be taken to make pin settings to prevent these pins from being used directly as output signal pins during a reset, or to prevent collision with signals outside the MCU.



20.2.2 Module Standby Control Register H (MSTCRH)

MSTCRH is an 8-bit readable/writable register that controls output of the system clock (ϕ). It also controls the module standby function, which places individual on-chip supporting modules in the standby state. Module standby can be designated for the SCI0, SCI1.



MSTCRH is initialized to H'78 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—ϕ Clock Stop (PSTOP): Enables or disables output of the system clock (ϕ).

Bit 7 PSTOP	Description	
0	System clock output is enabled	(Initial value)
1	System clock output is disabled	

Bits 6 to 3—Reserved: These bits cannot be modified and are always read as 1.

Bit 2—Reserved: This bit can be written and read.

Bit 1—Module Standby H1 (MSTPH1): Selects whether to place the SCI1 in standby.

Bit 1 MSTPH1	Description	
0	SCI1 operates normally	(Initial value)
1	SCI1 is in standby state	

Table 21.4 Clock Timing

Conditions: V_{CC} = 3.0 to 3.6 V, AV_{CC} = 3.0 to 3.6 V, V_{REF} = 3.0 to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min	Max	Unit	Test Conditions
Clock cycle time	t_{cyc}	40	500	ns	Figure 21.11
Clock pulse low width	t_{CL}	10	—	ns	
Clock pulse high width	t_{CH}	10	—	ns	
Clock rise time	t_{Cr}	—	10	ns	
Clock fall time	t_{Cf}	—	10	ns	
Clock oscillator settling time at reset	t_{OSC1}	20	—	ms	Figure 21.7
Clock oscillator settling time in software standby	t_{OSC2}	7	—	ms	Figure 20.1

Table 21.5 Control Signal Timing

Conditions: V_{CC} = 3.0 to 3.6 V, AV_{CC} = 3.0 to 3.6 V, V_{REF} = 3.0 to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min	Max	Unit	Test Conditions
$\overline{RES}$ setup time	t_{RESS}	150	—	ns	Figure 21.8
$\overline{RES}$ pulse width	t_{RESW}	20	—	t_{cyc}	
Mode programming setup time	t_{MDS}	200	—	ns	
$\overline{RESO}$ output delay time	t_{RESD}	—	50	ns	Figure 21.9
$\overline{RESO}$ output pulse width	t_{RESOW}	132	—	t_{cyc}	
NMI, $\overline{IRQ}$ setup time	t_{NMIS}	150	—	ns	Figure 21.10
NMI, $\overline{IRQ}$ hold time	t_{NMIH}	10	—	ns	
NMI, $\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{NMIW}	200	—	ns	

2. Given current consumption values are when all the output pins are made to unloaded state and, furthermore, when the on-chip pull-up MOS is turned off under conditions that V_{IH} min = V_{CC} – 0.5 V and V_{IL} max = 0.5 V.
   Also, the aforesaid current consumption values are when V_{IH} min = $V_{CC} \times 0.9$ and V_{IL} max = 0.3 V under the condition of $V_{RAM} \leq V_{CC} < 3.0$ V.
3. I_{CC} max. (under normal operations) = 3.0 (mA) + 0.61 (mA/(MHz × V)) × V_{CC} × f
   I_{CC} max. (when using the sleeve) = 3.0 (mA) + 0.49 (mA/(MHz × V)) × V_{CC} x f
   I_{CC} max. (when the sleeve + module are standing by)
   = 3.0 (mA) + 0.38 (mA/(MHz × V)) × V_{CC} × f
   Also, the typ. values for current dissipation are reference values.

Table 21.12 Permissible Output Currents

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{REF} = 3.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, 2, and 5	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 20 pins in Ports 1, 2, and 5	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$\lvert -I_{OH} \rvert$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\lvert -\Sigma I_{OH} \rvert$	—	—	40	mA

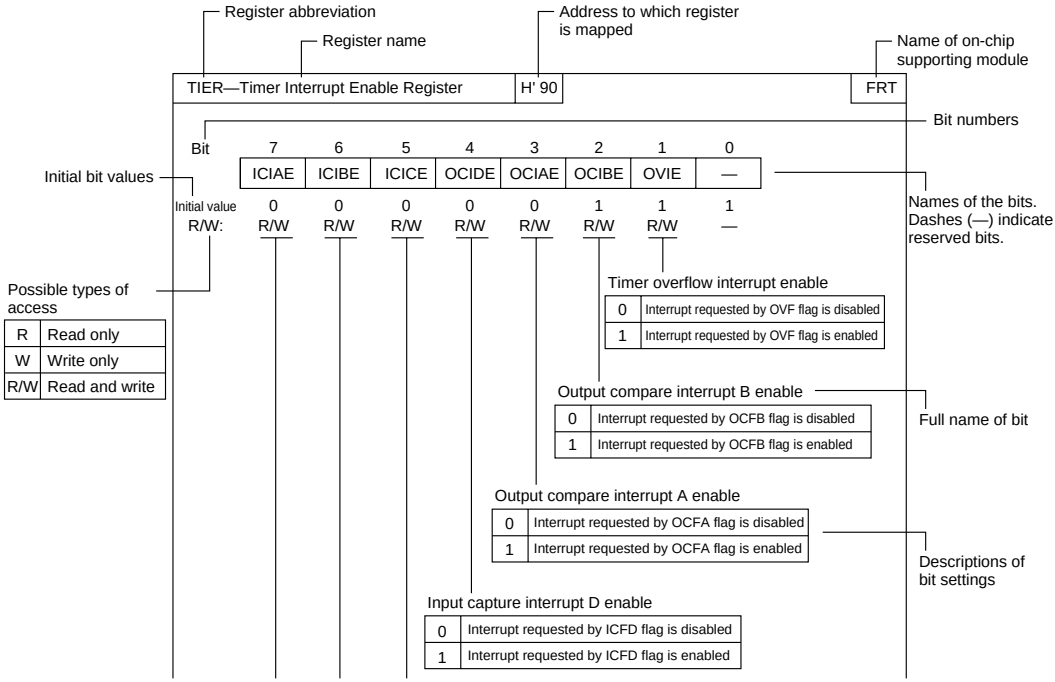
Notes: 1. To protect chip reliability, do not exceed the output current values in table 21.12.
2. When directly driving a darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 21.4 and 21.5.

Mnemonic	Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
		#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	|		I	H	N	Z	V	C	Normal	Advanced
INC.L #1, ERd	L		2								ERd32+1 → ERd32	—	—	↕	↕	↕	—	2	
INC.L #2, ERd	L		2								ERd32+2 → ERd32	—	—	↕	↕	↕	—	2	
DAA Rd	B		2								Rd8 decimal adjust → Rd8	—	*	↕	↕	*	—	2	
SUB.B Rs, Rd	B		2								Rd8–Rs8 → Rd8	—	↕	↕	↕	↕	↕	2	
SUB.W #xx:16, Rd	W	4									Rd16–#xx:16 → Rd16	—	(1)	↕	↕	↕	↕	4	
SUB.W Rs, Rd	W		2								Rd16–Rs16 → Rd16	—	(1)	↕	↕	↕	↕	2	
SUB.L #xx:32, ERd	L	6									ERd32–#xx:32 → ERd32	—	(2)	↕	↕	↕	↕	6	
SUB.L ERs, ERd	L		2								ERd32–ERs32 → ERd32	—	(2)	↕	↕	↕	↕	2	
SUBX.B #xx:8, Rd	B	2									Rd8–#xx:8–C → Rd8	—	↕	↕	(3)	↕	↕	2	
SUBX.B Rs, Rd	B		2								Rd8–Rs8–C → Rd8	—	↕	↕	(3)	↕	↕	2	
SUBS.L #1, ERd	L		2								ERd32–1 → ERd32	—	—	—	—	—	—	2	
SUBS.L #2, ERd	L		2								ERd32–2 → ERd32	—	—	—	—	—	—	2	
SUBS.L #4, ERd	L		2								ERd32–4 → ERd32	—	—	—	—	—	—	2	
DEC.B Rd	B		2								Rd8–1 → Rd8	—	—	↕	↕	↕	—	2	
DEC.W #1, Rd	W		2								Rd16–1 → Rd16	—	—	↕	↕	↕	—	2	
DEC.W #2, Rd	W		2								Rd16–2 → Rd16	—	—	↕	↕	↕	—	2	
DEC.L #1, ERd	L		2								ERd32–1 → ERd32	—	—	↕	↕	↕	—	2	
DEC.L #2, ERd	L		2								ERd32–2 → ERd32	—	—	↕	↕	↕	—	2	
DAS.Rd	B		2								Rd8 decimal adjust → Rd8	—	*	↕	↕	*	—	2	
MULXU. B Rs, Rd	B		2								Rd8 × Rs8 → Rd16 (unsigned multiplication)	—	—	—	—	—	—	14	
MULXU. W Rs, ERd	W		2								Rd16 × Rs16 → ERd32 (unsigned multiplication)	—	—	—	—	—	—	22	
MULXS. B Rs, Rd	B		4								Rd8 × Rs8 → Rd16 (signed multiplication)	—	—	↕	↕	—	—	16	
MULXS. W Rs, ERd	W		4								Rd16 × Rs16 → ERd32 (signed multiplication)	—	—	↕	↕	—	—	24	
DIVXU. B Rs, Rd	B		2								Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (unsigned division)	—	—	(6)	(7)	—	—	14	

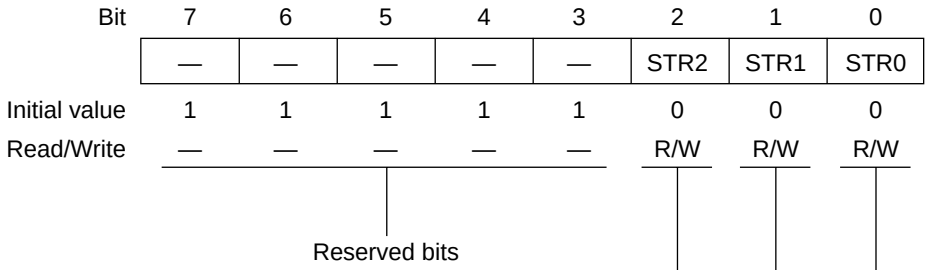
6. Branching instructions

Mnemonic	Operand Size	Addressing Mode and Instruction Length (bytes)								Operation	Branch Condition	Condition Code						No. of States*1	
		#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa			I	H	N	Z	V	C	Normal	Advanced
BRA d:8 (BT d:8)	—							2		If condition is true then PC ← PC+d else next;	Always	—	—	—	—	—	—	4	
BRA d:16 (BT d:16)	—							4				—	—	—	—	—	—	6	
BRN d:8 (BF d:8)	—							2			Never	—	—	—	—	—	—	4	
BRN d:16 (BF d:16)	—							4				—	—	—	—	—	—	6	
BHI d:8	—							2			C ∨ Z = 0	—	—	—	—	—	—	4	
BHI d:16	—							4				—	—	—	—	—	—	6	
BLS d:8	—							2			C ∨ Z = 1	—	—	—	—	—	—	4	
BLS d:16	—							4				—	—	—	—	—	—	6	
BCC d:8 (BHS d:8)	—							2			C = 0	—	—	—	—	—	—	4	
BCC d:16 (BHS d:16)	—							4				—	—	—	—	—	—	6	
BCS d:8 (BLO d:8)	—							2			C = 1	—	—	—	—	—	—	4	
BCS d:16 (BLO d:16)	—							4				—	—	—	—	—	—	6	
BNE d:8	—							2			Z = 0	—	—	—	—	—	—	4	
BNE d:16	—							4				—	—	—	—	—	—	6	
BEQ d:8	—							2			Z = 1	—	—	—	—	—	—	4	
BEQ d:16	—							4				—	—	—	—	—	—	6	
BVC d:8	—							2			V = 0	—	—	—	—	—	—	4	
BVC d:16	—							4				—	—	—	—	—	—	6	
BVS d:8	—							2			V = 1	—	—	—	—	—	—	4	
BVS d:16	—							4				—	—	—	—	—	—	6	
BPL d:8	—							2			N = 0	—	—	—	—	—	—	4	
BPL d:16	—							4				—	—	—	—	—	—	6	
BMI d:8	—							2			N = 1	—	—	—	—	—	—	4	
BMI d:16	—							4				—	—	—	—	—	—	6	
BGE d:8	—							2			N⊕V = 0	—	—	—	—	—	—	4	
BGE d:16	—							4				—	—	—	—	—	—	6	
BLT d:8	—							2			N⊕V = 1	—	—	—	—	—	—	4	
BLT d:16	—							4				—	—	—	—	—	—	6	
BGT d:8	—							2			Z ∨ (N⊕V) = 0	—	—	—	—	—	—	4	
BGT d:16	—							4				—	—	—	—	—	—	6	

B.3 Functions



TSTR—Timer Start Register **H'FFF60** **16-bit timer (all channels)**



Counter start 0

0	16TCNT0 is halted	(Initial value)
1	16TCNT0 is counting	

Counter start 1

0	16TCNT1 is halted	(Initial value)
1	16TCNT1 is counting	

Counter start 2

0	16TCNT2 is halted	(Initial value)
1	16TCNT2 is counting	

D.2 Pin States at Reset

Modes 1 and 2: Figure D.1 is a timing diagram for the case in which $\overline{RES}$ goes low during an external memory access in mode 1 or 2. As soon as $\overline{RES}$ goes low, all ports are initialized to the input state. $\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, $\overline{LWR}$, and $\overline{CS}_0$ go high, and D_{15} to D_0 go to the high-impedance state. The address bus is initialized to the low output level 2.5 ϕ clock cycles after the low level of $\overline{RES}$ is sampled. Clock pin $P6_7/\phi$ goes to the output state at the next rise of ϕ after $\overline{RES}$ goes low.

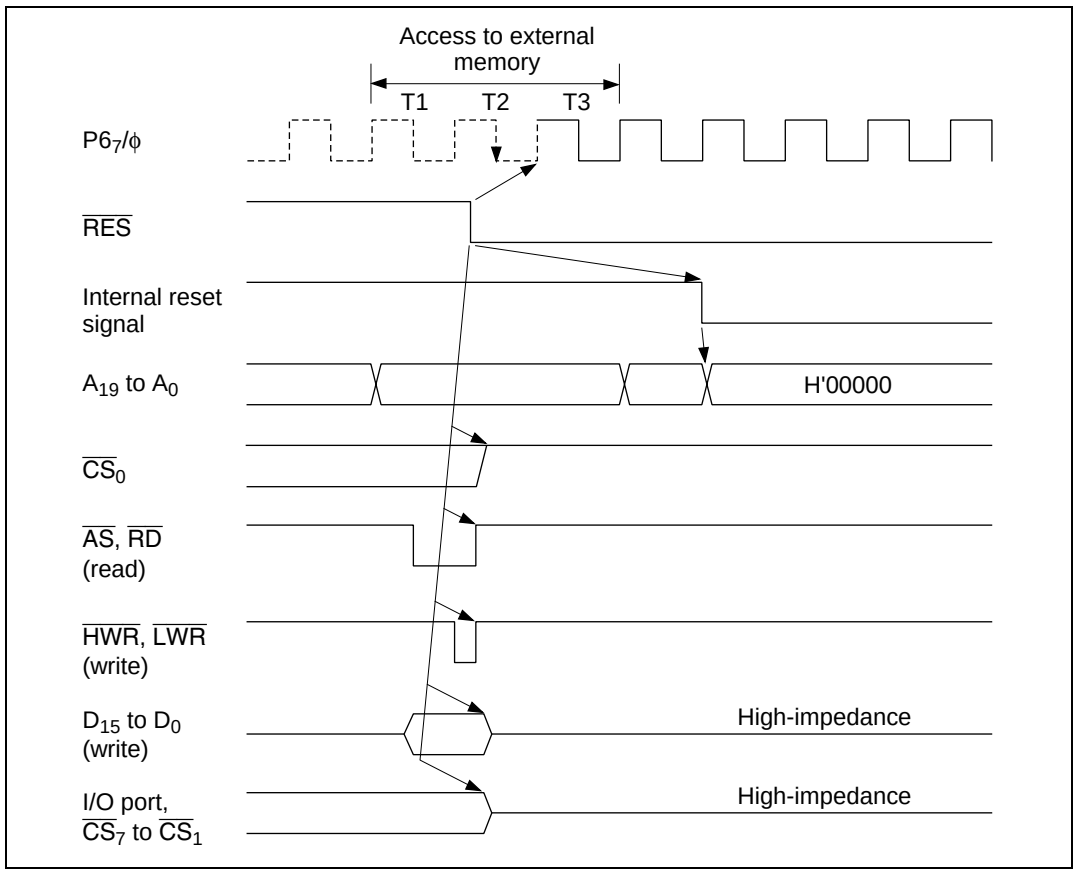


Figure D.1 Reset during Memory Access (Modes 1 and 2)