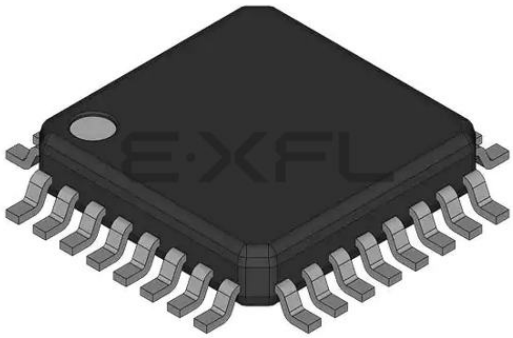

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Applications of "Embedded - Microcontrollers"

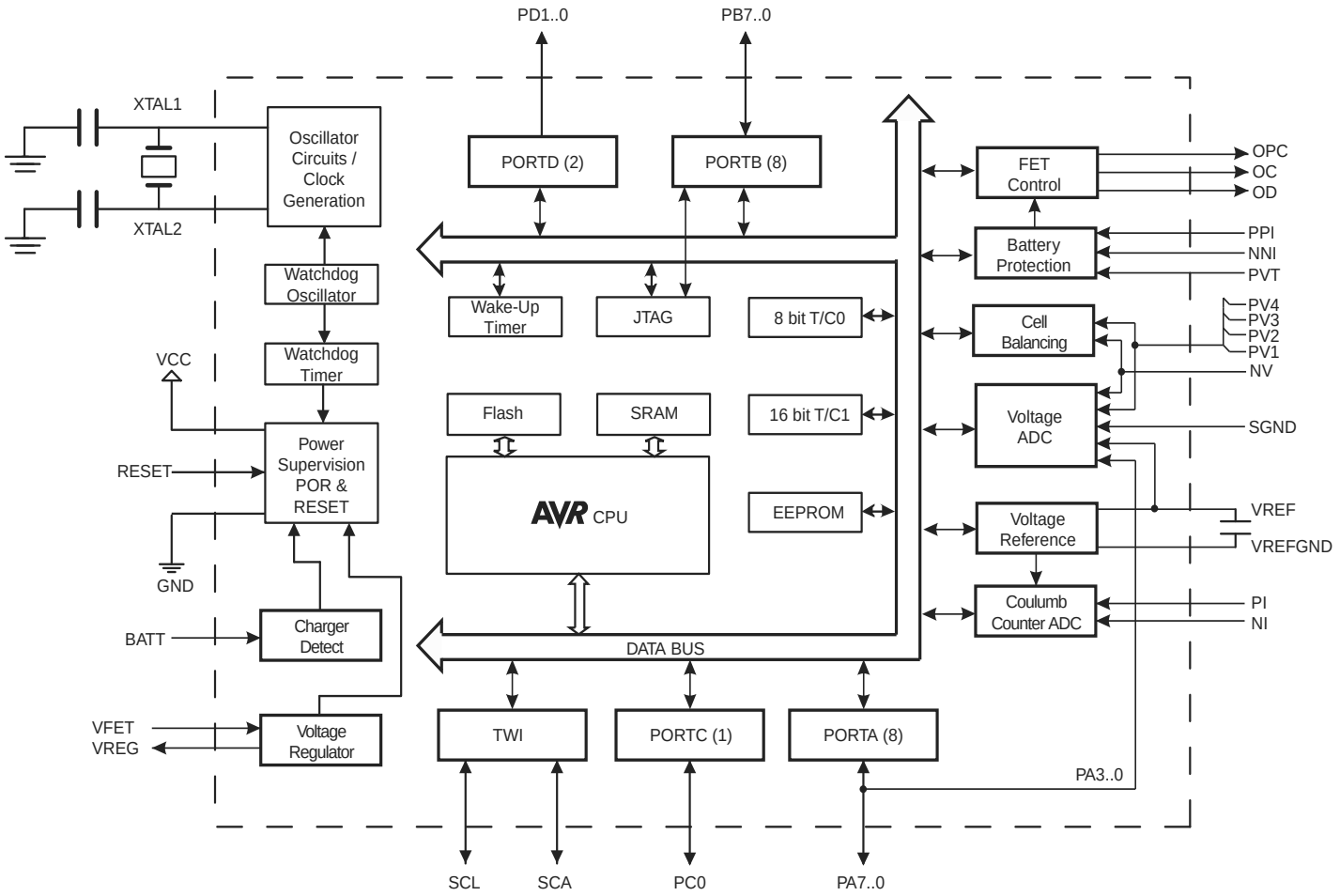
Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	1MHz
Connectivity	I²C
Peripherals	POR, WDT
Number of I/O	18
Program Memory Size	40KB (20K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 25V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atmega406-1aau

2. Overview

The ATmega406 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega406 achieves throughputs approaching 1 MIPS at 1 MHz.

2.1 Block Diagram

Figure 2-1. Block Diagram



The ATmega406 provides the following features: a Voltage Regulator, dedicated Battery Protection Circuitry, integrated cell balancing FETs, high-voltage analog front-end, and an MCU with two ADCs with On-chip voltage reference for battery fuel gauging.

The voltage regulator operates at a wide range of voltages, 4.0 - 25 volts. This voltage is regulated to a constant supply voltage of nominally 3.3 volts for the integrated logic and analog functions.

The battery protection monitors the battery voltage and charge/discharge current to detect illegal conditions and protect the battery from these when required. The illegal conditions are deep under-voltage during discharging, short-circuit during discharging and over-current during charging and discharging.

2.2 Pin Descriptions

2.2.1 VFET

High voltage supply pin. This pin is used as supply for the internal voltage regulator, described in ”Voltage Regulator” on page 114. In addition the voltage level on this pin is monitored by the battery protection circuit, for deep-under-voltage protection. For details, see ”Battery Protection” on page 125.

2.2.2 VCC

Digital supply voltage. Normally connected to VREG.

2.2.3 VREG

Output from the internal Voltage Regulator. Used for external decoupling to ensure stable regulator operation. For details, see ”Voltage Regulator” on page 114.

2.2.4 VREF

Internal Voltage Reference for external decoupling. For details, see ”Voltage Reference and Temperature Sensor” on page 121.

2.2.5 VREFGND

Ground for decoupling of Internal Voltage Reference. For details, see ”Voltage Reference and Temperature Sensor” on page 121.

2.2.6 GND

Ground

2.2.7 SGND

Signal ground pin, used as reference for Voltage-ADC conversions. For details, see ”Voltage ADC – 10-channel General Purpose 12-bit Sigma-Delta ADC” on page 116.

2.2.8 Port A (PA7:PA0)

PA3:PA0 serves as the analog inputs to the Voltage A/D Converter.

Port A also serves as a low-voltage 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega406 as listed in ”Alternate Functions of Port A” on page 68.

2.2.9 Port B (PB7:PB0)

Port B is a low-voltage 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega406 as listed in ”Alternate Functions of Port B” on page 70.

2.2.10 Port C (PC0)

Port C is a high voltage Open Drain output port.

2.2.11 Port D (PD1:PD0)

Port D is a low-voltage 2-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega406 as listed in ”Alternate Functions of Port D” on page 72.

2.2.12 SCL

SMBUS clock, Open Drain bidirectional pin.

2.2.13 SDA

SMBUS data, Open Drain bidirectional pin.

2.2.14 OC/OD/OPC

High voltage output to drive external Charge/Discharge/Pre-charge FETs. For details, see ”FET Control” on page 133.

2.2.15 PPI/NNI

Unfiltered positive/negative input from external current sense resistor, used by the battery protection circuit, for over-current and short-circuit detection. For details, see ”Battery Protection” on page 125.

2.2.16 PI/NI

Filtered positive/negative input from external current sense resistor, used to by the Coulomb Counter ADC to measure charge/discharge currents flowing in the battery pack. For details, see ”Coulomb Counter - Dedicated Fuel Gauging Sigma-delta ADC” on page 106.

2.2.17 NV/PV1/PV2/PV3/PV4

NV, PV1, PV2, PV3, and PV4 are the inputs for battery cells 1, 2, 3 and 4, used by the Voltage ADC to measure each cell voltage. For details, see ”Voltage ADC – 10-channel General Purpose 12-bit Sigma-Delta ADC” on page 116.

2.2.18 PVT

PVT defines the pull-up level for the OD output.

2.2.19 BATT

Input for detecting when a charger is connected. This pin also defines the pull-up level for OC and OPC outputs.

2.2.20 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 11 on page 38. Shorter pulses are not guaranteed to generate a reset.

4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	–	–	–	–	–	–	–	–	
(0xFE)	Reserved	–	–	–	–	–	–	–	–	
(0xFD)	Reserved	–	–	–	–	–	–	–	–	
(0xFC)	Reserved	–	–	–	–	–	–	–	–	
(0xFB)	Reserved	–	–	–	–	–	–	–	–	
(0xFA)	Reserved	–	–	–	–	–	–	–	–	
(0xF9)	Reserved	–	–	–	–	–	–	–	–	
(0xF8)	BPPLR	–	–	–	–	–	–	BPPLE	BPPL	128
(0xF7)	BPCR	–	–	–	–	DUVD	SCD	DCD	CCD	128
(0xF6)	CBPTR	SCPT[3:0]				OCPT[3:0]				129
(0xF5)	BPOCD	DCDL[3:0]				CCDL[3:0]				130
(0xF4)	BPSCD	–	–	–	–	SCDL[3:0]				130
(0xF3)	BPDUV	–	–	DUVT1	DUVT0	DUDL[3:0]				131
(0xF2)	BPIR	DUVIF	COCIF	DOCIF	SCIF	DUVIE	COCIE	DOCIE	SCIE	132
(0xF1)	CBCR	–	–	–	–	CBE4	CBE3	CBE2	CBE1	137
(0xF0)	FCSR	–	–	PWMOC	PWMOPC	CPS	DFE	CFE	PFD	134
(0xEF)	Reserved	–	–	–	–	–	–	–	–	
(0xEE)	Reserved	–	–	–	–	–	–	–	–	
(0xED)	Reserved	–	–	–	–	–	–	–	–	
(0xEC)	Reserved	–	–	–	–	–	–	–	–	
(0xEB)	Reserved	–	–	–	–	–	–	–	–	
(0xEA)	Reserved	–	–	–	–	–	–	–	–	
(0xE9)	CADICH	CADIC[15:8]								111
(0xE8)	CADICL	CADIC[7:0]								111
(0xE7)	CADRDC	CADRDC[7:0]								112
(0xE6)	CADRCC	CADRCC[7:0]								112
(0xE5)	CADCSRB	–	CADACIE	CADRCIE	CADICIE	–	CADACIF	CADRCIF	CADICIF	110
(0xE4)	CADCSRA	CADEN	–	CADUB	CADAS1	CADAS0	CADSI1	CADSI0	CADSE	109
(0xE3)	CADAC3	CADAC[31:24]								111
(0xE2)	CADAC2	CADAC[23:16]								111
(0xE1)	CADAC1	CADAC[15:8]								111
(0xE0)	CADAC0	CADAC[7:0]								111
(0xDF)	Reserved	–	–	–	–	–	–	–	–	
(0xDE)	Reserved	–	–	–	–	–	–	–	–	
(0xDD)	Reserved	–	–	–	–	–	–	–	–	
(0xDC)	Reserved	–	–	–	–	–	–	–	–	
(0xDB)	Reserved	–	–	–	–	–	–	–	–	
(0xDA)	Reserved	–	–	–	–	–	–	–	–	
(0xD9)	Reserved	–	–	–	–	–	–	–	–	
(0xD8)	Reserved	–	–	–	–	–	–	–	–	
(0xD7)	Reserved	–	–	–	–	–	–	–	–	
(0xD6)	Reserved	–	–	–	–	–	–	–	–	
(0xD5)	Reserved	–	–	–	–	–	–	–	–	
(0xD4)	Reserved	–	–	–	–	–	–	–	–	
(0xD3)	Reserved	–	–	–	–	–	–	–	–	
(0xD2)	Reserved	–	–	–	–	–	–	–	–	
(0xD1)	BGCRR	BGCR7	BGCR6	BGCR5	BGCR4	BGCR3	BGCR2	BGCR1	BGCR0	123
(0xD0)	BGCCR	BGEN	–	BGCC5	BGCC4	BGCC3	BGCC2	BGCC1	BGCC0	123
(0xCF)	Reserved	–	–	–	–	–	–	–	–	
(0xCE)	Reserved	–	–	–	–	–	–	–	–	
(0xCD)	Reserved	–	–	–	–	–	–	–	–	
(0xCC)	Reserved	–	–	–	–	–	–	–	–	
(0xCB)	Reserved	–	–	–	–	–	–	–	–	
(0xCA)	Reserved	–	–	–	–	–	–	–	–	
(0xC9)	Reserved	–	–	–	–	–	–	–	–	
(0xC8)	Reserved	–	–	–	–	–	–	–	–	
(0xC7)	Reserved	–	–	–	–	–	–	–	–	
(0xC6)	Reserved	–	–	–	–	–	–	–	–	
(0xC5)	Reserved	–	–	–	–	–	–	–	–	
(0xC4)	Reserved	–	–	–	–	–	–	–	–	
(0xC3)	Reserved	–	–	–	–	–	–	–	–	
(0xC2)	Reserved	–	–	–	–	–	–	–	–	
(0xC1)	Reserved	–	–	–	–	–	–	–	–	
(0xC0)	CCSR	–	–	–	–	–	–	XOE	ACS	29

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBF)	Reserved	–	–	–	–	–	–	–	–	
(0xBE)	TWBCSR	TWBCIF	TWBCIE	–	–	–	TWBDT1	TWBDT0	TWBCIP	169
(0xBD)	TWAMR	TWAM[6:0]							–	150
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	147
(0xBB)	TWDR	2–wire Serial Interface Data Register								149
(0xBA)	TWAR	TWA[6:0]							TWGCE	149
(0xB9)	TWSR	TWS[7:3]					–	TWPS1	TWPS0	148
(0xB8)	TWBR	2–wire Serial Interface Bit Rate Register								147
(0xB7)	Reserved	–		–	–	–	–	–	–	
(0xB6)	Reserved	–	–	–	–	–	–	–	–	
(0xB5)	Reserved	–	–	–	–	–	–	–	–	
(0xB4)	Reserved	–	–	–	–	–	–	–	–	
(0xB3)	Reserved	–	–	–	–	–	–	–	–	
(0xB2)	Reserved	–	–	–	–	–	–	–	–	
(0xB1)	Reserved	–	–	–	–	–	–	–	–	
(0xB0)	Reserved	–	–	–	–	–	–	–	–	
(0xAF)	Reserved	–	–	–	–	–	–	–	–	
(0xAE)	Reserved	–	–	–	–	–	–	–	–	
(0xAD)	Reserved	–	–	–	–	–	–	–	–	
(0xAC)	Reserved	–	–	–	–	–	–	–	–	
(0xAB)	Reserved	–	–	–	–	–	–	–	–	
(0xAA)	Reserved	–	–	–	–	–	–	–	–	
(0xA9)	Reserved	–	–	–	–	–	–	–	–	
(0xA8)	Reserved	–	–	–	–	–	–	–	–	
(0xA7)	Reserved	–	–	–	–	–	–	–	–	
(0xA6)	Reserved	–	–	–	–	–	–	–	–	
(0xA5)	Reserved	–	–	–	–	–	–	–	–	
(0xA4)	Reserved	–	–	–	–	–	–	–	–	
(0xA3)	Reserved	–	–	–	–	–	–	–	–	
(0xA2)	Reserved	–	–	–	–	–	–	–	–	
(0xA1)	Reserved	–	–	–	–	–	–	–	–	
(0xA0)	Reserved	–	–	–	–	–	–	–	–	
(0x9F)	Reserved	–	–	–	–	–	–	–	–	
(0x9E)	Reserved	–	–	–	–	–	–	–	–	
(0x9D)	Reserved	–	–	–	–	–	–	–	–	
(0x9C)	Reserved	–	–	–	–	–	–	–	–	
(0x9B)	Reserved	–	–	–	–	–	–	–	–	
(0x9A)	Reserved	–	–	–	–	–	–	–	–	
(0x99)	Reserved	–	–	–	–	–	–	–	–	
(0x98)	Reserved	–	–	–	–	–	–	–	–	
(0x97)	Reserved	–	–	–	–	–	–	–	–	
(0x96)	Reserved	–	–	–	–	–	–	–	–	
(0x95)	Reserved	–	–	–	–	–	–	–	–	
(0x94)	Reserved	–	–	–	–	–	–	–	–	
(0x93)	Reserved	–	–	–	–	–	–	–	–	
(0x92)	Reserved	–	–	–	–	–	–	–	–	
(0x91)	Reserved	–	–	–	–	–	–	–	–	
(0x90)	Reserved	–	–	–	–	–	–	–	–	
(0x8F)	Reserved	–	–	–	–	–	–	–	–	
(0x8E)	Reserved	–	–	–	–	–	–	–	–	
(0x8D)	Reserved	–	–	–	–	–	–	–	–	
(0x8C)	Reserved	–	–	–	–	–	–	–	–	
(0x8B)	Reserved	–	–	–	–	–	–	–	–	
(0x8A)	Reserved	–	–	–	–	–	–	–	–	
(0x89)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte								101
(0x88)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte								101
(0x87)	Reserved	–	–	–	–	–	–	–	–	
(0x86)	Reserved	–	–	–	–	–	–	–	–	
(0x85)	TCNT1H	Timer/Counter1 – Counter Register High Byte								101
(0x84)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								101
(0x83)	Reserved	–	–	–	–	–	–	–	–	
(0x82)	Reserved	–	–	–	–	–	–	–	–	
(0x81)	TCCR1B	–	–	–	–	CTC1	CS12	CS11	CS10	100
(0x80)	Reserved	–	–	–	–	–	–	–	–	
(0x7F)	Reserved	–	–	–	–	–	–	–	–	
(0x7E)	DIDR0	–	–	–	–	VADC3D	VADC2D	VADC1D	VADC0D	120

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF − Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 − Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd − 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
JMP	k	Direct Jump	PC ← k	None	3
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
CALL	k	Direct Subroutine Call	PC ← k	None	4
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd − Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd − Rr − C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd − K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2

5. Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1

5. Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

6. Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package[1]	Operation Range
1	4.0 - 25V	ATmega406-1AAU[2]	48AA	Industrial (-30·C to 85·C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

Package Type	
48AA	48-lead, 7 x 7 x 1.44 mm body, 0.5 mm lead pitch, Low Profile Plastic Quad Flat Package (LQFP)

8. Errata

8.1 Rev. F

- **Voltage-ADC Common Mode Offset**
- **Voltage Reference Spike**

1. Voltage-ADC Common Mode Offset

The cell conversion will have an Offset-error depending on the Common Mode (CM) level. This means that the error of a cell is depending on the voltage of the lower cells. The CM Offset is calibrated away in Atmel production when the cells are balanced. When the cells get un-balanced the CM depending offset will reappear:

a. Cell 1 defines its own CM level, and will never be affected by the CM dependent offset.

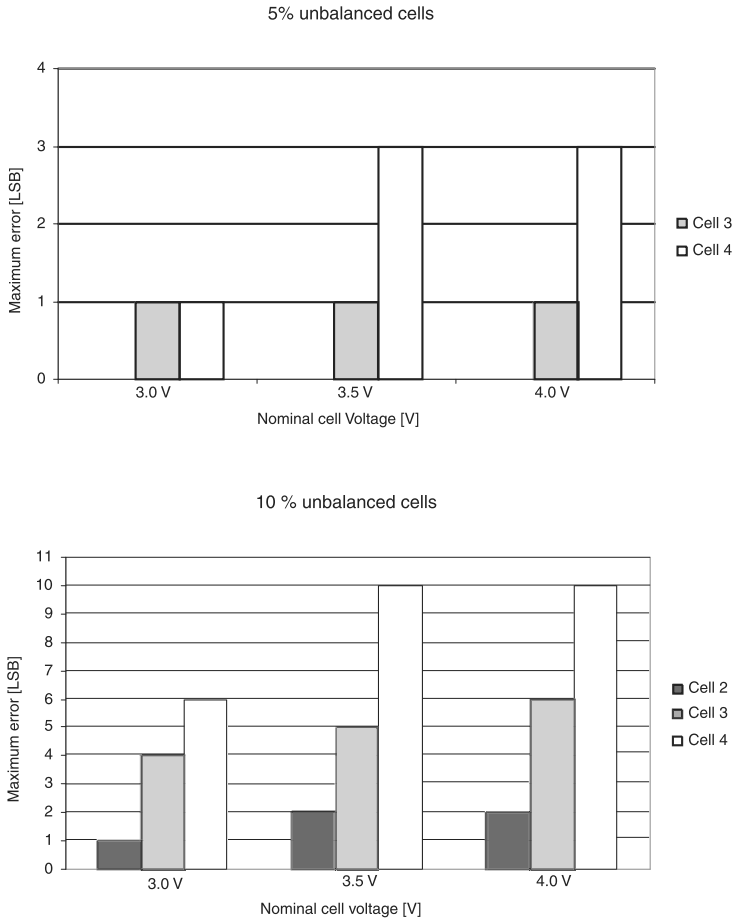
b. The CM level for Cell 2 will change if Cell 1 voltage deviates from Cell 2 voltage.

c. The CM level for Cell 3 will change if Cell 1 and/or Cell 2 voltage deviates from the voltage at Cell 3. The worst-case error is when Cell 1 and 2 are balanced while Cell 3 voltage deviates from the voltage at Cell 1 and 2.

d. The CM level for Cell 4 will change if Cell 1, Cell 2 and/or Cell 3 deviate from the voltage at Cell 4. The worst-case error is when Cell 1, Cell 2 and Cell 3 are balanced while Cell 4 voltage deviates from the voltage at Cell 1, 2 and 3.

Figure 8-1 on page 20, shows the error of Cell2, Cell3 and Cell4 with 5% and 10% unbalanced cells.

Figure 8-1. CM Offset with unbalanced cells.



Problem Fix/Workaround

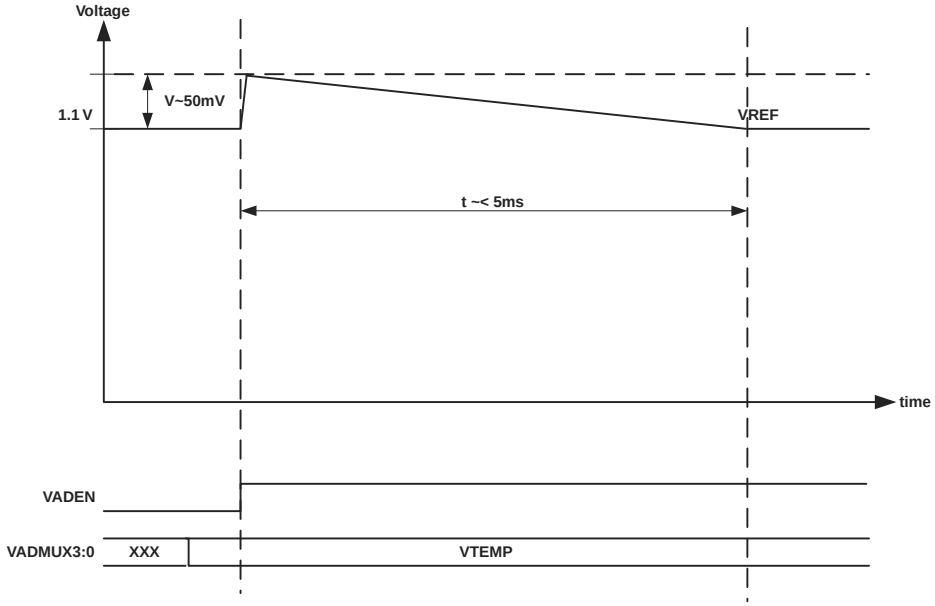
Avoid getting unbalanced cells by using the internal cell balancing FETs.

2. Voltage Reference spike

The Voltage Reference, VREF, will spike each time the internal temperature sensor is enabled. The temperature sensor is enabled when the VTEMP is selected in the VADMUX register and the V-ADC is enabled by the VADEN bit.

The spike will be approximately 50mV and lasts for about 5ms, and it will affect any ongoing current accumulation in the CC-ADC, as well as V-ADC conversions in the period of the spike. Figure 8-2 on page 21 illustrates the Voltage Reference spike.

Figure 8-2. Voltage Reference Spike



Problem workaround:

To get correct temperature measurement, the VADSC bit should not be written until the spike has settled (external decoupling capacitor of 1µF).

8.2 Rev. E

- **Voltage ADC not functional below 0**°C
- **Voltage-ADC Common Mode Offset**
- **Voltage Reference Spike**

1. Voltage-ADC Failing at Low Temperatures

Voltage ADC not functional below 0°C. The voltage ADC has a very large error below 0°C, and can not be used

Problem Fix/Workaround

Do not use this revision below 0 celsius.

2. Voltage-ADC Common Mode Offset

The cell conversion will have an Offset-error depending on the Common Mode (CM) level. This means that the error of a cell is depending on the voltage of the lower cells. The CM Offset is calibrated away in Atmel production when the cells are balanced. When the cells get un-balanced the CM depending offset will reappear:

a. Cell 1 defines its own CM level, and will never be affected by the CM dependent offset.

b. The CM level for Cell 2 will change if Cell 1 voltage deviates from Cell 2 voltage.

c. The CM level for Cell 3 will change if Cell 1 and/or Cell 2 voltage deviates from the voltage at Cell 3. The worst-case error is when Cell 1 and 2 are balanced while Cell 3 voltage deviates from the voltage at Cell 1 and 2.

d. The CM level for Cell 4 will change if Cell 1, Cell 2 and/or Cell 3 deviate from the voltage at Cell 4. The worst-case error is when Cell 1, Cell 2 and Cell 3 are balanced while Cell 4 voltage deviates from the voltage at Cell 1, 2 and 3.

Figure 8-1 on page 20, shows the error of Cell2, Cell3 and Cell4 with 5% and 10% unbalanced cells.

a. Cell 1 defines its own CM level, and will never be affected by the CM dependent offset.

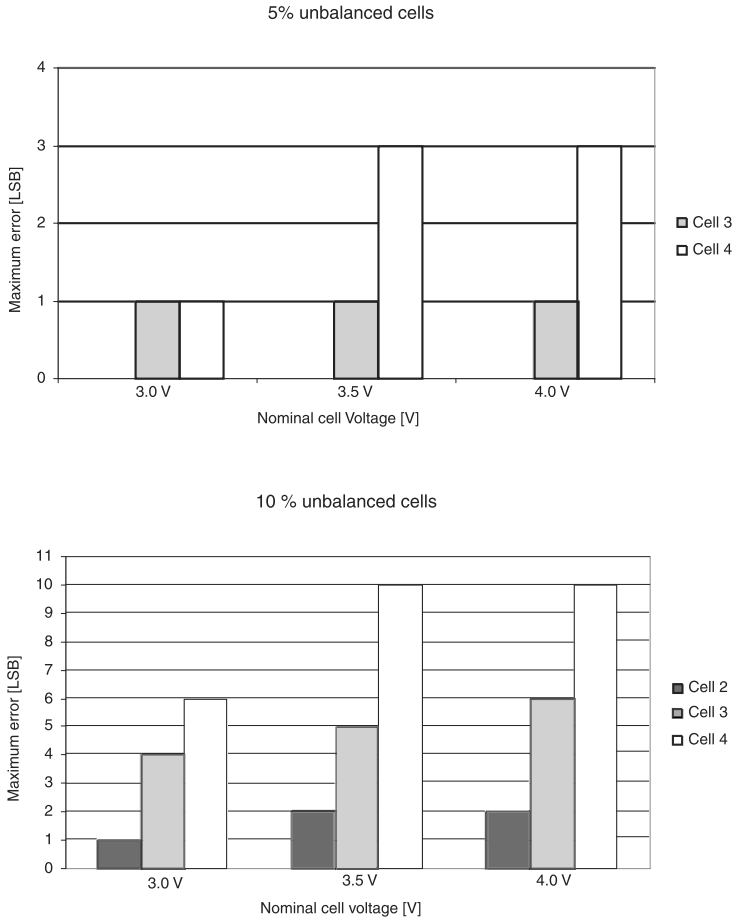
b. The CM level for Cell 2 will change if Cell 1 voltage deviates from Cell 2 voltage.

c. The CM level for Cell 3 will change if Cell 1 and/or Cell 2 voltage deviates from the voltage at Cell 3. The worst-case error is when Cell 1 and 2 are balanced while Cell 3 voltage deviates from the voltage at Cell 1 and 2.

d. The CM level for Cell 4 will change if Cell 1, Cell 2 and/or Cell 3 deviate from the voltage at Cell 4. The worst-case error is when Cell 1, Cell 2 and Cell 3 are balanced while Cell 4 voltage deviates from the voltage at Cell 1, 2 and 3.

Figure 8-1 on page 20, shows the error of Cell2, Cell3 and Cell4 with 5% and 10% unbalanced cells.

Figure 8-5. CM Offset with unbalanced cells.



Problem Fix/Workaround

Avoid getting unbalanced cells by using the internal cell balancing FETs.

3. Voltage Reference Spike

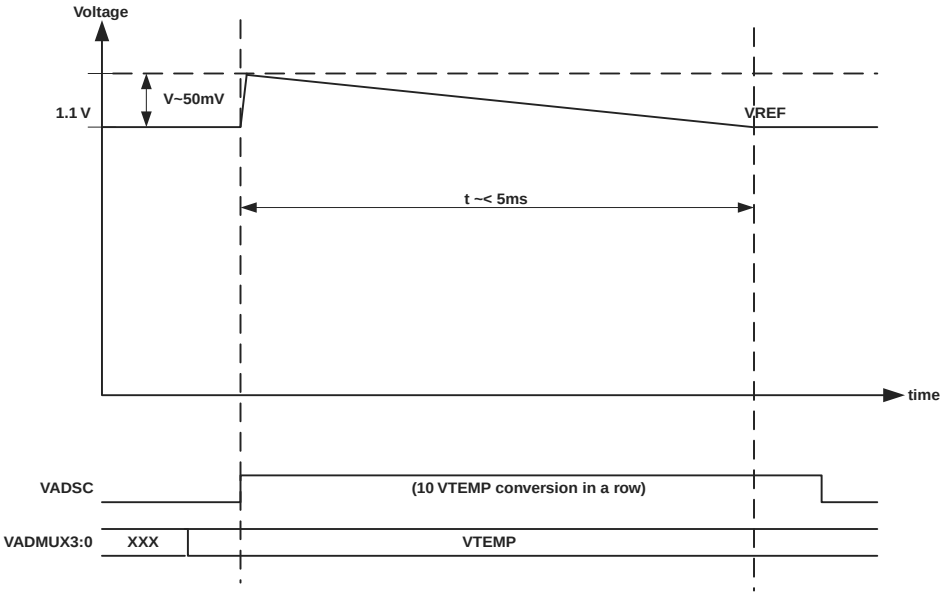
The Voltage Reference, VREF, will spike each time a temperature measurement is started with the Voltage-ADC.

Problem Fix/Workaround

An accurate temperature measurement could be obtained by doing 10 temperature conversions immediately after each other. The first 9 results would be inaccurate, but the 10th conversion will be correct.

Figure 8-6 illustrates the spike on the Voltage Reference when doing 10 temperature conversions in a row (external decoupling capacitor of 1µF).

Figure 8-6. Voltage Reference Spike



If the CC-ADC is doing current accumulation while the V-ADC is doing temperature measurement, both the Instantaneous and the Accumulated conversion results will be affected. The spike on VREF will be visible on 1 Accumulated Current (CADAC3…0) and 2 Instantaneous Current (CADIC1…0) conversion results.

4. Voltage Regulator Start-up sequence

When powering up ATmega406 some precautions are necessary to ensure proper start-up of the Voltage Regulator.

Problem Fix/Workaround

The three steps below are needed to ensure proper start-up of the voltage regulator.

a. Do NOT connect a capacitor larger than 100 nF on the VFET pin. This is to ensure fast rise time on the VFET pin when a supply voltage is connected.

b. During assembly, always connect Cell1 first, then Cell2 and so on until the top cell is connected to PVT. If the cell voltages are about 2 volts or larger, the Voltage Regulator will normally start up properly in Power-off mode (VREG appr. 2.8 volts).

c. After all cells have been assembled as described in step 2, a charger source must be connected at the BATT+ terminal to initialize the chip, see Section 8.3 ”Power-on Reset and Charger Connect” on page 38 in the datasheet.

If the Voltage Regulator started up in Power-off during assembly of the cells, the chip will initialize when the charger source makes the voltage at the BATT pin exceed 7 - 8 Volts.

If the Voltage Regulator did not start up properly, the charger source has one additional requirement to ensure proper start up and initialization. In this case the charger source must ensure that the voltage at the VFET pin increases quickly at least 3 Volts above the voltage at the PVT pin, and that the voltage at the BATT pin exceeds 7 - 8 Volts. This will start up and initialize the chip directly.

5. V_{REF} influenced by MCU state

The reference voltage at the V_{REF} pin depends on the following conditions of the device:

a. Charger Over-current and/or Discharge Over-current Protection active but Short-circuit inactive. This will increase V_{REF} voltage with typical 1 mV compared to a condition were all Current Protections are disabled.

b. Short-circuit Protection active. Short-circuit measurements are activated when SCD in BPCR is zero (default) and DFE in FET Control and Status Register (FCSR) is set. This will increase V_{REF} voltage with typical 8 mV compared to a condition with short-circuit measurements inactive.

c. V-ADC conversion of the internal VTEMP voltage. This will increase V_{REF} voltage with typical 15 mV compared to a condition with short-circuit measurements inactive.

Problem Fix/Work around

To ensure the highest accuracy, set the Bandgap Calibration Register (BGCC) to get 1.100 V at V_{REF} after the chip is configured with the actual Battery Protection settings and the Discharge FET is enabled.

6. EEPROM read from application code does not work in Lock Bit Mode 3

When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

Problem Fix/Work around

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

9.3 Rev 2548D - 06/05

1. Updated Section 8. ”Errata” on page 19.

9.4 Rev 2548C - 05/05

1. Updated Section 8. ”Errata” on page 19.

9.5 Rev 2548B - 04/05

1. Typos updated, bit “PSRASY” removed, CS12:0 renamed CS1[2:0].
2. Removed “BGEN” bit in BGCCR register. The bandgap voltage reference is always enabled in ATmega406 revision E.
3. Updated Figure 2-1 on page 3, Figure 6-1 on page 25, Figure 24-9 on page 137, Figure 21-1 on page 120.
4. Updated Table 7-2 on page 33, Table 7-3 on page 34, Table 8-1 on page 38, Table 26-5 on page 181, Figure 27-1 on page 188.
5. Updated Section 12.3.2 ”Alternate Functions of Port A” on page 66 and Section 21. ”Battery Protection” on page 118 description.
6. Updated registers ”External Interrupt Flag Register – EIFR” on page 55 and ”Timer/Counter Control Register B – TCCR0B” on page 89.
7. Updated Section 17.1 ”Features” on page 103 and Section 17.2 ”Operation” on page 103.
   Updated Section 19.1 ”Features” on page 111.
   Updated Section 20.2 ”Register Description for Voltage Reference and Temperature Sensor” on page 116.
8. Updated Section 29. ”Electrical Characteristics” on page 211.
9. Updated Section 35. ”Errata” on page 225.

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