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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc924fdh-518

7. Special function registers

Remark: Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must not attempt to access any SFR locations not deÞned.
- Accesses to any deÞned SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled Ô-Õ, Ô0Õ or Ô1Õ can be written and read as follows:
  - Ô-Õ Unless otherwise speciÞed, must be written with Ô0Õ, but can return any value when read (even if it was written with Ô0Õ). It is a reserved bit and may be used in future derivatives.
  - Ô0Õ must be written with Ô0Õ, and will return a Ô0Õ when read.
  - Ô1Õ must be written with Ô1Õ, and will return a Ô1Õ when read.

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Table 4: Special function registers *Écontinued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	00000000
SP	Stack pointer	81H									07	00000111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0xxx0
		Bit address	8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	00000000
TH0	Timer 0 HIGH	8CH									00	00000000
TH1	Timer 1 HIGH	8DH									00	00000000
TL0	Timer 0 LOW	8AH									00	00000000
TL1	Timer 1 LOW	8BH									00	00000000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	00000000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is Ô0Õ. If any are written while BRGEN = 1, the result is unpredictable.

[3] The RSTSRC register reßects the cause of the P89LPC924/925 reset. Upon a power-up reset, all reset source ßags are cleared except POF and BOF; the power-on reset value is xx110000.

[4] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all Ô1Õ, WDRUN = 1 and WDCLK = 1. WDTOF bit is Ô1Õ after watchdog reset and is Ô0Õ after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

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the minimum speciÞed operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum speciÞed operating voltage.

8.2.6 Clock output

The P89LPC924/925 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on X1) and if the Real-Time clock is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC924/925. This output is enabled by the ENCLK bit in the TRIM register. The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

8.3 On-chip RC oscillator option

The P89LPC924/925 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz, ±1% at room temperature. End-user applications can write to the Trim register to adjust the on-chip RC oscillator to other frequencies.

8.4 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

8.5 External clock input option

In this conÞguration, the processor clock is derived from an external source driving the XTAL1/P3.1 pin. The rate may be from 0 Hz up to 18 MHz. The XTAL2/P3.0 pin may be used as a standard port pin or a clock output. When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its speciÞed level. When system power is removed V_{DD} will fall below the minimum speciÞed operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum speciÞed operating voltage.

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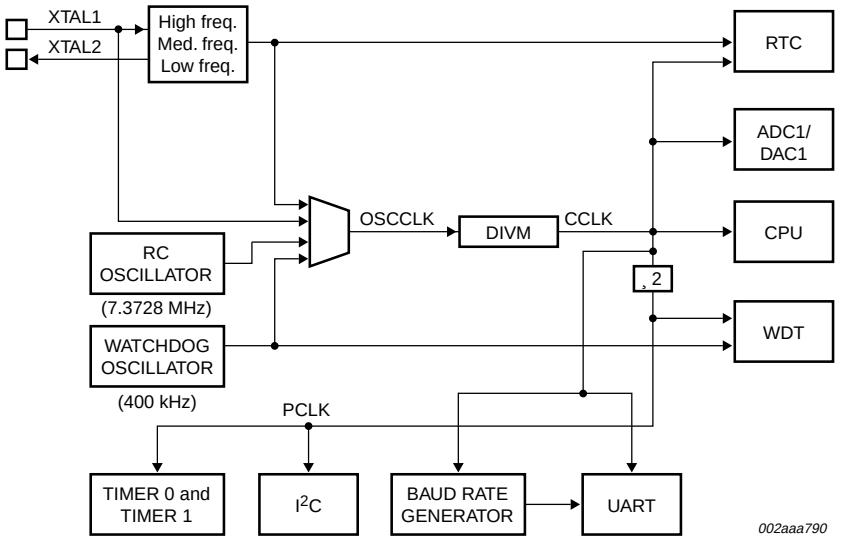

Fig 4. Block diagram of oscillator control.

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8.6 CPU Clock (CCLK) wake-up delay

The P89LPC924/925 has an internal wake-up timer that delays the clock until it stabilizes depending to the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 to 100 μs.

8.7 CPU Clock (CCLK) modiÞcation: DIVM register

The OSCCLK frequency can be divided down up to 510 times by conÞguring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.8 Low power select

The P89LPC924/925 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to Ô1Õ to lower the power consumption further. On any reset, CLKLP is Ô0Õ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

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8.9.5 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

8.9.6 DAC output to a port pin with high output impedance

The A/D converterÕs DAC block can be output to a port pin. In this mode, the AD1DAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC, the DAC output will appear on the channel 3 pin.

8.9.7 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.9.8 Power-down and idle mode

In idle mode the A/D converter, if enabled, will continue to function and can cause the device to exit idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total power-down mode, the A/D does not function. If the A/D is enabled, it will consume power. Power can be reduced by disabling the A/D.

8.10 Memory organization

The various P89LPC924/925 memory spaces are as follows:

- ¥DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the Stack may be in this area.

- ¥IDATA

  Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- ¥SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- ¥CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC924/925 has 4 kB/8 kB of on-chip Code memory.

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8.11 Data RAM arrangement

The 256 bytes of on-chip RAM are organized as shown in Table 5.

Table 5: On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256

8.12 Interrupts

The P89LPC924/925 uses a four priority level interrupt structure. This allows great ßexibility in controlling the handling of the many interrupt sources. The P89LPC924/925 supports 13 interrupt sources: A/D converter, external interrupts 0 and 1, timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/real-time clock, I^2C, keyboard, and comparators 1 and 2.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.12.1 External interrupt inputs

The P89LPC924/925 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request ßag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC924/925 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.15 ÒPower reduction modesó for details.

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8.13.1 Port conÞgurations

All but three I/O port pins on the P89LPC924/925 may be conÞgured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two conÞguration registers for each port select the output type for each port pin.

P1.5 ($\overline{RST}$) can only be an input and cannot be conÞgured.

P1.2 (SCL/T0) and P1.3 (SDA/$\overline{INT0}$) may only be conÞgured to be either input-only or open-drain.

8.13.2 Quasi-bidirectional output conÞguration

Quasi-bidirectional output type can be used as both an input and output without the need to reconÞgure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC924/925 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current ßowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.3 Open-drain output conÞguration

The open-drain output conÞguration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic Ô0Õ. To be used as a logic output, a port conÞgured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.4 Input-only conÞguration

The input-only port conÞguration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.5 Push-pull output conÞguration

The push-pull output conÞguration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic Ô1Õ. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.6 Port 0 analog functions

The P89LPC924/925 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

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8.20 I²C-bus serial interface

I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- ¥ Bidirectional data transfer between masters and slaves
- ¥ Multimaster bus (no central master)
- ¥ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- ¥ Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- ¥ Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- ¥ The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus conÞguration is shown in Figure 8. The P89LPC924/925 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

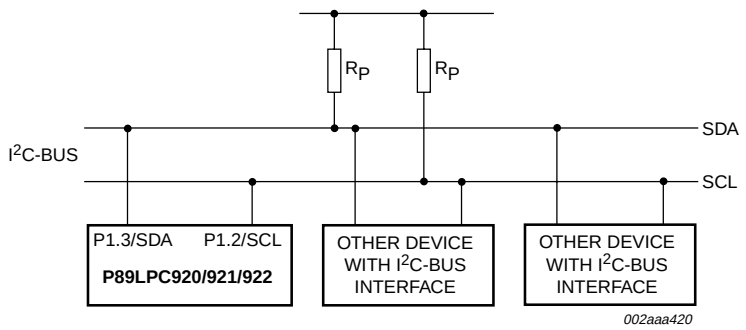

Fig 8. I²C-bus conÞguration.

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8.21 Analog comparators

Two analog comparators are provided on the P89LPC924/925. Input and output options allow use of the comparators in a number of different conÞgurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be conÞgured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 10. The comparators function to V_{DD} = 2.4 V.

When each comparator is Þrst enabled, the comparator output and interrupt ßag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt ßag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparatorÕs output, COx, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator ßag, CMFx. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator ßag, CMFx, after disabling the comparator.

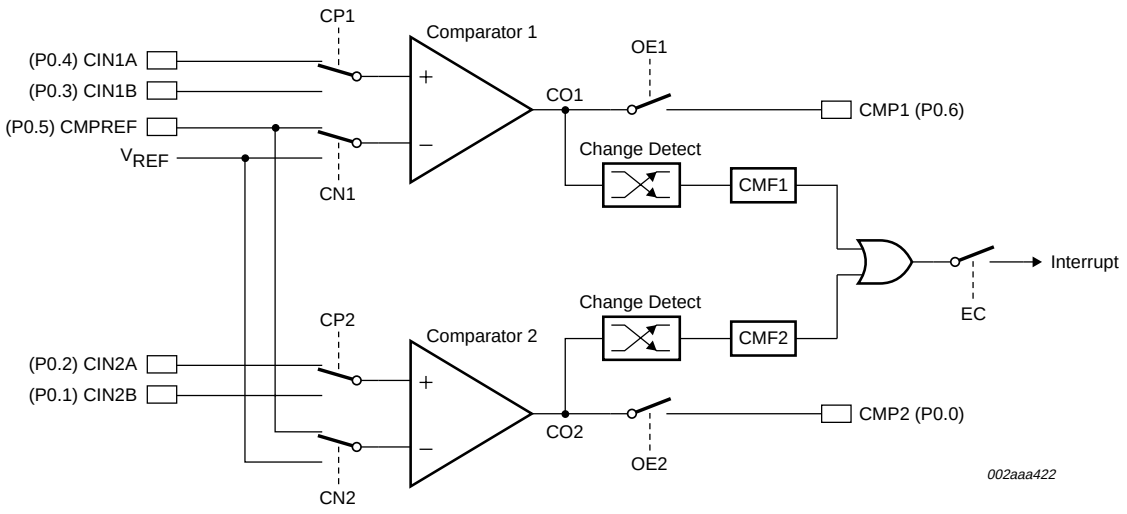

Fig 10. Comparator input and output connections.

8.21.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{REF}, is 1.23 V ±10%.

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8.21.2 Comparator interrupt

Each comparator has an interrupt ßag contained in its conÞguration register. This ßag is set whenever the comparator output changes state. The ßag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the ßags to determine which comparator caused the interrupt.

8.21.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode. If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be conÞgured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

8.22 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can conÞgure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to deÞne which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to deÞne a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to deÞne equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the ßag and cause an interrupt, the pattern on Port 0 must be held longer than 6 CCLKs.

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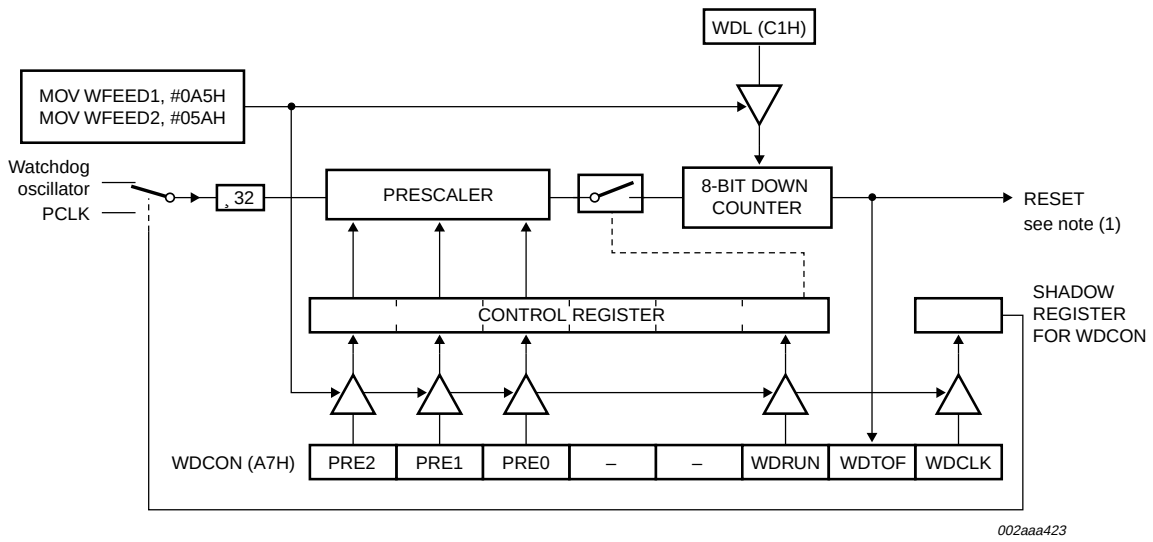
8.23 Watchdog timer

The watchdog timer causes a system reset when it underßows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz Watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 11 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered-down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few ms to a few seconds. Please refer to the *P89LPC924/925* UserÕs Manual for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 11. Watchdog timer in Watchdog mode (WDTE = Ô1Õ).

8.24 Additional features

8.24.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

8.24.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic Ô0Õ so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

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10. Static characteristics

Table 8: DC electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise speciÞed.

T_{amb} = - 40 °C to +85 °C for industrial, unless otherwise speciÞed.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$I_{DD(oper)}$	power supply current, operating	3.6 V; 12 MHz	[2]	-	9	15	mA
		3.6 V; 18 MHz	[2]	-	14	23	mA
$I_{DD(idle)}$	power supply current, Idle mode	3.6 V; 12 MHz	[2]	-	3.25	5	mA
		3.6 V; 18 MHz	[2]	-	5	7	mA
$I_{DD(PD)}$	power supply current, Power-down mode, voltage comparators powered-down	3.6 V	[2]	-	55	80	mA
$I_{DD(TPD)}$	power supply current, Total Power-down mode	3.6 V	[2]	-	1	5	mA
$(dV_{DD}/dt)_r$	V_{DD} rise rate			-	-	2	mV/ms
$(dV_{DD}/dt)_f$	V_{DD} fall rate			-	-	50	mV/ms
V_{POR}	Power-on reset detect voltage			-	-	0.2	V
V_{RAM}	RAM keep-alive voltage			1.5	-	-	V
$V_{th(HL)}$	negative-going threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		- 0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	positive-going threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	Port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage; all ports, all modes except Hi-Z	I_{OL} = 20 mA	[3]	-	0.6	1.0	V
		I_{OL} = 3.2 mA	[3]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage, all ports	I_{OH} = - 3.2 mA; push-pull mode		V_{DD} - 0.7	V_{DD} - 0.4	-	V
		I_{OH} = - 20 mA; quasi-bidirectional mode		V_{DD} - 0.3	V_{DD} - 0.2	-	V
C_{ig}	input/output pin capacitance		[4]	-	-	15	pF
I_{IL}	logical 0 input current, all ports	V_{IN} = 0.4 V	[5]	-	-	- 80	mA
I_{LI}	input leakage current, all ports	V_{IN} = V_{IL} or V_{IH}	[6]	-	-	± 10	mA
I_{TL}	logical 1-to-0 transition current, all ports	V_{IN} = 2.0 V at V_{DD} = 3.6 V	[7], [8]	- 30	-	- 450	mA
R_{RST}	internal reset pull-up resistor			10	-	30	kW

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15. Revision history

Table 14: Revision history

Rev	Date	CPCN	Description
03	20041215	-	Product data (9397 750 14471) ModiÞcation: ¥ Added 18 MHz information.
02	20040615	-	Product data (9397 750 13459)
01	20040309	-	Objective data (9397 750 12879)

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Contents

1 General description . . . 1
2 Features . . . 1
2.1 Principal features . . . 1
2.2 Additional features . . . 2
3 Ordering information . . . 3
3.1 Ordering options . . . 3
4 Block diagram . . . 4
5 Pinning information . . . 5
5.1 Pinning . . . 5
5.2 Pin description . . . 6
6 Logic symbol . . . 8
7 Special function registers . . . 9
8 Functional description . . . 14
8.1 Enhanced CPU . . . 14
8.2 Clocks . . . 14
8.2.1 Clock deÞnitions . . . 14
8.2.2 CPU clock (OSCCLK) . . . 14
8.2.3 Low speed oscillator option . . . 14
8.2.4 Medium speed oscillator option . . . 14
8.2.5 High speed oscillator option . . . 14
8.2.6 Clock output . . . 15
8.3 On-chip RC oscillator option . . . 15
8.4 Watchdog oscillator option . . . 15
8.5 External clock input option . . . 15
8.6 CPU Clock (CCLK) wake-up delay . . . 17
8.7 CPU Clock (CCLK) modiÞcation: DIVM register . . . 17
8.8 Low power select . . . 17
8.9 A/D converter . . . 18
8.9.1 General description . . . 18
8.9.2 Features . . . 19
8.9.3 A/D operating modes . . . 19
8.9.4 Conversion start modes . . . 20
8.9.5 Boundary limits interrupt . . . 21
8.9.6 DAC output to a port pin with high output impedance 21
8.9.7 Clock divider . . . 21
8.9.8 Power-down and idle mode . . . 21
8.10 Memory organization . . . 21
8.11 Data RAM arrangement . . . 22
8.12 Interrupts . . . 22
8.12.1 External interrupt inputs . . . 22
8.13 I/O ports . . . 23
8.13.1 Port conÞgurations . . . 24
8.13.2 Quasi-bidirectional output conÞguration . . . 24
8.13.3 Open-drain output conÞguration . . . 24
8.13.4 Input-only conÞguration . . . 24
8.13.5 Push-pull output conÞguration . . . 24
8.13.6 Port 0 analog functions . . . 24
8.13.7 Additional port features . . . 25
8.14 Power monitoring functions . . . 25
8.14.1 Brownout detection . . . 25
8.14.2 Power-on detection . . . 25
8.15 Power reduction modes . . . 26
8.15.1 Idle mode . . . 26
8.15.2 Power-down mode . . . 26
8.15.3 Total Power-down mode . . . 26
8.16 Reset . . . 26
8.16.1 Reset vector . . . 27
8.17 Timers/counters 0 and 1 . . . 27
8.17.1 Mode 0 . . . 28
8.17.2 Mode 1 . . . 28
8.17.3 Mode 2 . . . 28
8.17.4 Mode 3 . . . 28
8.17.5 Mode 6 . . . 28
8.17.6 Timer overßow toggle output . . . 28
8.18 Real-Time clock/system timer . . . 28
8.19 UART . . . 28
8.19.1 Mode 0 . . . 29
8.19.2 Mode 1 . . . 29
8.19.3 Mode 2 . . . 29
8.19.4 Mode 3 . . . 29
8.19.5 Baud rate generator and selection . . . 29
8.19.6 Framing error . . . 30
8.19.7 Break detect . . . 30
8.19.8 Double buffering . . . 30
8.19.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3) . . . 30
8.19.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3) . . . 30
8.20 I^2C-bus serial interface . . . 31
8.21 Analog comparators . . . 33
8.21.1 Internal reference voltage . . . 33
8.21.2 Comparator interrupt . . . 34
8.21.3 Comparators and power reduction modes . . . 34
8.22 Keypad interrupt (KBI) . . . 34
8.23 Watchdog timer . . . 35
8.24 Additional features . . . 35
8.24.1 Software reset . . . 35
8.24.2 Dual data pointers . . . 35
8.25 Flash program memory . . . 36
8.25.1 General description . . . 36
8.25.2 Features . . . 36
8.25.3 ISP and IAP capabilities of the P89LPC924/925 . . . 36
8.26 User conÞguration bytes . . . 38
8.27 User sector security bytes . . . 38
9 Limiting values . . . 39
10 Static characteristics . . . 40
11 Dynamic characteristics . . . 42
12 Comparator electrical characteristics . . . 45
13 A/D converter electrical characteristics . . . 45
14 Package outline . . . 46
15 Revision history . . . 47
16 Data sheet status . . . 48
17 DeÞnitions . . . 48
18 Disclaimers . . . 48
19 Licenses . . . 48

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