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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I <sup>2</sup> C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc925fdhy">https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc925fdhy</a>

## 4. Block diagram

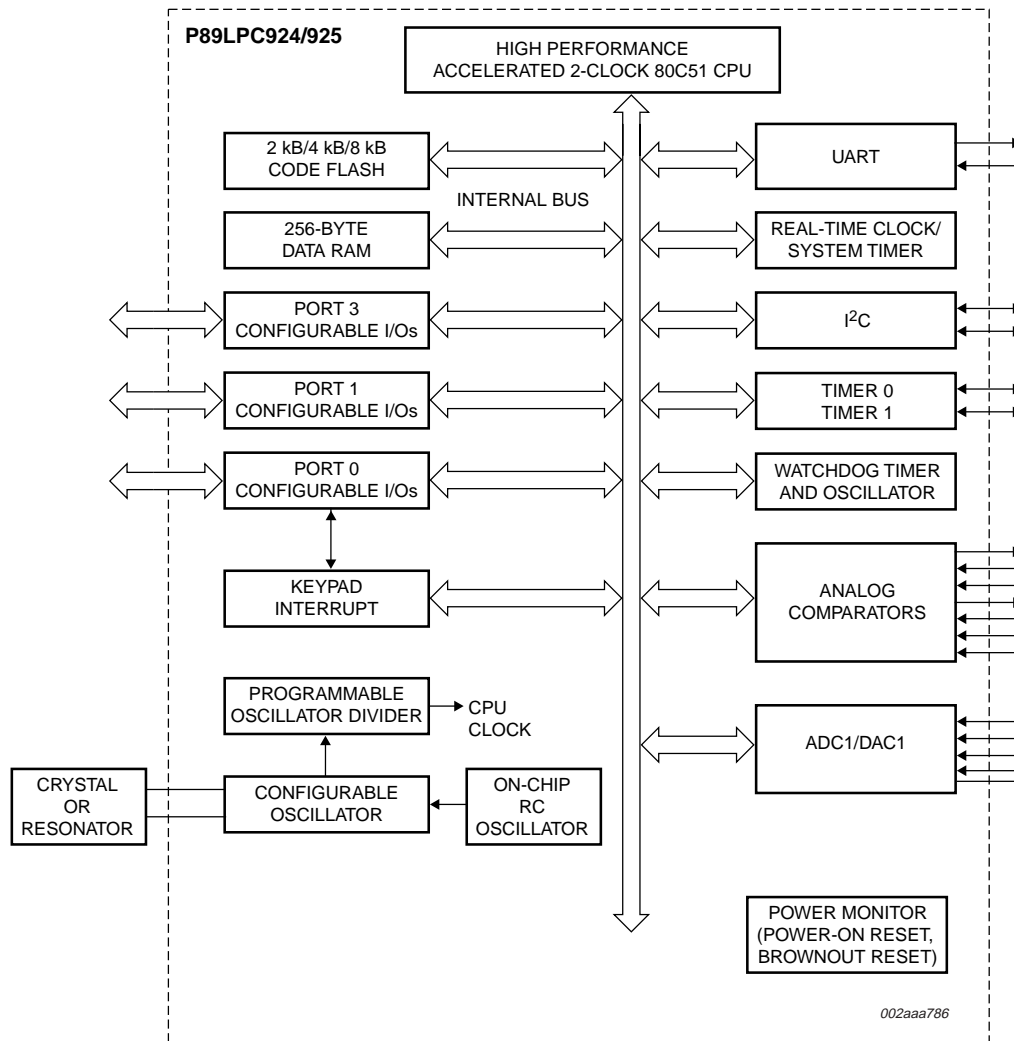
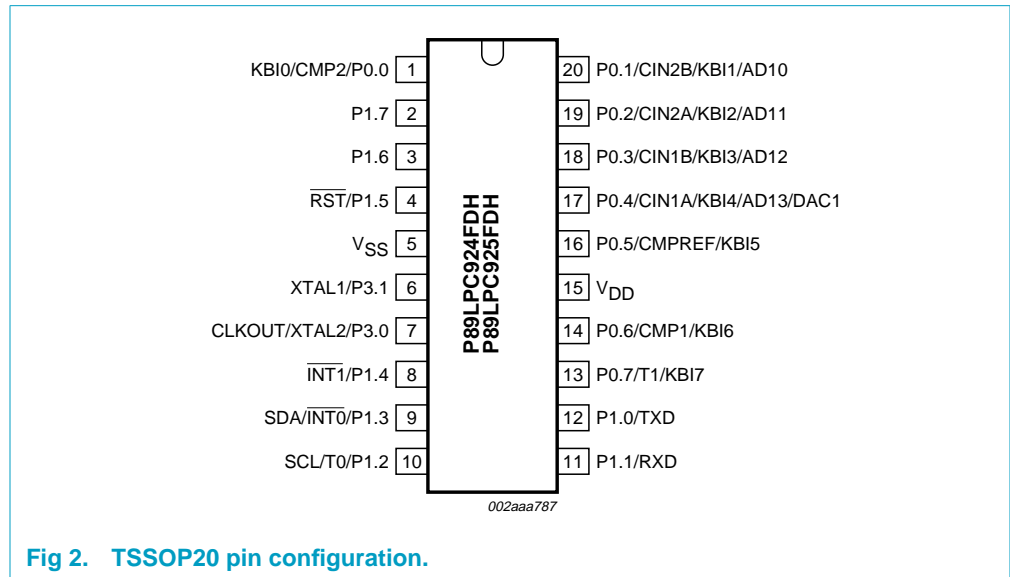


Fig 1. Block diagram.

## 5. Pinning information

### 5.1 Pinning



**Fig 2. TSSOP20 pin configuration.**

Table 3: Pin description...continued

Symbol	Pin	Type	Description
P1.0 - P1.7	12, 11, 10, 9, 8, 4, 3, 2	I/O, I <sup>[1]</sup>	<p><b>Port 1:</b> Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to <a href="#">Section 8.13.1 "Port configurations"</a> and <a href="#">Table 8 "DC electrical characteristics"</a> for details. P1.2 - P1.3 are open drain when used as outputs. P1.5 is input only.</p> <p>All pins have Schmitt triggered inputs.</p> <p>Port 1 also provides various special functions as described below:</p>
	12	I/O	<b>P1.0</b> — Port 1 bit 0.
		O	<b>TXD</b> — Transmitter output for the serial port.
	11	I/O	<b>P1.1</b> — Port 1 bit 1.
		I	<b>RXD</b> — Receiver input for the serial port.
	10	I/O	<b>P1.2</b> — Port 1 bit 2 (open-drain when used as output).
		I/O	<b>T0</b> — Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	<b>SCL</b> — I <sup>2</sup> C serial clock input/output.
	9	I/O	<b>P1.3</b> — Port 1 bit 3 (open-drain when used as output).
		I	<b>INT0</b> — External interrupt 0 input.
		I/O	<b>SDA</b> — I <sup>2</sup> C serial data input/output.
	8	I/O	<b>P1.4</b> — Port 1 bit 4.
		I	<b>INT1</b> — External interrupt 1 input.
	4	I	<b>P1.5</b> — Port 1 bit 5 (input only).
		I	<b>RST</b> — External Reset input (if selected via FLASH configuration). A LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. <b>When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V<sub>DD</sub> has reached its specified level. When system power is removed V<sub>DD</sub> will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V<sub>DD</sub> falls below the minimum specified operating voltage.</b>
	3	I/O	<b>P1.6</b> — Port 1 bit 6.
	2	I/O	<b>P1.7</b> — Port 1 bit 7.

Table 3: Pin description...continued

Symbol	Pin	Type	Description
P3.0 - P3.1	7, 6	I/O	<b>Port 3:</b> Port 3 is an 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to <a href="#">Section 8.13.1 "Port configurations"</a> and <a href="#">Table 8 "DC electrical characteristics"</a> for details.  All pins have Schmitt triggered inputs.  Port 3 also provides various special functions as described below:
	7	I/O	<b>P3.0</b> — Port 3 bit 0.
		O	<b>XTAL2</b> — Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration).
		O	<b>CLKOUT</b> — CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the real time clock/system timer.
	6	I/O	<b>P3.1</b> — Port 3 bit 1.
		I	<b>XTAL1</b> — Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, <b>and</b> if XTAL1/XTAL2 are not used to generate the clock for the real time clock/system timer.
V <sub>SS</sub>	5	I	<b>Ground:</b> 0 V reference.
V <sub>DD</sub>	15	I	<b>Power Supply:</b> This is the power supply voltage for normal operation as well as Idle and Power Down modes.

[1] Input/Output for P1.0-P1.4, P1.6, P1.7. Input for P1.5.

## 6. Logic symbol

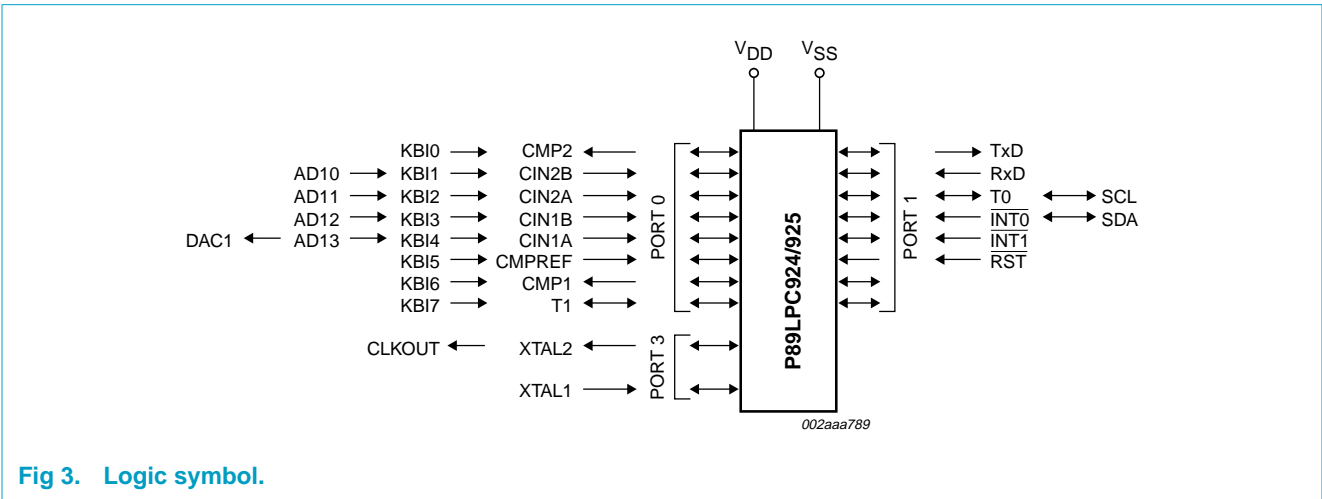


Fig 3. Logic symbol.

**Table 4: Special function registers...continued**

\* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
											Hex	Binary
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	00000000
SP	Stack pointer	81H									07	00000111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0xxx0
Bit address			8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	00000000
TH0	Timer 0 HIGH	8CH									00	00000000
TH1	Timer 1 HIGH	8DH									00	00000000
TL0	Timer 0 LOW	8AH									00	00000000
TL1	Timer 1 LOW	8BH									00	00000000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	00000000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

- [1] All ports are in input only (high impedance) state after power-up.
- [2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any are written while BRGEN = 1, the result is unpredictable.
- [3] The RSTSRC register reflects the cause of the P89LPC924/925 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.
- [4] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all '1', WDRUN = 1 and WDCLK = 1. WDTOF bit is '1' after watchdog reset and is '0' after power-on reset. Other resets will not affect WDTOF.
- [5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.
- [6] The only reset source that affects these SFRs is power-on reset.

## 8.9 A/D converter

### 8.9.1 General description

The P89LPC924/925 has an 8-bit, 4-channel multiplexed successive approximation analog-to-digital converter module. A block diagram of the A/D converter is shown in Figure 5. The A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the successive approximation register (SAR) drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.

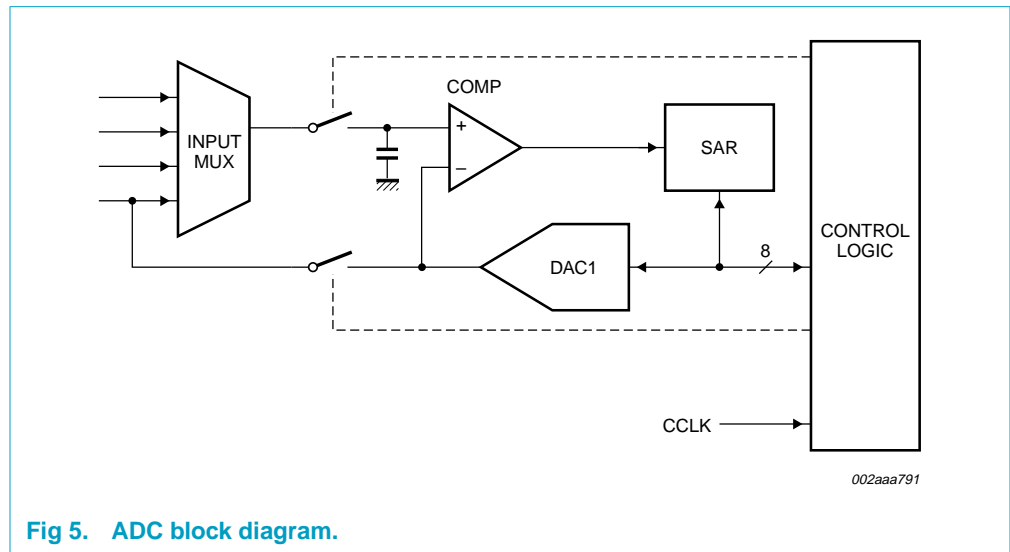


Fig 5. ADC block diagram.

### 8.9.5 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

### 8.9.6 DAC output to a port pin with high output impedance

The A/D converter's DAC block can be output to a port pin. In this mode, the AD1DAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC, the DAC output will appear on the channel 3 pin.

### 8.9.7 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

### 8.9.8 Power-down and idle mode

In idle mode the A/D converter, if enabled, will continue to function and can cause the device to exit idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total power-down mode, the A/D does not function. If the A/D is enabled, it will consume power. Power can be reduced by disabling the A/D.

## 8.10 Memory organization

The various P89LPC924/925 memory spaces are as follows:

- DATA  
128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the Stack may be in this area.
- IDATA  
Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.
- SFR  
Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.
- CODE  
64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC924/925 has 4 kB/8 kB of on-chip Code memory.



### 8.13.1 Port configurations

All but three I/O port pins on the P89LPC924/925 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ( $\overline{\text{RST}}$ ) can only be an input and cannot be configured.

P1.2 (SCL/T0) and P1.3 (SDA/ $\overline{\text{INT0}}$ ) may only be configured to be either input-only or open-drain.

### 8.13.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC924/925 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to  $V_{DD}$ , causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

### 8.13.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic '0'. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to  $V_{DD}$ .

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

### 8.13.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

### 8.13.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic '1'. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

### 8.13.6 Port 0 analog functions

The P89LPC924/925 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high impedance) mode as described in [Section 8.13.4](#).

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD1:5 defaults to '0's to enable digital functions.

#### 8.13.7 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC924/925 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to [Table 8 "DC electrical characteristics"](#) for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

### 8.14 Power monitoring functions

The P89LPC924/925 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on Detect and Brownout detect.

#### 8.14.1 Brownout detection

The Brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a Brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If Brownout detection is enabled, the brownout condition occurs when  $V_{DD}$  falls below the brownout trip voltage,  $V_{BO}$  (see [Table 8 "DC electrical characteristics"](#)), and is negated when  $V_{DD}$  rises above  $V_{BO}$ . If the P89LPC924/925 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the  $V_{DD}$  rise and fall times must be observed. Please see [Table 8 "DC electrical characteristics"](#) for specifications.

#### 8.14.2 Power-on detection

The Power-on Detect has a function similar to the Brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

## 8.15 Power reduction modes

The P89LPC924/925 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

### 8.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

### 8.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC924/925 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage  $V_{RAM}$ . This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after  $V_{DD}$  has been lowered to  $V_{RAM}$ , therefore it is highly recommended to wake up the processor via reset in this case.  $V_{DD}$  must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down. These include: Brownout detect, Watchdog Timer, Comparators (note that Comparators can be powered-down separately), and Real-Time Clock (RTC)/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock AND the RTC is enabled.

### 8.15.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during Power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the Real-Time Clock running during Power-down.

## 8.16 Reset

The P1.5/ $\overline{RST}$  pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to '1', enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

**Remark:** During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

**Remark:** During a power cycle,  $V_{DD}$  must fall below  $V_{POR}$  (see Table 8 “DC electrical characteristics” on page 40) before power is reapplied, in order to ensure a power-on reset.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1. This option must be used for an oscillator frequency above 12 MHz);
- Power-on detect;
- Brownout detect;
- Watchdog Timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a '0' to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

#### 8.16.1 Reset vector

Following reset, the P89LPC924/925 will fetch instructions from either address 0000h or the Boot address. The Boot address is formed by using the Boot Vector as the high byte of the address and the low byte of the address = 00h.

The Boot address will be used if a UART break reset occurs, or the non-volatile Boot Status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC924/925 User's Manual*). Otherwise, instructions will be fetched from address 0000H.

### 8.17 Timers/counters 0 and 1

The P89LPC924/925 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counter. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

**8.17.1 Mode 0**

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

**8.17.2 Mode 1**

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

**8.17.3 Mode 2**

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

**8.17.4 Mode 3**

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

**8.17.5 Mode 6**

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

**8.17.6 Timer overflow toggle output**

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

**8.18 Real-Time clock/system timer**

The P89LPC924/925 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all '0's, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

**8.19 UART**

The P89LPC924/925 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC924/925 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

**8.19.1 Mode 0**

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at  $\frac{1}{16}$  of the CPU clock frequency.

**8.19.2 Mode 1**

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical '0'), 8 data bits (LSB first), and a stop bit (logical '1'). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in [Section 8.19.5 "Baud rate generator and selection"](#)).

**8.19.3 Mode 2**

11 bits are transmitted (through TxD) or received (through RxD): start bit (logical '0'), 8 data bits (LSB first), a programmable 9<sup>th</sup> data bit, and a stop bit (logical '1'). When data is transmitted, the 9<sup>th</sup> data bit (TB8 in SCON) can be assigned the value of '0' or '1'. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9<sup>th</sup> data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either  $\frac{1}{16}$  or  $\frac{1}{32}$  of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

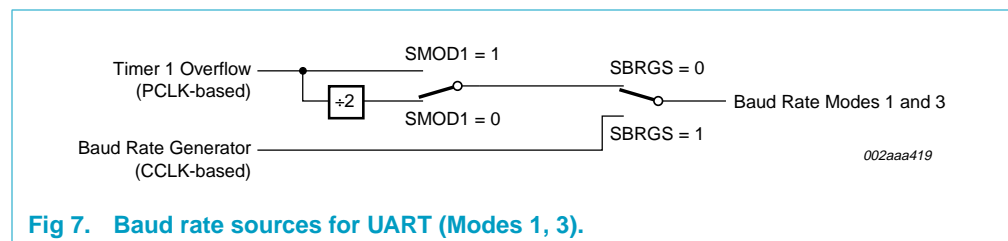
**8.19.4 Mode 3**

11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical '0'), 8 data bits (LSB first), a programmable 9<sup>th</sup> data bit, and a stop bit (logical '1'). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in [Section 8.19.5 "Baud rate generator and selection"](#)).

**8.19.5 Baud rate generator and selection**

The P89LPC924/925 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see [Figure 7](#)). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is set. The independent Baud Rate Generator uses OSCCLK.



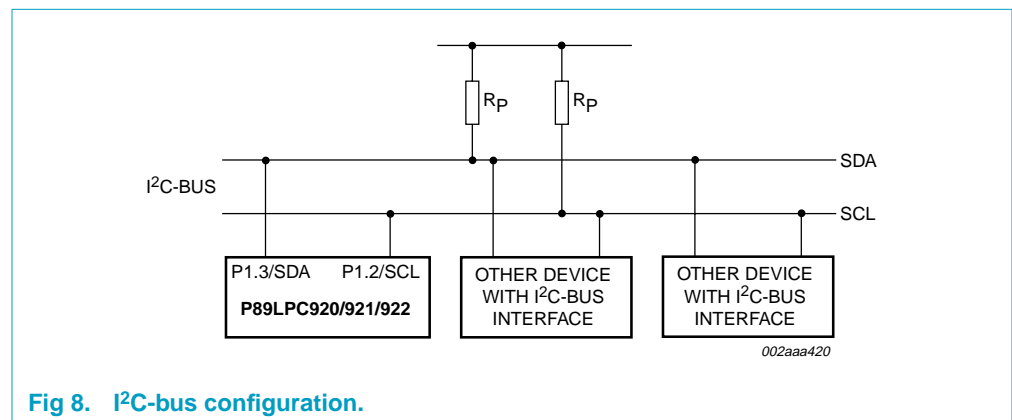
**Fig 7. Baud rate sources for UART (Modes 1, 3).**

## 8.20 I<sup>2</sup>C-bus serial interface

I<sup>2</sup>C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multimaster bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I<sup>2</sup>C-bus may be used for test and diagnostic purposes.

A typical I<sup>2</sup>C-bus configuration is shown in **Figure 8**. The P89LPC924/925 device provides a byte-oriented I<sup>2</sup>C-bus interface that supports data transfers up to 400 kHz.



**Fig 8. I<sup>2</sup>C-bus configuration.**

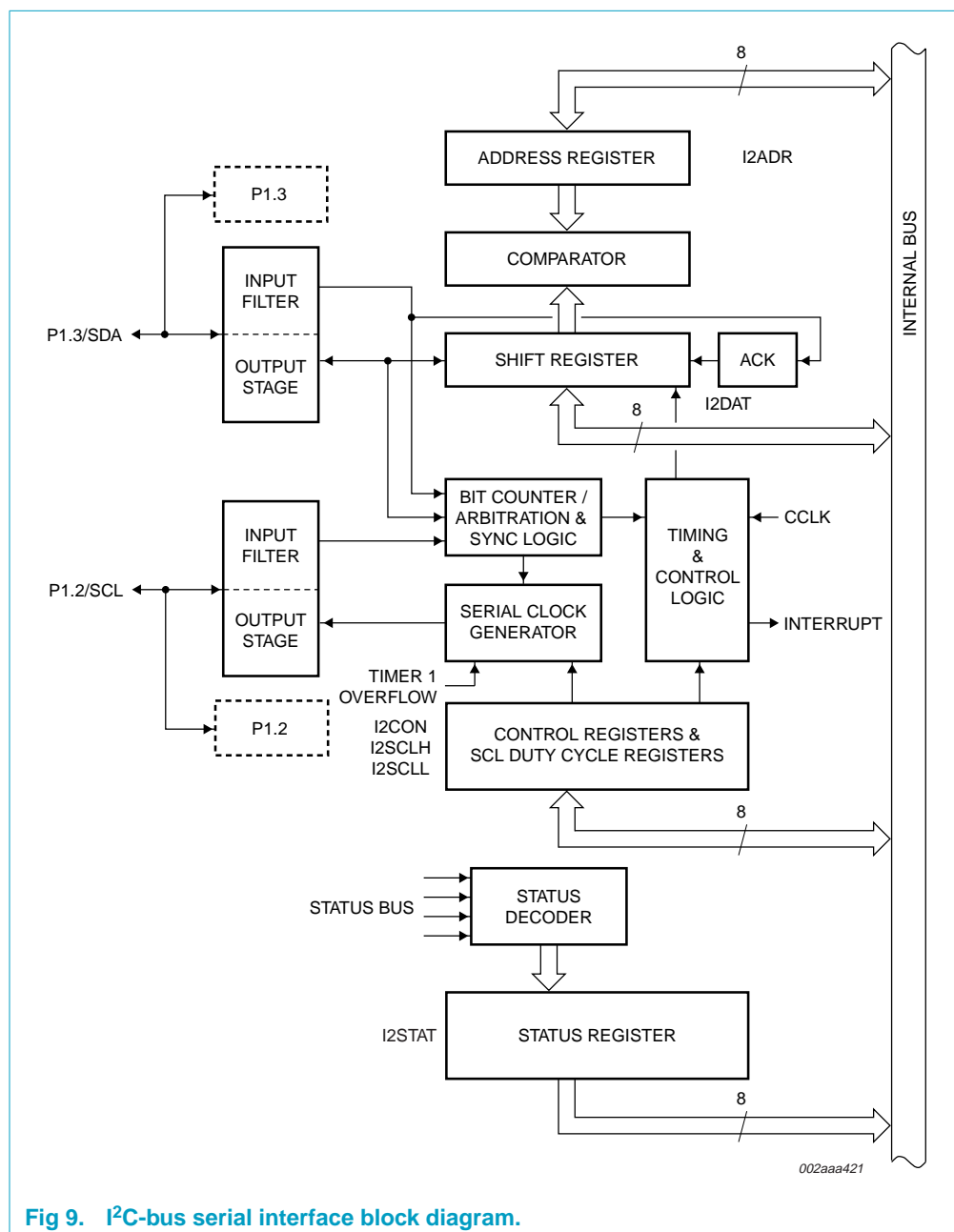


Fig 9. I²C-bus serial interface block diagram.



## 9. Limiting values

**Table 7: Limiting values<sup>[1]</sup>**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{\text{amb(bias)}}$	operating bias ambient temperature		−55	+125	°C
$T_{\text{stg}}$	storage temperature range		−65	+150	°C
$V_{\text{xtal}}$	voltage on XTAL1, XTAL2 pin to $V_{\text{SS}}$		-	$V_{\text{DD}} + 0.5$	V
$V_{\text{n}}$	voltage on any other pin to $V_{\text{SS}}$		−0.5	+5.5	V
$I_{\text{OH(I/O)}}$	HIGH-level output current per I/O pin		-	8	mA
$I_{\text{OL(I/O)}}$	LOW-level output current per I/O pin		-	20	mA
$I_{\text{I/O(tot)(max)}}$	maximum total I/O current		-	80	mA
$P_{\text{tot(pack)}}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Limiting values:

- Stresses above those listed under [Table 7](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in [Table 8 “DC electrical characteristics”](#), [Table 9 “AC characteristics”](#) and [Table 10 “AC characteristics”](#) of this specification are not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{\text{SS}}$  unless otherwise noted.

**Table 8: DC electrical characteristics...continued** $V_{DD} = 2.4\text{ V to }3.6\text{ V}$ , unless otherwise specified. $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$  for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{BO}$	brownout trip voltage with BOV = '0', BOPD = '1'	$2.4\text{ V} < V_{DD} < 3.6\text{ V}$	2.40	-	2.70	V
$V_{REF}$	bandgap reference voltage		1.11	1.23	1.34	V
$TC_{(V_{REF})}$	bandgap temperature coefficient		-	10	20	ppm/ $^{\circ}\text{C}$

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The  $I_{DD(oper)}$ ,  $I_{DD(idle)}$ , and  $I_{DD(PD)}$  specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and watchdog timer.

[3] See Table 7 "Limiting values<sup>[1]</sup>" on page 39 for steady state (non-transient) limits on  $I_{OL}$  or  $I_{OH}$ . If  $I_{OL}/I_{OH}$  exceeds the test condition,  $V_{OL}/V_{OH}$  may exceed the related specification.

[4] Pin capacitance is characterized but not tested.

[5] Measured with port in quasi-bidirectional mode.

[6] Measured with port in high-impedance mode.

[7] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups). Does not apply to open-drain pins.

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from '1' to '0'. This current is highest when  $V_{IN}$  is approximately 2 V.

**Table 10: AC characteristics** $V_{DD} = 3.0\text{ V to }3.6\text{ V}$ , unless otherwise specified. $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$  for industrial, unless otherwise specified.<sup>[1]</sup>

Symbol	Parameter	Conditions	Variable clock		$f_{osc} = 18\text{ MHz}$		Unit
			Min	Max	Min	Max	
$f_{RCOSC}$	internal RC oscillator frequency (nominal $f = 7.3728\text{ MHz}$ )	trimmed to $\pm 1\%$ at $T_{amb} = 25\text{ }^{\circ}\text{C}$	7.189	7.557	7.189	7.557	MHz
$f_{WDOSC}$	internal Watchdog oscillator frequency (nominal $f = 400\text{ kHz}$ )		320	520	320	520	kHz
$f_{osc}$	oscillator frequency	[2]	0	18	-	-	MHz
$t_{CLCL}$	clock cycle	see Figure 13	55	-	-	-	ns
$f_{CLKP}$	CLKLP active frequency		0	8	-	-	MHz
<b>Glitch filter</b>							
	glitch rejection, P1.5/ $\overline{\text{RST}}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/ $\overline{\text{RST}}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/ $\overline{\text{RST}}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/ $\overline{\text{RST}}$		50	-	50	-	ns
<b>External clock</b>							
$t_{CHCX}$	HIGH time	see Figure 13	22	$t_{CLCL} - t_{CLCX}$	22	-	ns
$t_{CLCX}$	LOW time	see Figure 13	22	$t_{CLCL} - t_{CHCX}$	22	-	ns
$t_{CLCH}$	rise time	see Figure 13	-	5	-	5	ns
$t_{CHCL}$	fall time	see Figure 13	-	5	-	5	ns
<b>Shift register (UART mode 0)</b>							
$t_{XLXL}$	serial port clock cycle time		16 $t_{CLCL}$	-	888	-	ns
$t_{QVXH}$	output data set-up to clock rising edge		13 $t_{CLCL}$	-	722	-	ns
$t_{XHGX}$	output data hold after clock rising edge		-	$t_{CLCL} + 20$	-	75	ns
$t_{XHDX}$	input data hold after clock rising edge		-	0	-	0	ns
$t_{DVXH}$	input data valid to clock rising edge		150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until  $V_{DD}$  has reached its specified level. When system power is removed  $V_{DD}$  will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when  $V_{DD}$  falls below the minimum specified operating voltage.

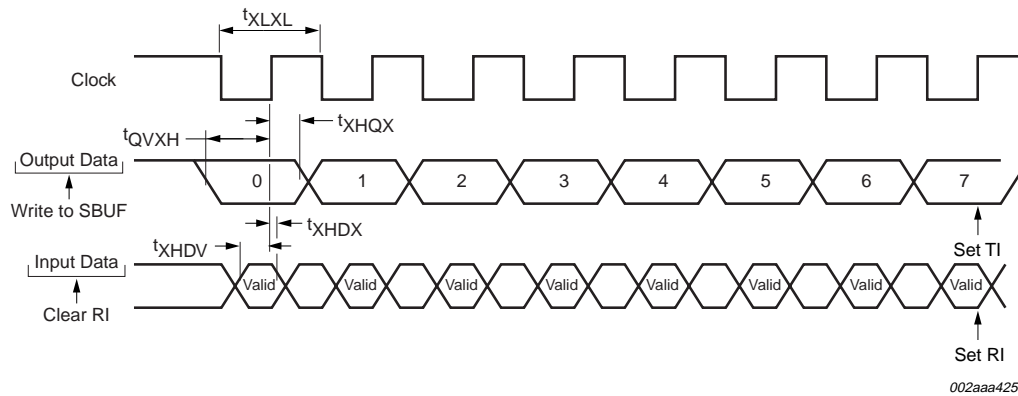


Fig 12. Shift register mode timing.

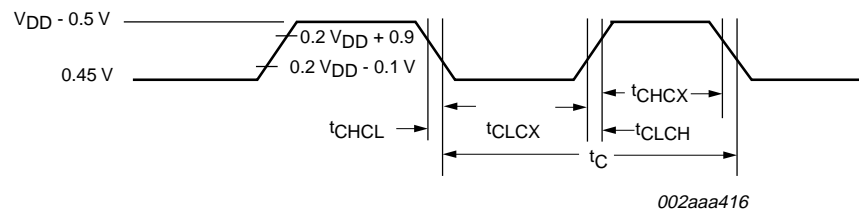


Fig 13. External clock timing.

Table 11: AC characteristics, ISP entry mode

$V_{DD} = 2.4 \text{ V to } 3.6 \text{ V}$ , unless otherwise specified.

$T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$  for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{VR}$	$\overline{\text{RST}}$ delay from $V_{DD}$ active		50	-	-	$\mu\text{s}$
$t_{RH}$	$\overline{\text{RST}}$ HIGH time		1	-	32	$\mu\text{s}$
$t_{RL}$	$\overline{\text{RST}}$ LOW time		1	-	-	$\mu\text{s}$

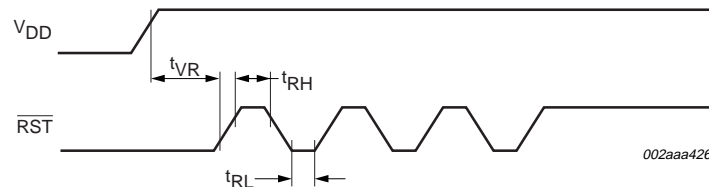


Fig 14. ISP entry waveform.

14. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

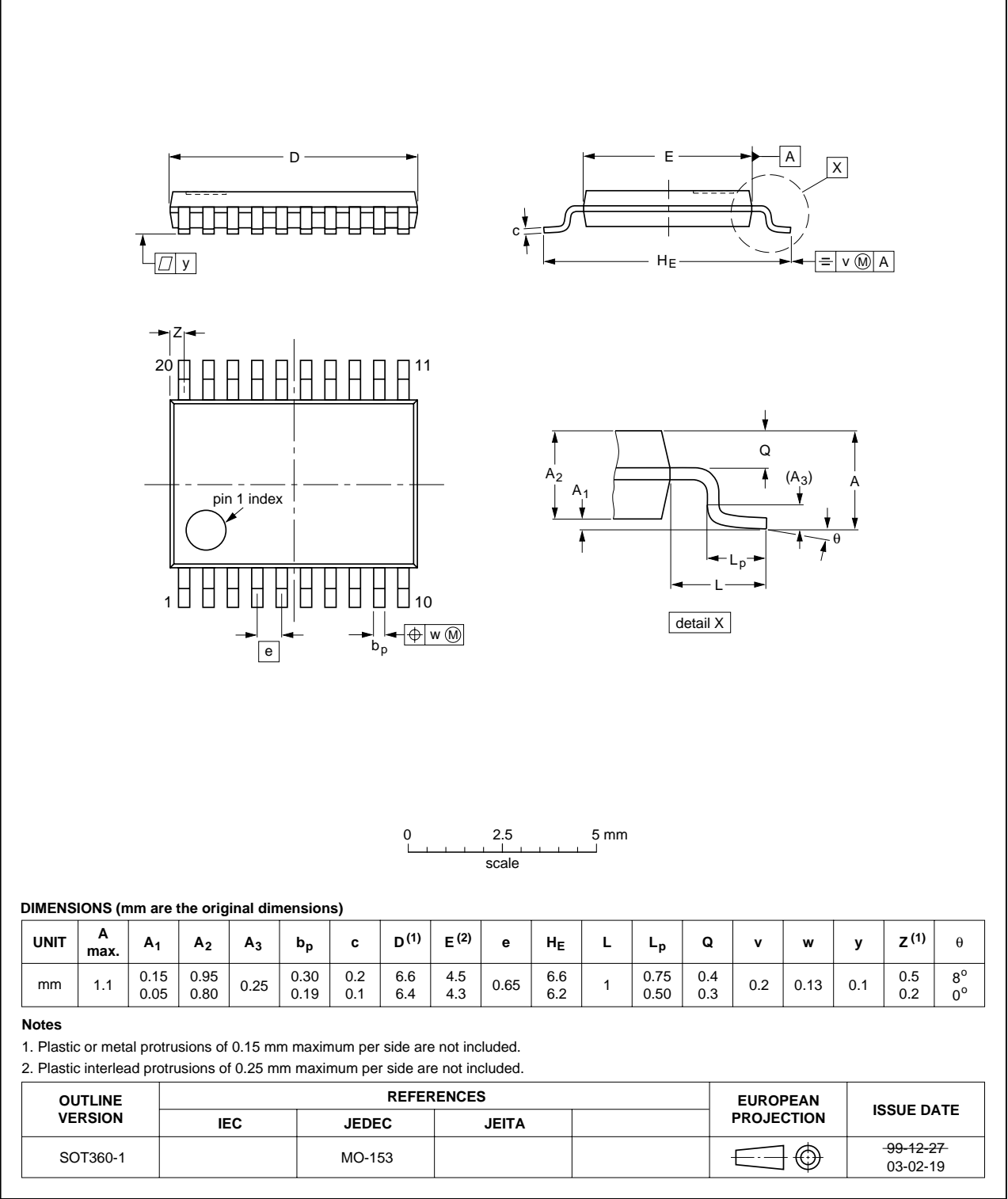


Fig 15. TSSOP20 (SOT360-1).