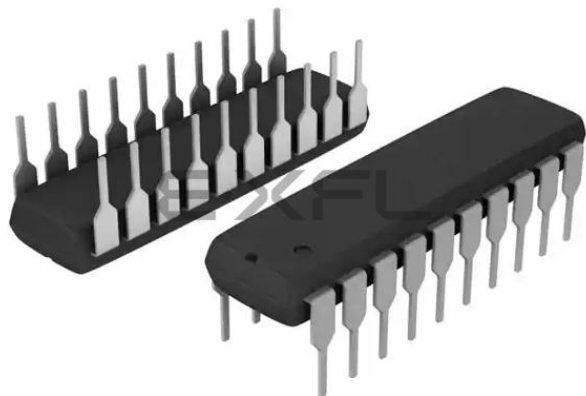




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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I ² C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc925fn-129

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LPC924FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC925FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

3.1 Ordering options

Table 2: Part options

Type number	Flash memory	Temperature range	Frequency
P89LPC924FDH	4 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC925FDH	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz

4. Block diagram

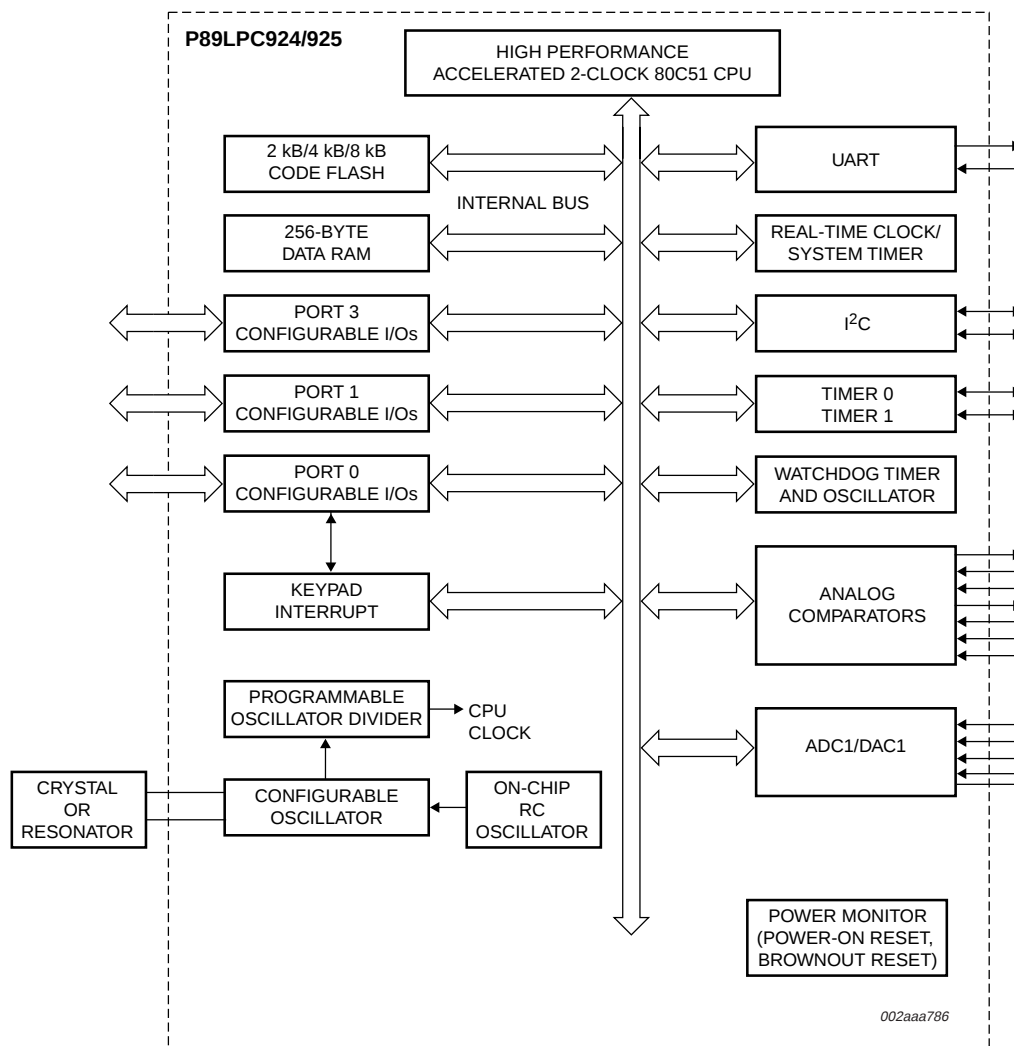


Fig 1. Block diagram.

5. Pinning information

5.1 Pinning

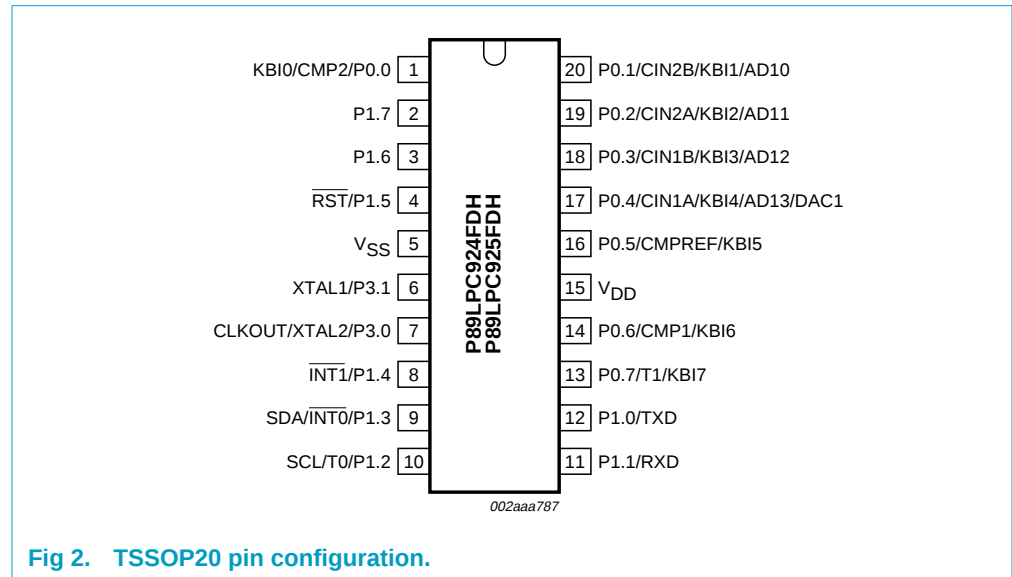


Fig 2. TSSOP20 pin configuration.

Table 3: Pin description...continued

Symbol	Pin	Type	Description
P1.0 - P1.7	12, 11, 10, 9, 8, 4, 3, 2	I/O, I ^[1]	Port 1: Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. P1.2 - P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
	12	I/O	P1.0 — Port 1 bit 0.
		O	TXD — Transmitter output for the serial port.
	11	I/O	P1.1 — Port 1 bit 1.
		I	RXD — Receiver input for the serial port.
	10	I/O	P1.2 — Port 1 bit 2 (open-drain when used as output).
		I/O	T0 — Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	SCL — I ² C serial clock input/output.
	9	I/O	P1.3 — Port 1 bit 3 (open-drain when used as output).
		I	INT0 — External interrupt 0 input.
		I/O	SDA — I ² C serial data input/output.
	8	I/O	P1.4 — Port 1 bit 4.
		I	INT1 — External interrupt 1 input.
	4	I	P1.5 — Port 1 bit 5 (input only).
		I	RST — External Reset input (if selected via FLASH configuration). A LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.
	3	I/O	P1.6 — Port 1 bit 6.
	2	I/O	P1.7 — Port 1 bit 7.

Table 3: Pin description...continued

Symbol	Pin	Type	Description
P3.0 - P3.1	7, 6	I/O	Port 3: Port 3 is an 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
	7	I/O	P3.0 — Port 3 bit 0.
		O	XTAL2 — Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration).
		O	CLKOUT — CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the real time clock/system timer.
	6	I/O	P3.1 — Port 3 bit 1.
		I	XTAL1 — Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, and if XTAL1/XTAL2 are not used to generate the clock for the real time clock/system timer.
V _{SS}	5	I	Ground: 0 V reference.
V _{DD}	15	I	Power Supply: This is the power supply voltage for normal operation as well as Idle and Power Down modes.

[1] Input/Output for P1.0-P1.4, P1.6, P1.7. Input for P1.5.

6. Logic symbol

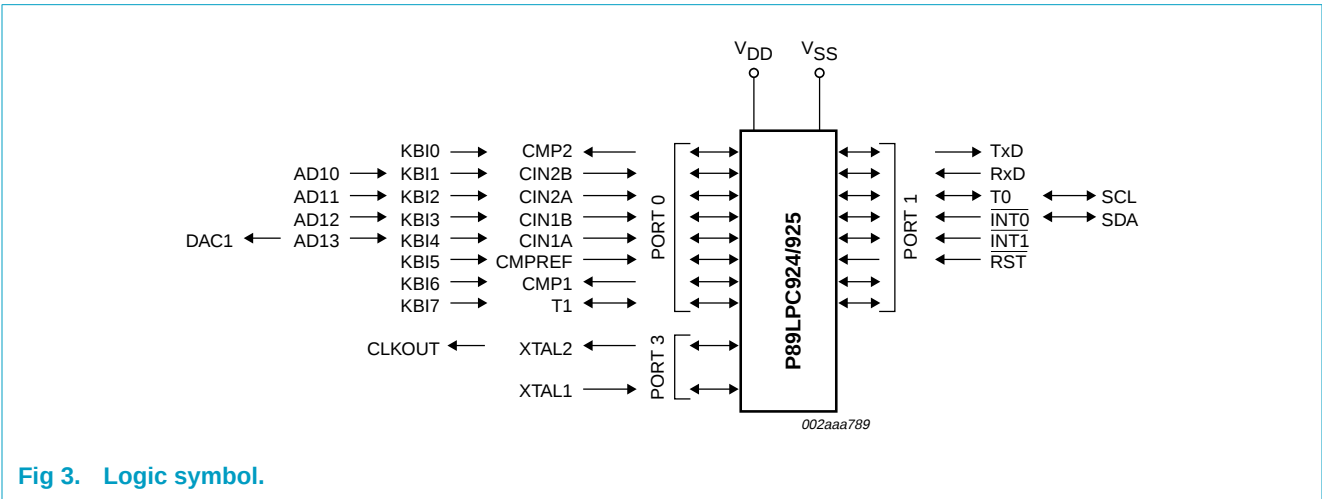


Fig 3. Logic symbol.

8. Functional description

Remark: Please refer to the *P89LPC924/925 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC924/925 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC924/925 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 4) and can also be optionally divided to a slower frequency (see Section 8.7 “CPU Clock (CCLK) modification: DIVM register”).

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.2.2 CPU clock (OSCCLK)

The P89LPC924/925 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.2.3 Low speed oscillator option

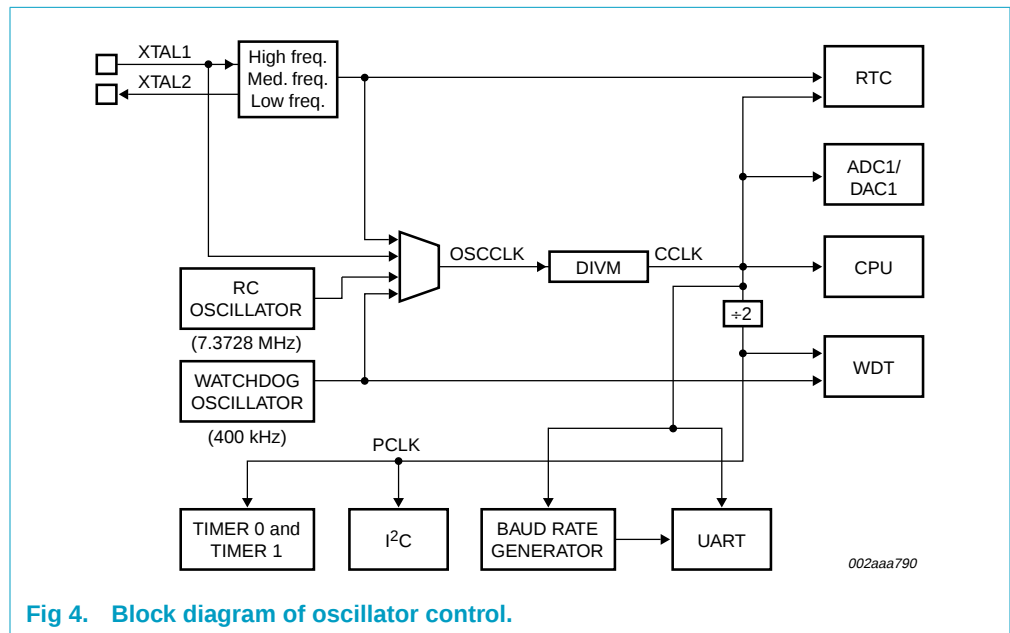
This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.2.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.2.5 High speed oscillator option

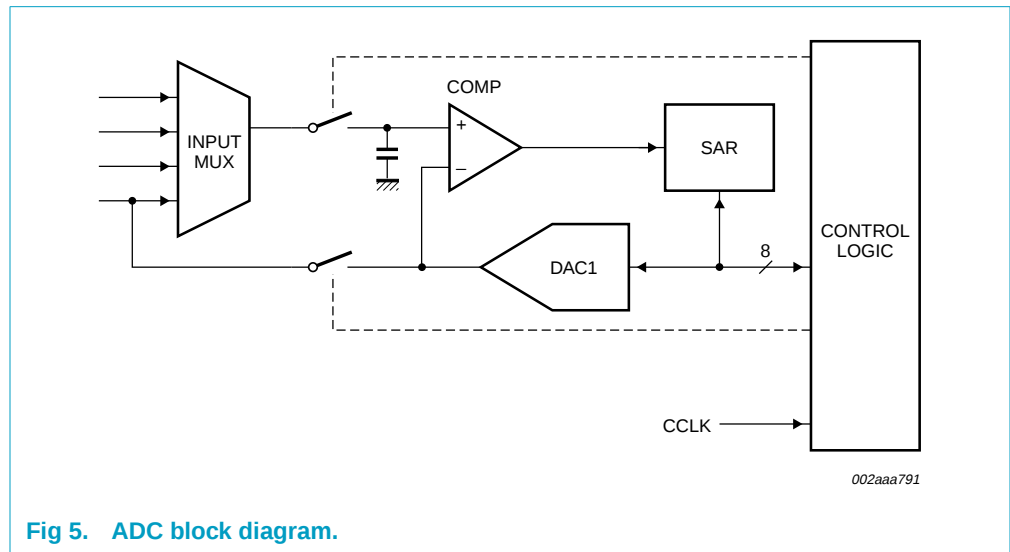
This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below**



8.9 A/D converter

8.9.1 General description

The P89LPC924/925 has an 8-bit, 4-channel multiplexed successive approximation analog-to-digital converter module. A block diagram of the A/D converter is shown in **Figure 5**. The A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the successive approximation register (SAR) drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.



8.9.2 Features

- 8-bit, 4-channel multiplexed input, successive approximation A/D converter.
- Four result registers.
- Six operating modes
 - Fixed channel, single conversion mode
 - Fixed channel, continuous conversion mode
 - Auto scan, single conversion mode
 - Auto scan, continuous conversion mode
 - Dual channel, continuous conversion mode
 - Single step mode
- Three conversion start modes
 - Timer triggered start
 - Start immediately
 - Edge triggered
- 8-bit conversion time of $\geq 3.9 \mu\text{s}$ at an ADC clock of 3.3 MHz
- Interrupt or polled operation
- Boundary limits interrupt
- DAC output to a port pin with high output impedance
- Clock divider
- Power down mode

8.9.3 A/D operating modes

Fixed channel, single conversion mode: A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

Fixed channel, continuous conversion mode: A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

Auto scan, single conversion mode: Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

Auto scan, continuous conversion mode: Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected

8.9.5 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

8.9.6 DAC output to a port pin with high output impedance

The A/D converter's DAC block can be output to a port pin. In this mode, the AD1DAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC, the DAC output will appear on the channel 3 pin.

8.9.7 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.9.8 Power-down and idle mode

In idle mode the A/D converter, if enabled, will continue to function and can cause the device to exit idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total power-down mode, the A/D does not function. If the A/D is enabled, it will consume power. Power can be reduced by disabling the A/D.

8.10 Memory organization

The various P89LPC924/925 memory spaces are as follows:

- DATA
128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the Stack may be in this area.
- IDATA
Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.
- SFR
Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.
- CODE
64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC924/925 has 4 kB/8 kB of on-chip Code memory.

8.13.1 Port configurations

All but three I/O port pins on the P89LPC924/925 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.

P1.2 (SCL/T0) and P1.3 (SDA/ $\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

8.13.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC924/925 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD} , causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic '0'. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD} .

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic '1'. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.6 Port 0 analog functions

The P89LPC924/925 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

8.17.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.17.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.17.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.17.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.17.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.17.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.18 Real-Time clock/system timer

The P89LPC924/925 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all '0's, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

8.19 UART

The P89LPC924/925 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC924/925 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

8.19.1 Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{16}$ of the CPU clock frequency.

8.19.2 Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical '0'), 8 data bits (LSB first), and a stop bit (logical '1'). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in [Section 8.19.5 "Baud rate generator and selection"](#)).

8.19.3 Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logical '0'), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical '1'). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of '0' or '1'. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $\frac{1}{16}$ or $\frac{1}{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

8.19.4 Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical '0'), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical '1'). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in [Section 8.19.5 "Baud rate generator and selection"](#)).

8.19.5 Baud rate generator and selection

The P89LPC924/925 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see [Figure 7](#)). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is set. The independent Baud Rate Generator uses OSCCLK.

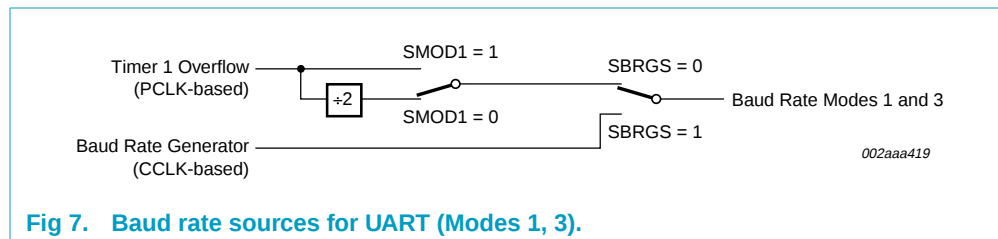


Fig 7. Baud rate sources for UART (Modes 1, 3).

8.20 I²C-bus serial interface

I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multimaster bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 8. The P89LPC924/925 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

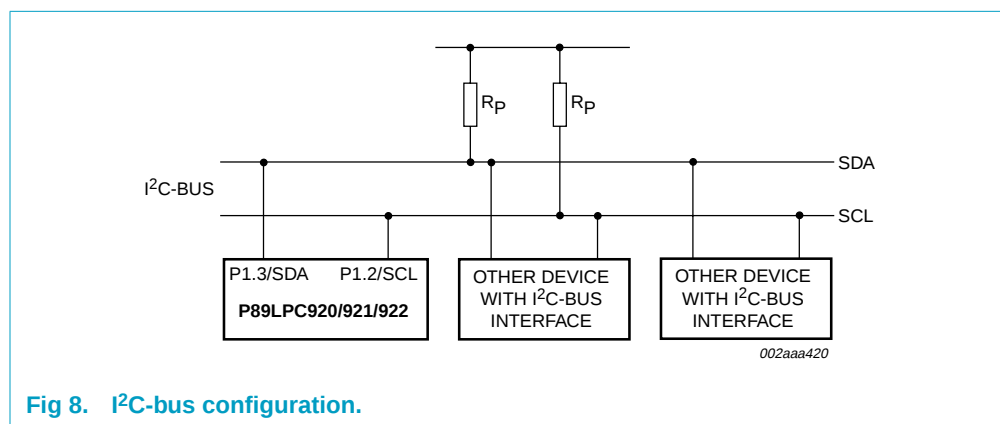


Fig 8. I²C-bus configuration.

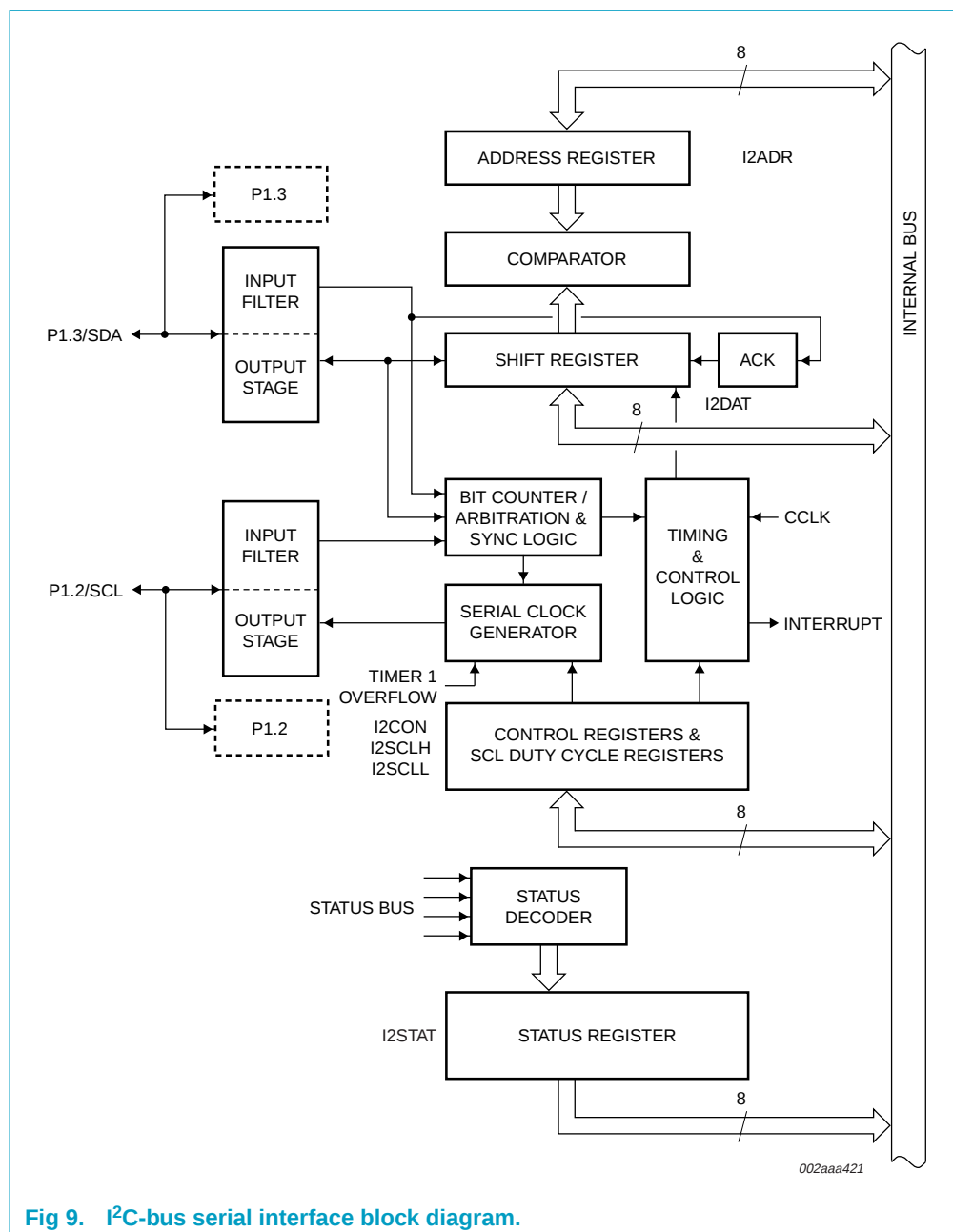


Fig 9. I²C-bus serial interface block diagram.

8.21.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

8.21.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode. If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

8.22 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than 6 CCLKs.

8.25 Flash program memory

8.25.1 General description

The P89LPC924/925 Flash memory provides in-circuit electrical erasure and programming. The Flash can be read, erased, or written as bytes. The Sector and Page Erase functions can erase any Flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. In-System Programming and standard parallel programming are both available. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC924/925 Flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC924/925 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.25.2 Features

- Parallel programming with industry-standard commercial programmers.
- In-Circuit serial Programming (ICP) with industry-standard commercial programmers.
- IAP-Lite allows individual and multiple bytes of code memory to be used for data storage and programmed under control of the end application.
- Internal fixed boot ROM, containing low-level In-Application Programming (IAP) routines that can be called from the end application (in addition to IAP-Lite).
- Default serial loader providing In-System Programming (ISP) via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided Flash loader code to reside anywhere in the Flash memory space, providing flexibility to the user.
- Programming and erase over the full operating voltage range.
- Read/Programming/Erase using ISP/IAP/IAP-Lite.
- Any flash program operation in 2 ms.
- Any flash erase operation in 4 ms.
- Programmable security for the code in the Flash for each sector.
- >100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

8.25.3 ISP and IAP capabilities of the P89LPC924/925

Flash organization: The P89LPC924/925 program memory consists of four/eight 1 kB sectors. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time. An In-Application Programming (IAP) interface is provided to allow the end user's application to erase and reprogram the user code memory. In addition, erasing and reprogramming of user-programmable bytes including UCFG1, the Boot Status Byte and the Boot Vector are supported. As shipped from the factory, the upper 512 bytes of user code space contains a serial In-System Programming (ISP) routine allowing for the device to be programmed in circuit through the serial port.

10. Static characteristics

Table 8: DC electrical characteristics

$V_{DD} = 2.4\text{ V}$ to 3.6 V , unless otherwise specified.

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$I_{DD(oper)}$	power supply current, operating	3.6 V; 12 MHz	[2]	-	9	15 mA
		3.6 V; 18 MHz	[2]	-	14	23 mA
$I_{DD(idle)}$	power supply current, Idle mode	3.6 V; 12 MHz	[2]	-	3.25	5 mA
		3.6 V; 18 MHz	[2]	-	5	7 mA
$I_{DD(PD)}$	power supply current, Power-down mode, voltage comparators powered-down	3.6 V	[2]	-	55	80 μA
$I_{DD(TPD)}$	power supply current, Total Power-down mode	3.6 V	[2]	-	1	5 μA
$(dV_{DD}/dt)_r$	V_{DD} rise rate		-	-	2	mV/ μs
$(dV_{DD}/dt)_f$	V_{DD} fall rate		-	-	50	mV/ μs
V_{POR}	Power-on reset detect voltage		-	-	0.2	V
V_{RAM}	RAM keep-alive voltage		1.5	-	-	V
$V_{th(HL)}$	negative-going threshold voltage	except SCL, SDA	$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only	-0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	positive-going threshold voltage	except SCL, SDA	-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only	$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	Port 1	-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage; all ports, all modes except Hi-Z	$I_{OL} = 20\text{ mA}$	[3]	-	0.6	1.0 V
		$I_{OL} = 3.2\text{ mA}$	[3]	-	0.2	0.3 V
V_{OH}	HIGH-level output voltage, all ports	$I_{OH} = -3.2\text{ mA}$; push-pull mode	$V_{DD} - 0.7$	$V_{DD} - 0.4$	-	V
		$I_{OH} = -20\text{ }\mu\text{A}$; quasi-bidirectional mode	$V_{DD} - 0.3$	$V_{DD} - 0.2$	-	V
C_{ig}	input/output pin capacitance		[4]	-	-	15 pF
I_{IL}	logical 0 input current, all ports	$V_{IN} = 0.4\text{ V}$	[5]	-	-	-80 μA
I_{LI}	input leakage current, all ports	$V_{IN} = V_{IL}$ or V_{IH}	[6]	-	-	$\pm 10\text{ }\mu\text{A}$
I_{TL}	logical 1-to-0 transition current, all ports	$V_{IN} = 2.0\text{ V}$ at $V_{DD} = 3.6\text{ V}$	[7], [8]	-30	-	-450 μA
R_{RST}	internal reset pull-up resistor		10	-	30	k Ω

12. Comparator electrical characteristics

Table 12: Comparator electrical characteristics

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$, unless otherwise specified.

$T_{amb} = -40\text{ °C to }+85\text{ °C}$ for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	offset voltage comparator inputs		-	-	± 20	mV
V_{CR}	common mode range comparator inputs		0	-	$V_{DD} - 0.3$	V
CMRR	common mode rejection ratio	[1]	-	-	-50	dB
	response time		-	250	500	ns
	comparator enable to output valid		-	-	10	μs
I_{IL}	input leakage current, comparator	$0 < V_{IN} < V_{DD}$	-	-	± 10	μA

[1] This parameter is characterized, but not tested in production.

13. A/D converter electrical characteristics

Table 13: A/D converter electrical characteristics

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$, unless otherwise specified.

$T_{amb} = -40\text{ °C to }+85\text{ °C}$ for industrial, unless otherwise specified.

All limits valid for an external source impedance of less than 10 k Ω .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AV_{IN}	analog input voltage		$V_{SS} - 0.2$	-	$V_{SS} + 0.2$	V
C_{IA}	analog input capacitance		-	-	15	pF
D_{NL}	differential non-linearity		-	-	± 1	LSB
I_{NL}	integral non-linearity		-	-	± 1	LSB
OS_e	offset error		-	-	± 2	LSB
G_e	gain error		-	-	± 1	%
T_{ue}	total unadjusted error		-	-	± 2	LSB
M_{CTC}	channel-to-channel matching		-	-	± 1	LSB
$\alpha_{ct(port)}$	crosstalk between port inputs	0 to 100 kHz	-	-	-60	dB
SR_{in}	input slew rate		-	-	100	V/ms
t_{ADC}	conversion time	A/D enabled	-	-	13	ADC clocks

15. Revision history

Table 14: Revision history

Rev	Date	CPCN	Description
03	20041215	-	Product data (9397 750 14471) Modification: • Added 18 MHz information.
02	20040615	-	Product data (9397 750 13459)
01	20040309	-	Objective data (9397 750 12879)