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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f980-gm

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Table 4.14. Comparator Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V, -40 to $+85$ °C unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Response Time: Mode 0, $V_{DD} = 2.4$ V, $V_{CM}^* = 1.2$ V	CP0+ – CP0– = 100 mV	—	120	—	ns
	CP0+ – CP0– = –100 mV	—	110	—	ns
Response Time: Mode 1, $V_{DD} = 2.4$ V, $V_{CM}^* = 1.2$ V	CP0+ – CP0– = 100 mV	—	180	—	ns
	CP0+ – CP0– = –100 mV	—	220	—	ns
Response Time: Mode 2, $V_{DD} = 2.4$ V, $V_{CM}^* = 1.2$ V	CP0+ – CP0– = 100 mV	—	350	—	ns
	CP0+ – CP0– = –100 mV	—	600	—	ns
Response Time: Mode 3, $V_{DD} = 2.4$ V, $V_{CM}^* = 1.2$ V	CP0+ – CP0– = 100 mV	—	1240	—	ns
	CP0+ – CP0– = –100 mV	—	3200	—	ns
Common-Mode Rejection Ratio		—	1.5	—	mV/V
Inverting or Non-Inverting Input Voltage Range		–0.25	—	$V_{DD} + 0.25$	V
Input Capacitance		—	12	—	pF
Input Bias Current		—	1	—	nA
Input Offset Voltage		–7	—	+7	mV
Power Supply					
Power Supply Rejection		—	0.1	—	mV/V
Power-up Time	$V_{DD} = 3.6$ V	—	0.6	—	μ s
	$V_{DD} = 3.0$ V	—	1.0	—	μ s
	$V_{DD} = 2.4$ V	—	1.8	—	μ s
	$V_{DD} = 1.8$ V	—	10	—	μ s
Supply Current at DC	Mode 0	—	23	—	μ A
	Mode 1	—	8.8	—	μ A
	Mode 2	—	2.6	—	μ A
	Mode 3	—	0.4	—	μ A
*Note: V_{cm} is the common-mode voltage on CP0+ and CP0–.					

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SFR Definition 5.3. ADC0AC: ADC0 Accumulator Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD012BE	AD0AE	AD0SJST[2:0]			AD0RPT[2:0]		
Type	R/W	W	R/W			R/W		
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xBA

Bit	Name	Function
7	AD012BE	ADC0 12-Bit Mode Enable. Enables 12-bit Mode on C8051F980/6 and C8051F990/6 devices. 0: 12-bit Mode Disabled. 1: 12-bit Mode Enabled.
6	AD0AE	ADC0 Accumulate Enable. Enables multiple conversions to be accumulated when burst mode is disabled. 0: ADC0H:ADC0L contain the result of the latest conversion when Burst Mode is disabled. 1: ADC0H:ADC0L contain the accumulated conversion results when Burst Mode is disabled. Software must write 0x0000 to ADC0H:ADC0L to clear the accumulated result. This bit is write-only. Always reads 0b.
5:3	AD0SJST[2:0]	ADC0 Accumulator Shift and Justify. Specifies the format of data read from ADC0H:ADC0L. 000: Right justified. No shifting applied. 001: Right justified. Shifted right by 1 bit. 010: Right justified. Shifted right by 2 bits. 011: Right justified. Shifted right by 3 bits. 100: Left justified. No shifting applied. All remaining bit combinations are reserved.
2:0	AD0RPT[2:0]	ADC0 Repeat Count. Selects the number of conversions to perform and accumulate in Burst Mode. This bit field must be set to 000 if Burst Mode is disabled. 000: Perform and Accumulate 1 conversion. 001: Perform and Accumulate 4 conversions. 010: Perform and Accumulate 8 conversions. 011: Perform and Accumulate 16 conversions. 100: Perform and Accumulate 32 conversions. 101: Perform and Accumulate 64 conversions. All remaining bit combinations are reserved.

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5.6.1. Window Detector In Single-Ended Mode

Figure 5.5 shows two example window comparisons for right-justified data, with $ADC0LTH:ADC0LTL = 0x0080$ (128d) and $ADC0GTH:ADC0GTL = 0x0040$ (64d). The input voltage can range from 0 to $VREF \times (1023/1024)$ with respect to GND, and is represented by a 10-bit unsigned integer value. In the left example, an $AD0WINT$ interrupt will be generated if the $ADC0$ conversion word ($ADC0H:ADC0L$) is within the range defined by $ADC0GTH:ADC0GTL$ and $ADC0LTH:ADC0LTL$ (if $0x0040 < ADC0H:ADC0L < 0x0080$). In the right example, an $AD0WINT$ interrupt will be generated if the $ADC0$ conversion word is outside of the range defined by the $ADC0GT$ and $ADC0LT$ registers (if $ADC0H:ADC0L < 0x0040$ or $ADC0H:ADC0L > 0x0080$). Figure 5.6 shows an example using left-justified data with the same comparison values.

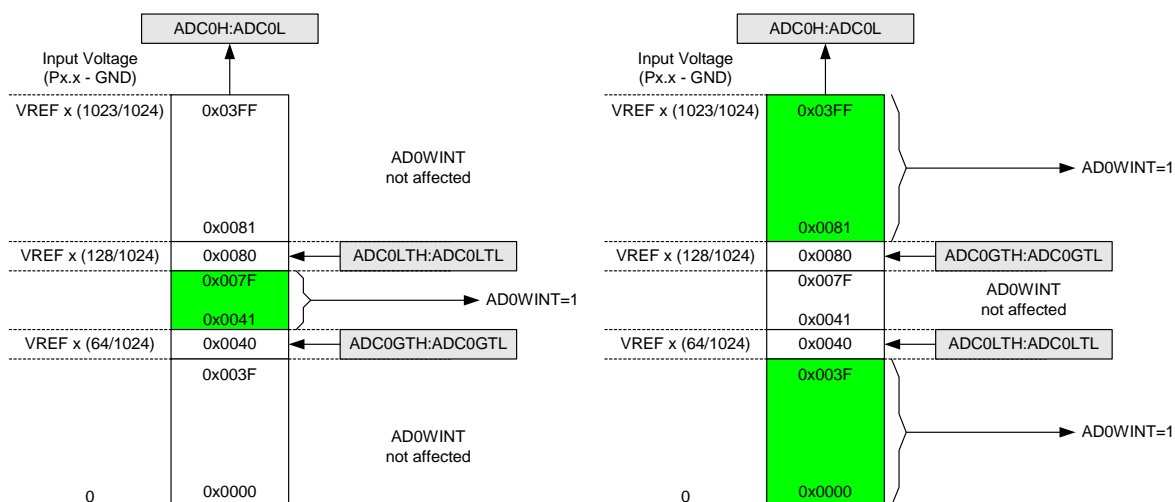


Figure 5.5. ADC Window Compare Example: Right-Justified Single-Ended Data

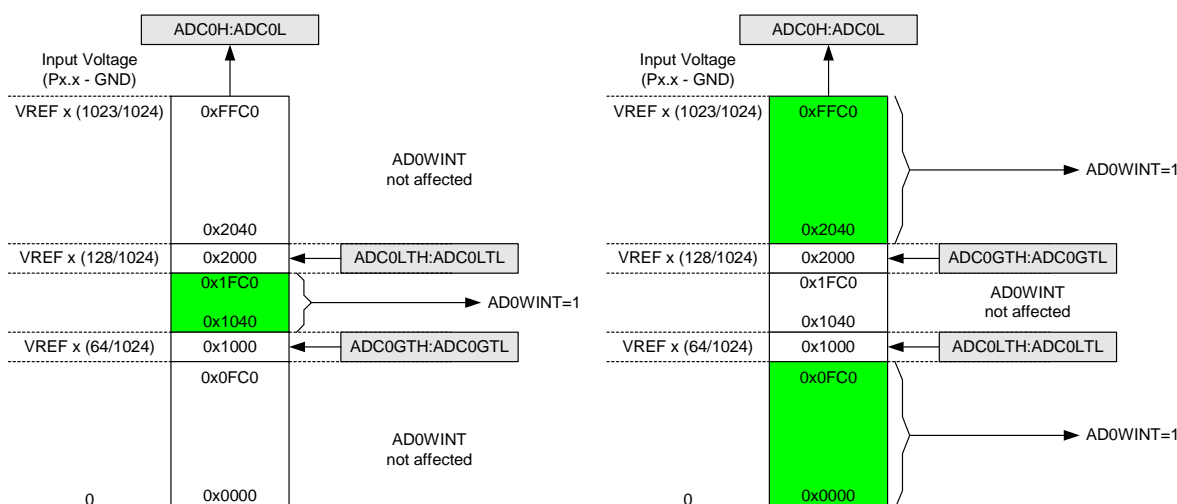


Figure 5.6. ADC Window Compare Example: Left-Justified Single-Ended Data

5.6.2. ADC0 Specifications

See "4. Electrical Characteristics" on page 48 for a detailed listing of ADC0 specifications.

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5.7. ADC0 Analog Multiplexer

ADC0 on C8051F99x-C8051F98x has an analog multiplexer, referred to as AMUX0.

AMUX0 selects the positive inputs to the single-ended ADC0. Any of the following may be selected as the positive input: Port I/O pins, the on-chip temperature sensor, Regulated Digital Supply Voltage (Output of VREG0), VDD Supply, or the positive input may be connected to GND. The ADC0 input channels are selected in the ADC0MX register described in SFR Definition 5.12.

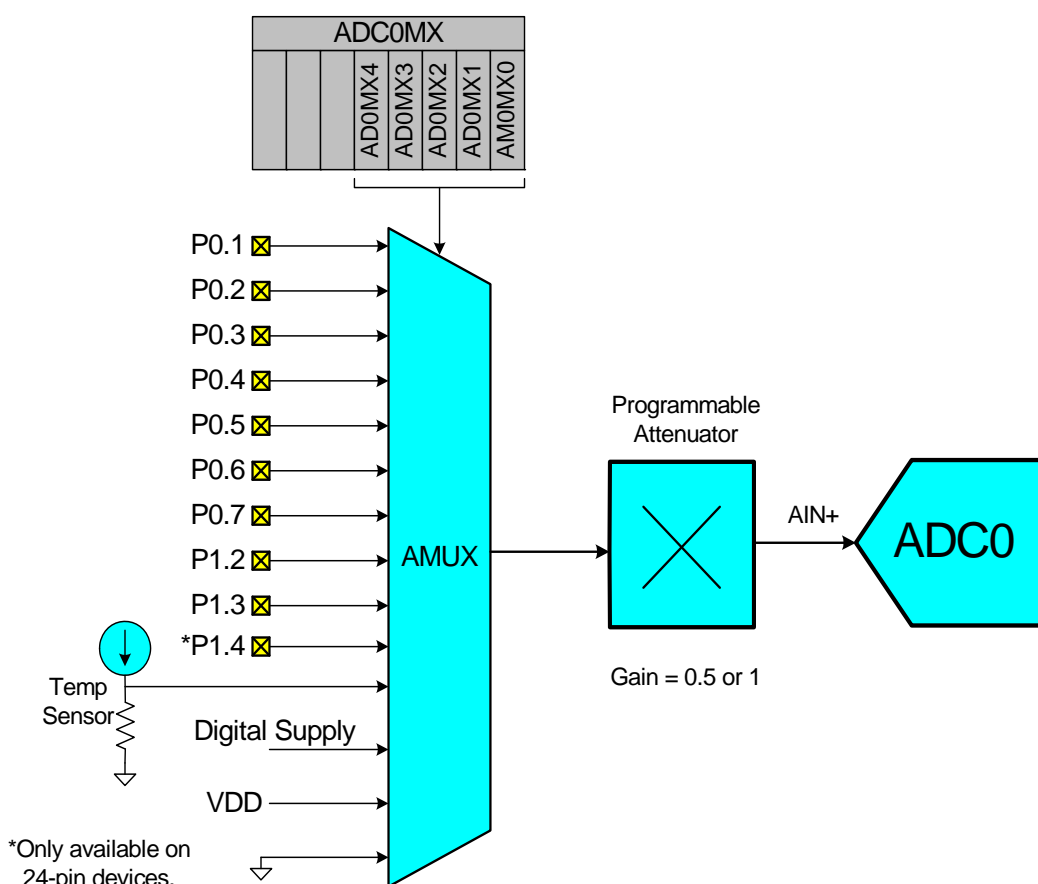


Figure 5.7. ADC0 Multiplexer Block Diagram

Important Note About ADC0 Input Configuration: Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN and disable the digital driver (PnMDOUT = 0 and Port Latch = 1). To force the Crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP. See Section “21. Port Input/Output” on page 215 for more Port I/O configuration details.

SFR Definition 7.3. CPT0MX: Comparator0 Input Channel Select

Bit	7	6	5	4	3	2	1	0
Name	CMX0N[3:0]				CMX0P[3:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	1	0	0

SFR Page = 0x0; SFR Address = 0x9F

Bit	Name	Function																																
7:4	CMX0N	Comparator0 Negative Input Selection. Selects the negative input channel for Comparator0. <table><tr><td>0000:</td><td>Reserved</td><td>1000:</td><td>Reserved</td></tr><tr><td>0001:</td><td>Reserved</td><td>1001:</td><td>Reserved</td></tr><tr><td>0010:</td><td>Reserved</td><td>1010:</td><td>Reserved</td></tr><tr><td>0011:</td><td>Reserved</td><td>1011:</td><td>Reserved</td></tr><tr><td>0100:</td><td>P1.1</td><td>1100:</td><td>Capacitive Touch Sense Compare</td></tr><tr><td>0101:</td><td>Reserved</td><td>1101:</td><td>VDD divided by 2</td></tr><tr><td>0110:</td><td>Reserved</td><td>1110:</td><td>Digital Supply Voltage</td></tr><tr><td>0111:</td><td>Reserved</td><td>1111:</td><td>Ground</td></tr></table>	0000:	Reserved	1000:	Reserved	0001:	Reserved	1001:	Reserved	0010:	Reserved	1010:	Reserved	0011:	Reserved	1011:	Reserved	0100:	P1.1	1100:	Capacitive Touch Sense Compare	0101:	Reserved	1101:	VDD divided by 2	0110:	Reserved	1110:	Digital Supply Voltage	0111:	Reserved	1111:	Ground
0000:	Reserved	1000:	Reserved																															
0001:	Reserved	1001:	Reserved																															
0010:	Reserved	1010:	Reserved																															
0011:	Reserved	1011:	Reserved																															
0100:	P1.1	1100:	Capacitive Touch Sense Compare																															
0101:	Reserved	1101:	VDD divided by 2																															
0110:	Reserved	1110:	Digital Supply Voltage																															
0111:	Reserved	1111:	Ground																															
3:0	CMX0P	Comparator0 Positive Input Selection. Selects the positive input channel for Comparator0. <table><tr><td>0000:</td><td>Reserved</td><td>1000:</td><td>Reserved</td></tr><tr><td>0001:</td><td>Reserved</td><td>1001:</td><td>Reserved</td></tr><tr><td>0010:</td><td>Reserved</td><td>1010:</td><td>Reserved</td></tr><tr><td>0011:</td><td>Reserved</td><td>1011:</td><td>Reserved</td></tr><tr><td>0100:</td><td>P1.0</td><td>1100:</td><td>Capacitive Touch Sense Compare</td></tr><tr><td>0101:</td><td>Reserved</td><td>1101:</td><td>VDD divided by 2</td></tr><tr><td>0110:</td><td>Reserved</td><td>1110:</td><td>VDD Supply Voltage</td></tr><tr><td>0111:</td><td>Reserved</td><td>1111:</td><td>VDD Supply Voltage</td></tr></table>	0000:	Reserved	1000:	Reserved	0001:	Reserved	1001:	Reserved	0010:	Reserved	1010:	Reserved	0011:	Reserved	1011:	Reserved	0100:	P1.0	1100:	Capacitive Touch Sense Compare	0101:	Reserved	1101:	VDD divided by 2	0110:	Reserved	1110:	VDD Supply Voltage	0111:	Reserved	1111:	VDD Supply Voltage
0000:	Reserved	1000:	Reserved																															
0001:	Reserved	1001:	Reserved																															
0010:	Reserved	1010:	Reserved																															
0011:	Reserved	1011:	Reserved																															
0100:	P1.0	1100:	Capacitive Touch Sense Compare																															
0101:	Reserved	1101:	VDD divided by 2																															
0110:	Reserved	1110:	VDD Supply Voltage																															
0111:	Reserved	1111:	VDD Supply Voltage																															

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Table 9.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/3
JNC rel	Jump if Carry is not set	2	2/3
JB bit, rel	Jump if direct bit is set	3	3/4
JNB bit, rel	Jump if direct bit is not set	3	3/4
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/4
Program Branching			
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

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SFR Definition 14.4. FLKEY: Flash Lock and Key

Bit	7	6	5	4	3	2	1	0
Name	FLKEY[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0xB7

Bit	Name	Function
7:0	FLKEY[7:0]	<p>Flash Lock and Key Register.</p> <p>Write:</p> <p>This register provides a lock and key function for Flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is complete. If any writes to FLKEY are performed incorrectly, or if a Flash write or erase operation is attempted while these operations are disabled, the Flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to Flash, it can intentionally lock the Flash by writing a non-0xA5 value to FLKEY from software.</p> <p>Read:</p> <p>When read, bits 1–0 indicate the current Flash lock state.</p> <p>00: Flash is write/erase locked.</p> <p>01: The first key code has been written (0xA5).</p> <p>10: Flash is unlocked (writes/erases allowed).</p> <p>11: Flash writes/erases disabled until the next reset.</p>

19. Clocking Sources

C8051F99x-C8051F98x devices include a programmable precision internal oscillator, an external oscillator drive circuit, a low power internal oscillator, and a SmartClock real time clock oscillator. The precision internal oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 19.1. The external oscillator can be configured using the OSCXCN register. The low power internal oscillator is automatically enabled and disabled when selected and deselected as a clock source. SmartClock operation is described in the SmartClock oscillator chapter.

The system clock (SYSCLK) can be derived from the precision internal oscillator, external oscillator, low power internal oscillator, low power internal oscillator divided by 8, or SmartClock oscillator. The global clock divider can generate a system clock that is 1, 2, 4, 8, 16, 32, 64, or 128 times slower than the selected input clock source. Oscillator electrical specifications can be found in the Electrical Specifications Chapter.

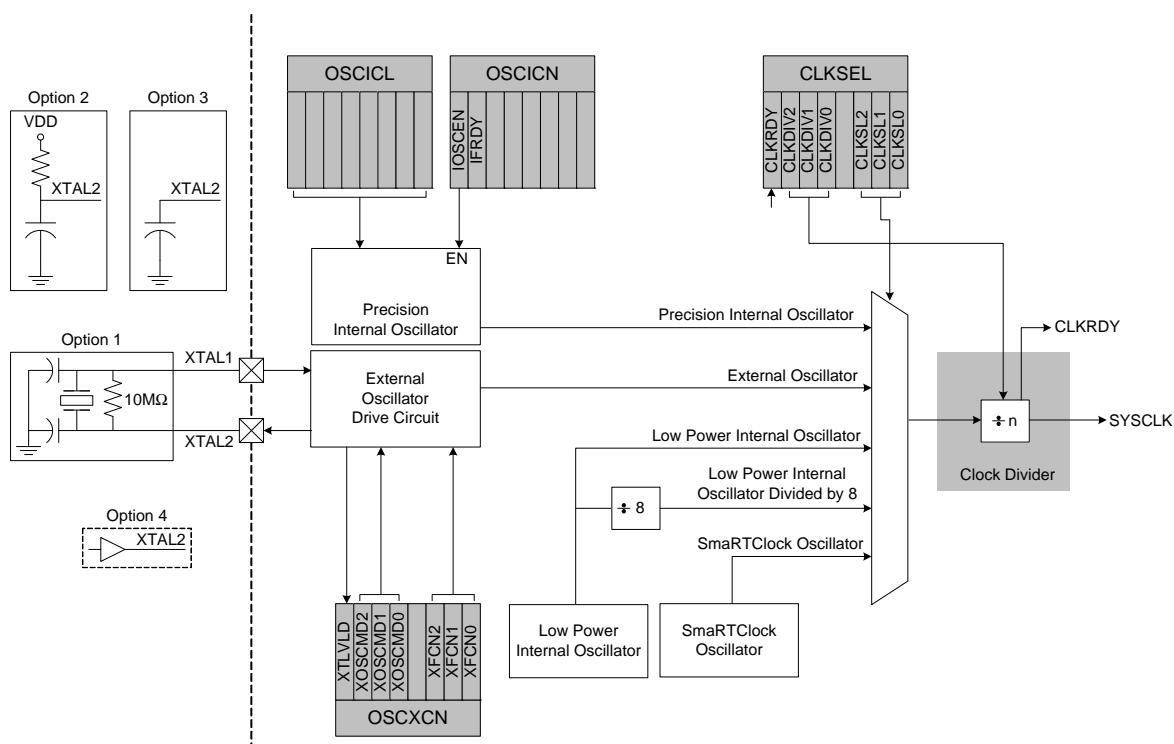


Figure 19.1. Clocking Sources Block Diagram

The proper way of changing the system clock when both the clock source and the clock divide value are being changed is as follows:

If switching from a fast “undivided” clock to a slower “undivided” clock:

1. Change the clock divide value.
2. Poll for CLKRDY > 1.
3. Change the clock source.

If switching from a slow “undivided” clock to a faster “undivided” clock:

1. Change the clock source.
2. Change the clock divide value.
3. Poll for CLKRDY > 1.

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SFR Definition 19.4. OSCXCN: External Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	XCLKVLD	XOSCMD[2:0]			Reserved	XFCN[2:0]		
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xB1

Bit	Name	Function
7	XCLKVLD	External Oscillator Valid Flag. Provides External Oscillator status and is valid at all times for all modes of operation except External CMOS Clock Mode and External CMOS Clock Mode with divide by 2. In these modes, XCLKVLD always returns 0. 0: External Oscillator is unused or not yet stable. 1: External Oscillator is running and stable.
6:4	XOSCMD	External Oscillator Mode Bits. Configures the external oscillator circuit to the selected mode. 00x: External Oscillator circuit disabled. 010: External CMOS Clock Mode. 011: External CMOS Clock Mode with divide by 2 stage. 100: RC Oscillator Mode. 101: Capacitor Oscillator Mode. 110: Crystal Oscillator Mode. 111: Crystal Oscillator Mode with divide by 2 stage.
3	Reserved	Read = 0b. Must Write 0b.
2:0	XFCN	External Oscillator Frequency Control Bits. Controls the external oscillator bias current. 000-111: See Table 19.1 on page 190 (Crystal Mode) or Table 19.2 on page 191 (RC or C Mode) for recommended settings.

21.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the Crossbar for pin assignment; however, some digital functions bypass the Crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in PnSKIP set to 1.** Table 21.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

Table 21.2. Port I/O Assignment for Digital Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
UART0, SPI0, SMBus, CP0 Outputs, System Clock Output, PCA0, Timer0 and Timer1 External Inputs.	Any Port pin available for assignment by the Crossbar. This includes P0.0–P1.7 pins which have their PnSKIP bit set to 0. Note: The Crossbar will always assign UART0 and SPI1 pins to fixed locations.	XBR0, XBR1, XBR2
Any pin used for GPIO	P0.0–P1.7, P2.7	P0SKIP, P1SKIP

21.2.3. Assigning Port I/O Pins to External Digital Event Capture Functions

External digital event capture functions can be used to trigger an interrupt or wake the device from a low power mode when a transition occurs on a digital I/O pin. The digital event capture functions do not require dedicated pins and will function on both GPIO pins (PnSKIP = 1) and pins in use by the Crossbar (PnSKIP = 0). External digital event capture functions cannot be used on pins configured for analog I/O. Table 21.3 shows all available external digital event capture functions.

Table 21.3. Port I/O Assignment for External Digital Event Capture Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
External Interrupt 0	P0.0–P0.7	IT01CF
External Interrupt 1	P0.0–P0.7	IT01CF
Port Match	P0.0–P1.7	P0MASK, P0MAT P1MASK, P1MAT

SFR Definition 21.8. P0: Port0

Bit	7	6	5	4	3	2	1	0
Name	P0[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = All; SFR Address = 0x80; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P0[7:0]	Port 0 Data. Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P0.n Port pin is logic LOW. 1: P0.n Port pin is logic HIGH.

SFR Definition 21.9. P0SKIP: Port0 Skip

Bit	7	6	5	4	3	2	1	0
Name	P0SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0xD4

Bit	Name	Function
7:0	P0SKIP[7:0]	Port 0 Crossbar Skip Enable Bits. These bits select Port 0 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P0.n pin is not skipped by the Crossbar. 1: Corresponding P0.n pin is skipped by the Crossbar.

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SFR Definition 21.13. P1: Port1

Bit	7	6	5	4	3	2	1	0
Name	P1[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = All; SFR Address = 0x90; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P1[6:0]	Port 1 Data. Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P1.n Port pin is logic LOW. 1: P1.n Port pin is logic HIGH.

SFR Definition 21.14. P1SKIP: Port1 Skip

Bit	7	6	5	4	3	2	1	0
Name	P1SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xD5

Bit	Name	Function
7:0	P1SKIP[6:0]	Port 1 Crossbar Skip Enable Bits. These bits select Port 1 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P1.n pin is not skipped by the Crossbar. 1: Corresponding P1.n pin is skipped by the Crossbar.

SFR Definition 23.1. SCON0: Serial Port 0 Control

Bit	7	6	5	4	3	2	1	0
Name	S0MODE		MCE0	REN0	TB80	RB80	TI0	RI0
Type	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x98; Bit-Addressable

Bit	Name	Function
7	S0MODE	Serial Port 0 Operation Mode. Selects the UART0 Operation Mode. 0: 8-bit UART with Variable Baud Rate. 1: 9-bit UART with Variable Baud Rate.
6	Unused	Read = 1b. Write = Don't Care.
5	MCE0	Multiprocessor Communication Enable. For Mode 0 (8-bit UART): Checks for valid stop bit. 0: Logic level of stop bit is ignored. 1: RI0 will only be activated if stop bit is logic level 1. For Mode 1 (9-bit UART): Multiprocessor Communications Enable. 0: Logic level of ninth bit is ignored. 1: RI0 is set and an interrupt is generated only when the ninth bit is logic 1.
4	REN0	Receive Enable. 0: UART0 reception disabled. 1: UART0 reception enabled.
3	TB80	Ninth Transmission Bit. The logic level of this bit will be sent as the ninth transmission bit in 9-bit UART Mode (Mode 1). Unused in 8-bit mode (Mode 0).
2	RB80	Ninth Receive Bit. RB80 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.
1	TI0	Transmit Interrupt Flag. Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.
0	RI0	Receive Interrupt Flag. Set to 1 by hardware when a byte of data has been received by UART0 (set at the STOP bit sampling time). When the UART0 interrupt is enabled, setting this bit to 1 causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

24. Enhanced Serial Peripheral Interface (SPI0)

The Enhanced Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

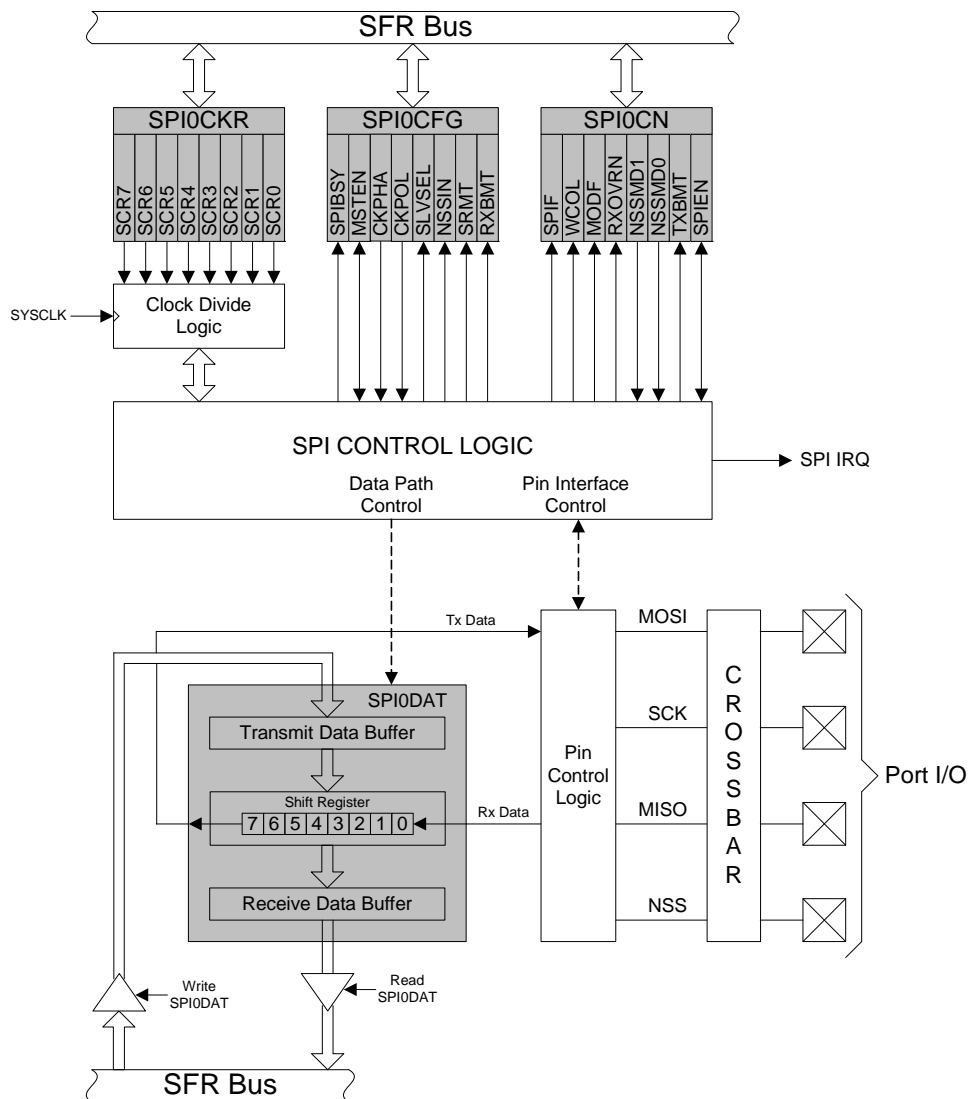
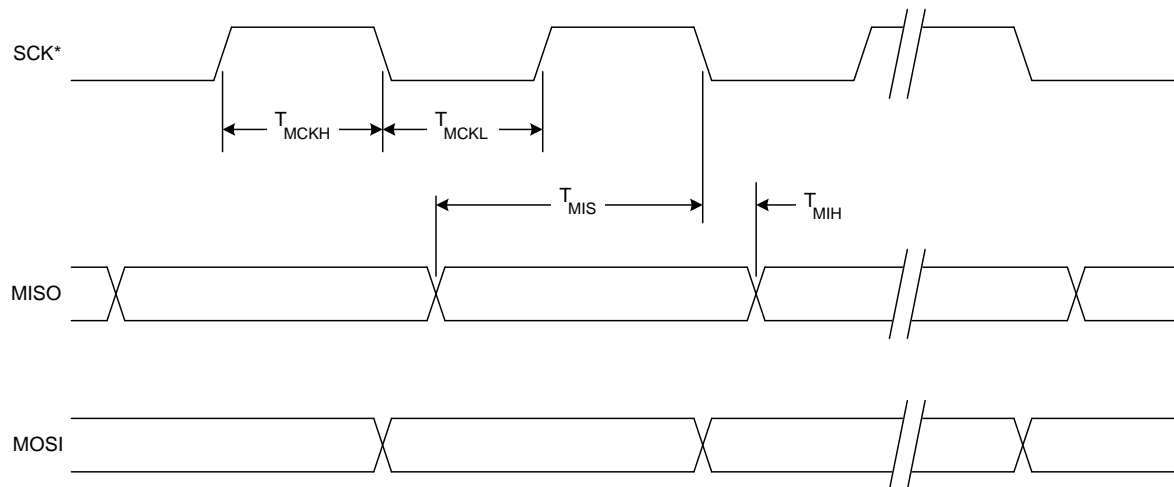
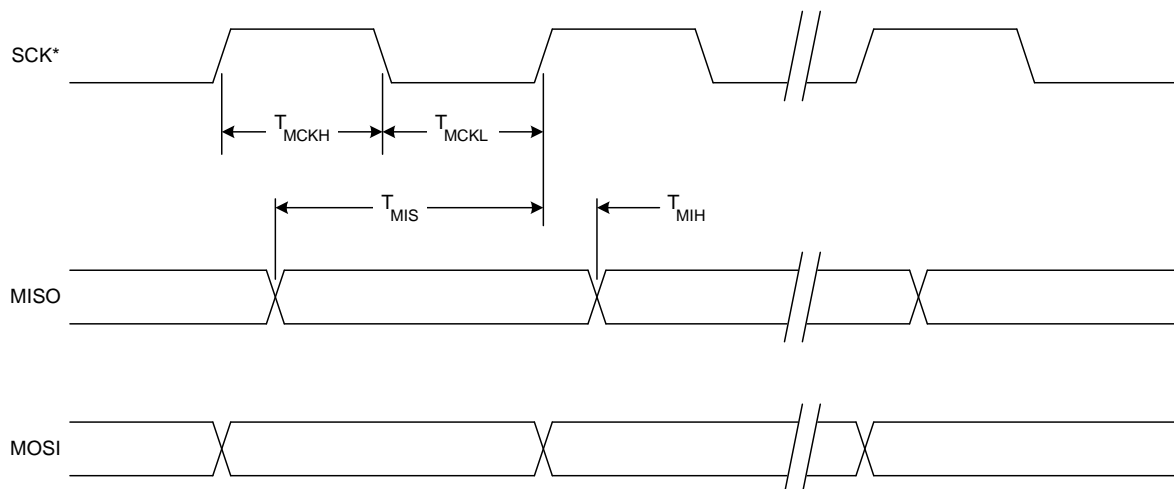


Figure 24.1. SPI Block Diagram



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 24.8. SPI Master Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 24.9. SPI Master Timing (CKPHA = 1)

25.3.3. SmarTClock/External Oscillator Capture Mode

The Capture Mode in Timer 3 allows either SmarTClock or the external oscillator period to be measured against the system clock or the system clock divided by 12. SmarTClock and the external oscillator period can also be compared against each other.

Setting TF3CEN to 1 enables the SmarTClock/External Oscillator Capture Mode for Timer 3. In this mode, T3SPLIT should be set to 0, as the full 16-bit timer is used.

When Capture Mode is enabled, a capture event will be generated either every SmarTClock rising edge or every 8 external clock cycles, depending on the T3XCLK1 setting. When the capture event occurs, the contents of Timer 3 (TMR3H:TMR3L) are loaded into the Timer 3 reload registers (TMR3RLH:TMR3RLL) and the TF3H flag is set (triggering an interrupt if Timer 3 interrupts are enabled). By recording the difference between two successive timer capture values, the SmarTClock or external clock period can be determined with respect to the Timer 3 clock. The Timer 3 clock should be much faster than the capture clock to achieve an accurate reading.

For example, if T3ML = 1b, T3XCLK1 = 0b, and TF3CEN = 1b, Timer 3 will clock every SYSCLK and capture every SmarTClock rising edge. If SYSCLK is 24.5 MHz and the difference between two successive captures is 350 counts, then the SmarTClock period is as follows:

$$350 \times (1 / 24.5 \text{ MHz}) = 14.2 \mu\text{s}.$$

This mode allows software to determine the exact frequency of the external oscillator in C and RC mode or the time between consecutive SmarTClock rising edges, which is useful for determining the SmarTClock frequency.

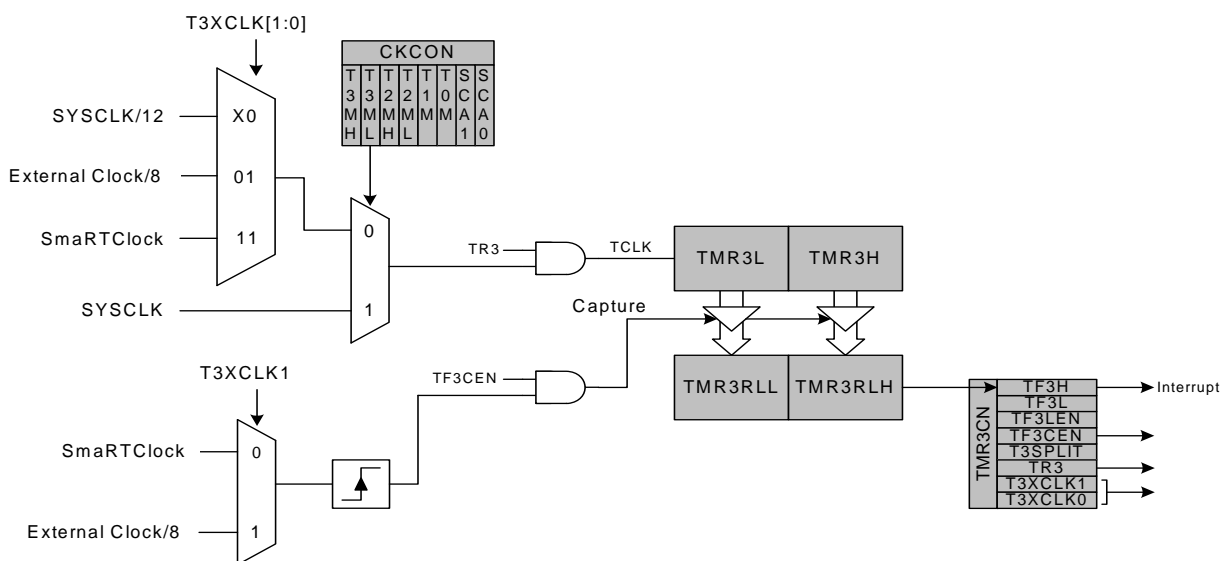


Figure 25.9. Timer 3 Capture Mode Block Diagram

C8051F99x-C8051F98x

SFR Definition 25.14. TMR3RLL: Timer 3 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x92

Bit	Name	Function
7:0	TMR3RLL[7:0]	Timer 3 Reload Register Low Byte. TMR3RLL holds the low byte of the reload value for Timer 3.

SFR Definition 25.15. TMR3RLH: Timer 3 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x93

Bit	Name	Function
7:0	TMR3RLH[7:0]	Timer 3 Reload Register High Byte. TMR3RLH holds the high byte of the reload value for Timer 3.

26.2. PCA0 Interrupt Sources

Figure 26.3 shows a diagram of the PCA interrupt tree. There are five independent event flags that can be used to generate a PCA0 interrupt. They are: the main PCA counter overflow flag (CF), which is set upon a 16-bit overflow of the PCA0 counter, an intermediate overflow flag (COVF), which can be set on an overflow from the 8th, 9th, 10th, or 11th bit of the PCA0 counter, and the individual flags for each PCA channel (CCF0, CCF1, and CCF2), which are set according to the operation mode of that module. These event flags are always set when the trigger condition occurs. Each of these flags can be individually selected to generate a PCA0 interrupt, using the corresponding interrupt enable flag (ECF for CF, ECOV for COVF, and ECCFn for each CCFn). PCA0 interrupts must be globally enabled before any individual interrupt sources are recognized by the processor. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1.

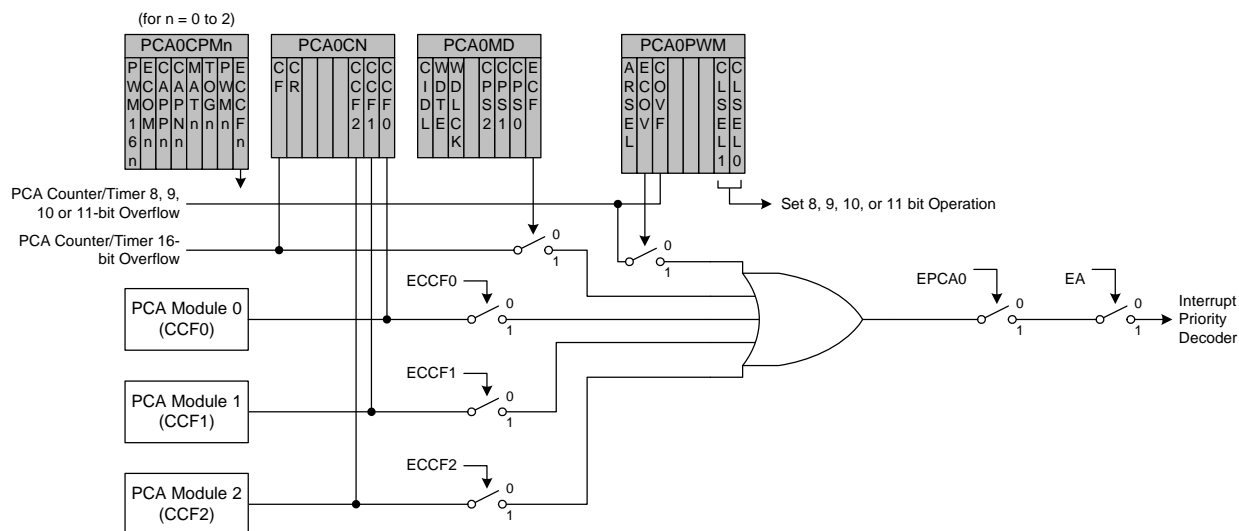


Figure 26.3. PCA Interrupt Block Diagram

C8051F99x-C8051F98x

SFR Definition 26.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	WDTE	WDLCK		CPS2	CPS1	CPS0	ECF
Type	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xD9

Bit	Name	Function
7	CIDL	PCA Counter/Timer Idle Control. Specifies PCA behavior when CPU is in Idle Mode. 0: PCA continues to function normally while the system controller is in Idle Mode. 1: PCA operation is suspended while the system controller is in Idle Mode.
6	WDTE	Watchdog Timer Enable. If this bit is set, PCA Module 2 is used as the watchdog timer. 0: Watchdog Timer disabled. 1: PCA Module 2 enabled as Watchdog Timer.
5	WDLCK	Watchdog Timer Lock. This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset. 0: Watchdog Timer Enable unlocked. 1: Watchdog Timer Enable locked.
4	Unused	Read = 0b, Write = don't care.
3:1	CPS[2:0]	PCA Counter/Timer Pulse Select. These bits select the timebase source for the PCA counter 000: System clock divided by 12 001: System clock divided by 4 010: Timer 0 overflow 011: High-to-low transitions on ECI (max rate = system clock divided by 4) 100: System clock 101: External clock divided by 8 (synchronized with the system clock) 110: SmarTClock divided by 8 (synchronized with the system clock) 111: Reserved
0	ECF	PCA Counter/Timer Overflow Interrupt Enable. This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.
Note: When the WDTE bit is set to 1, the other bits in the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.		