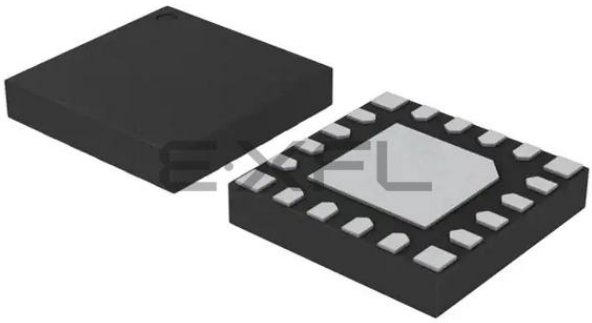

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f981-c-gm

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Table 3.3. PCB Land Pattern

Dimension	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 REF	
GD	2.10	—
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

SFR Definition 5.1. ADC0CN: ADC0 Control

Bit	7	6	5	4	3	2	1	0
Name	AD0EN	BURSTEN	AD0INT	AD0BUSY	AD0WINT	ADC0CM[2:0]		
Type	R/W	R/W	R/W	W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xE8; bit-addressable;

Bit	Name	Function
7	AD0EN	**ADC0 Enable.** 0: ADC0 Disabled (low-power shutdown). 1: ADC0 Enabled (active and ready for data conversions).
6	BURSTEN	**ADC0 Burst Mode Enable.** 0: ADC0 Burst Mode Disabled. 1: ADC0 Burst Mode Enabled.
5	AD0INT	**ADC0 Conversion Complete Interrupt Flag.** Set by hardware upon completion of a data conversion (BURSTEN=0), or a burst of conversions (BURSTEN=1). Can trigger an interrupt. Must be cleared by software.
4	AD0BUSY	**ADC0 Busy.** Writing 1 to this bit initiates an ADC conversion when ADC0CM[2:0] = 000.
3	AD0WINT	**ADC0 Window Compare Interrupt Flag.** Set by hardware when the contents of ADC0H:ADC0L fall within the window specified by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL. Can trigger an interrupt. Must be cleared by software.
2:0	ADC0CM[2:0]	**ADC0 Start of Conversion Mode Select.** Specifies the ADC0 start of conversion source. 000: ADC0 conversion initiated on write of 1 to AD0BUSY. 001: ADC0 conversion initiated on overflow of Timer 0. 010: ADC0 conversion initiated on overflow of Timer 2. 011: ADC0 conversion initiated on overflow of Timer 3. 1xx: ADC0 conversion initiated on rising edge of CNVSTR.

SFR Definition 5.12. ADC0MX: ADC0 Input Channel Select

Bit	7	6	5	4	3	2	1	0
Name				AD0MX				
Type	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	1

SFR Page = 0x0; SFR Address = 0x96

Bit	Name	Function
7:5	Unused	Read = 000b; Write = Don't Care.
4:0	AD0MX	**AMUX0 Positive Input Selection.** Selects the positive input channel for ADC0. 00000: Reserved. 00001: P0.1 00010: P0.2 00011: P0.3 00100: P0.4 00101: P0.5 00110: P0.6 00111: P0.7 01000: Reserved. 01001: Reserved. 01010: P1.2 01011: P1.3 01100: P1.4 (only available on 24-pin devices) 01101: Reserved. 01110: Reserved. 01111: Reserved. 10000: Reserved. 10001: Reserved. 10010: Reserved. 10011: Reserved. 10100: Reserved. 10101: Reserved. 10110: Reserved. 10111: Reserved. 11000: Reserved. 11001: Reserved. 11010: Reserved. 11011: Temperature Sensor 11100: V_{DD} Supply Voltage 11101: Digital Supply Voltage (VREG0 Output, 1.7 V Typical) 11110: V_{DD} Supply Voltage 11111: Ground

SFR Definition 6.2. IREF0CF: Current Reference Configuration

Bit	7	6	5	4	3	2	1	0
Name	PWMEN					PWMSS[2:0]		
Type	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0xB9

Bit	Name	Function
7	PWMEN	**PWM Enhanced Mode Enable.** Enables the PWM Enhanced Mode. 0: PWM Enhanced Mode disabled. 1: PWM Enhanced Mode enabled.
6:3	Unused	Read = 0000b, Write = don't care.
2:0	PWMSS[2:0]	**PWM Source Select.** Selects the PCA channel to use for the fine-tuning control signal. 000: CEX0 selected as fine-tuning control signal. 001: CEX1 selected as fine-tuning control signal. 010: CEX2 selected as fine-tuning control signal. All Other Values: Reserved.

6.2. IREF0 Specifications

See Table 4.13 on page 62 for a detailed listing of IREF0 specifications.

8.14. Capacitive Sense Multiplexer

The input multiplexer can be controlled through two methods. The CS0MX register can be written to through firmware, or the register can be configured automatically using the modules auto-scan functionality (see “8.8. Automatic Scanning (Method 1—CS0SMEN = 0)”).

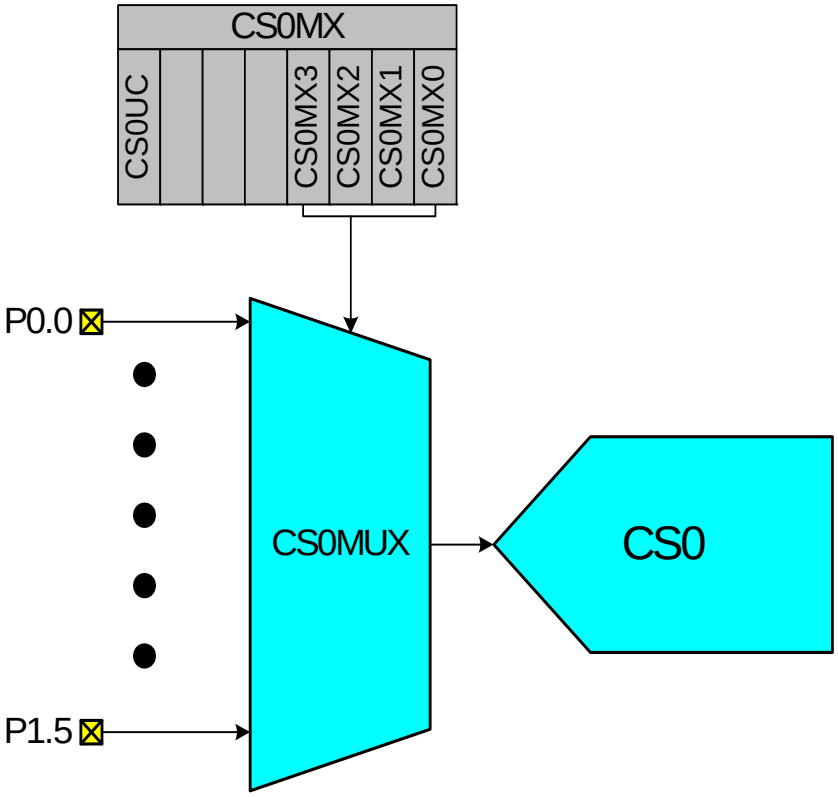

Figure 8.3. CS0 Multiplexer Block Diagram

12.1. SFR Paging

To accommodate more than 128 SFRs in the 0x80 to 0xFF address space, SFR paging has been implemented. By default, all SFR accesses target SFR Page 0x0 to allow access to the registers listed in Table 12.1. During device initialization, some SFRs located on SFR Page 0xF may need to be accessed. Table 12.2 lists the SFRs accessible from SFR Page 0x0F. Some SFRs are accessible from both pages, including the SFRPAGE register. SFRs only accessible from Page 0xF are in **bold**.

The following procedure should be used when accessing SFRs on Page 0xF:

1. Save the current interrupt state (EA_save = EA).
2. Disable Interrupts (EA = 0).
3. Set SFRPAGE = 0xF.
4. Access the SFRs located on SFR Page 0xF.
5. Set SFRPAGE = 0x0.
6. Restore interrupt state (EA = EA_save).

Table 12.2. Special Function Register (SFR) Memory Map (Page 0xF)

F8								
F0	B			**CS0MD3**			EIP1	EIP2
E8								
E0	ACC		**REVID**	**DEVICEID**		FLWR	EIE1	EIE2
D8							**CS0PM**	
D0	PSW							
C8								
C0								
B8		**IREF0CF**		ADC0PWR	ADC0TK			
B0						**PMU0MD**		
A8	IE	CLKSEL						
A0	P2							SFRPAGE
98		**P0DRV**	CRC0CNT	**P1DRV**	CRC0FLIP	**P2DRV**	CRC0AUTO	
90	P1							
88						**TOFFL**	**TOFFH**	
80	P0	SP	DPL	DPH	CRC0CN	CRC0IN	CRC0DAT	PCON
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

(bit addressable)

Table 12.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page
CS0DH	0xEE	0x0	CS0 Data High Byte	109
CS0DL	0xED	0x0	CS0 Data Low Byte	109
CS0MD1	0xAF	0x0	CS0 Mode1	113
CS0MD2	0xF3	0x0	CS0 Mode 2	114
CS0MD3	0xF3	0xF	CS0 Mode 3	115
CS0MX	0xAB	0x0	CS0 Mux Channel Select	118
CS0PM	0xDE	0xF	CS0 Power Management	116
CS0SCAN0	0xD2	0x0	CS0 Scan Channel Enable 0	110
CS0SCAN1	0xD3	0x0	CS0 Scan Channel Enable 1	110
CS0SE	0xDE	0x0	CS0 Auto-Scan End Channel	111
CS0SS	0xDD	0x0	CS0 Auto-Scan Start Channel	111
CS0THH	0xFE	0x0	CS0 Comparator Threshold High Byte	112
CS0THL	0xFD	0x0	CS0 Comparator Threshold Low Byte	112
DEVICEID	0xE3	0xF	Device ID	154
DPH	0x83	All	Data Pointer High	125
DPL	0x82	All	Data Pointer Low	125
EIE1	0xE6	All	Extended Interrupt Enable 1	144
EIE2	0xE7	All	Extended Interrupt Enable 2	146
EIP1	0xF6	All	Extended Interrupt Priority 1	145
EIP2	0xF7	All	Extended Interrupt Priority 2	147
FLKEY	0xB7	All	Flash Lock And Key	160
FLSCL	0xB6	0x0	Flash Scale Register	161
FLWR	0xE5	All	Flash Write Only Register	161
IE	0xA8	All	Interrupt Enable	142
IP	0xB8	All	Interrupt Priority	143
IREF0CF	0xB9	All	Current Reference IREF0 Configuration	92
IREF0CN	0xD6	0x0	Current Reference IREF0 Control	91
IT01CF	0xE4	0x0	INT0/INT1 Configuration	149
OSCICL	0xB3	0x0	Internal Oscillator Calibration	195
OSCICN	0xB2	0x0	Internal Oscillator Control	194
OSCXCN	0xB1	0x0	External Oscillator Control	196
P0	0x80	All	Port 0 Latch	228
P0DRV	0x99	0xF	Port 0 Drive Strength	230
P0MASK	0xC7	0x0	Port 0 Mask	225
P0MAT	0xD7	0x0	Port 0 Match	225
P0MDIN	0xF1	0x0	Port 0 Input Mode Configuration	229
P0MDOUT	0xA4	0x0	Port 0 Output Mode Configuration	229
P0SKIP	0xD4	0x0	Port 0 Skip	228
P1	0x90	All	Port 1 Latch	231
P1DRV	0x9B	0xF	Port 1 Drive Strength	233
P1MASK	0xBF	0x0	Port 1 Mask	226
P1MAT	0xCF	0x0	Port 1 Match	226
P1MDIN	0xF2	0x0	Port 1 Input Mode Configuration	232
P1MDOUT	0xA5	0x0	Port 1 Output Mode Configuration	228

13.3. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. If a high priority interrupt preempts a low priority interrupt, the low priority interrupt will finish execution after the high priority interrupt completes. Each interrupt has an associated interrupt priority bit in in the Interrupt Priority and Extended Interrupt Priority registers used to configure its priority level. Low priority is the default.

If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate. See Table 13.1 on page 140 to determine the fixed priority order used to arbitrate between simultaneously recognized interrupts.

13.4. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 7 system clock cycles: 1 clock cycle to detect the interrupt, 1 clock cycle to execute a single instruction, and 5 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 19 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 5 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.

SFR Definition 13.5. EIE2: Extended Interrupt Enable 2

Bit	7	6	5	4	3	2	1	0
Name		ECSEOS	ECSDC	ECSCPT		ERTC0F	EMAT	EWARN
Type	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All;SFR Address = 0xE7

Bit	Name	Function
7	Unused	Read = 0b. Write = Don't care.
6	ECSEOS	**Enable Capacitive Sense End of Scan Interrupt.** 0: Disable Capacitive Sense End of Scan interrupt. 1: Enable interrupt requests generated by CS0EOS.
5	ECSDC	**Enable Capacitive Sense Digital Comparator Interrupt.** 0: Disable Capacitive Sense Digital Comparator interrupt. 1: Enable interrupt requests generated by CS0CMPF.
4	ECSCPT	**Enable Capacitive Sense Conversion Complete Interrupt.** 0: Disable Capacitive Sense Conversion Complete interrupt. 1: Enable interrupt requests generated by CS0INT.
3	Unused	Read = 0b. Write = Don't care.
2	ERTC0F	**Enable SmaRTClock Oscillator Fail Interrupt.** This bit sets the masking of the SmaRTClock Alarm interrupt. 0: Disable SmaRTClock Alarm interrupts. 1: Enable interrupt requests generated by SmaRTClock Alarm.
1	EMAT	**Enable Port Match Interrupts.** This bit sets the masking of the Port Match Event interrupt. 0: Disable all Port Match interrupts. 1: Enable interrupt requests generated by a Port Match.
0	EWARN	**Enable Supply Monitor Early Warning Interrupt.** This bit sets the masking of the Supply Monitor Early Warning interrupt. 0: Disable the Supply Monitor Early Warning interrupt. 1: Enable interrupt requests generated by the Supply Monitor.

14.1.2. Flash Erase Procedure

The Flash memory is organized in 512-byte pages. The erase operation applies to an entire page (setting all bytes in the page to 0xFF). To erase an entire Flash page, perform the following steps:

1. Save current interrupt state and disable interrupts.
2. Set the PSEE bit (register PSCTL).
3. Set the PSWE bit (register PSCTL).
4. Write the first key code to FLKEY: 0xA5.
5. Write the second key code to FLKEY: 0xF1.
6. Using the MOVX instruction, write a data byte to any location within the page to be erased.
7. Clear the PSWE and PSEE bits.
8. Restore previous interrupt state.

Steps 4–6 must be repeated for each 512-byte page to be erased.

Notes:

1. Flash security settings may prevent erasure of some Flash pages, such as the reserved area and the page containing the lock bytes. For a summary of Flash security settings and restrictions affecting Flash erase operations, please see Section “14.3. Security Options” on page 152.
2. 8-bit MOVX instructions cannot be used to erase or write to Flash memory at addresses higher than 0x00FF.

14.1.3. Flash Write Procedure

A write to Flash memory can clear bits to logic 0 but cannot set them; only an erase operation can set bits to logic 1 in Flash. **A byte location to be programmed should be erased before a new value is written.**

The recommended procedure for writing a single byte in Flash is as follows:

1. Save current interrupt state and disable interrupts.
2. Ensure that the Flash byte has been erased (has a value of 0xFF).
3. Set the PSWE bit (register PSCTL).
4. Clear the PSEE bit (register PSCTL).
5. Write the first key code to FLKEY: 0xA5.
6. Write the second key code to FLKEY: 0xF1.
7. Using the MOVX instruction, write a single data byte to the desired location within the 1024-byte sector.
8. Clear the PSWE bit.
9. Restore previous interrupt state.

Steps 5–7 must be repeated for each byte to be written.

Notes:

1. Flash security settings may prevent writes to some areas of Flash, such as the reserved area. For a summary of Flash security settings and restrictions affecting Flash write operations, please see Section “14.3. Security Options” on page 152.
2. 8-bit MOVX instructions cannot be used to erase or write to Flash memory at addresses higher than 0x00FF.

14.2. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction. MOVX read instructions always target XRAM.

SFR Definition 15.1. PMU0CF: Power Management Unit Configuration[1,2,3]

Bit	7	6	5	4	3	2	1	0
Name	SLEEP	SUSPEND	CLEAR	RSTWK	RTCFWK	RTCAWK	PMATWK	CPT0WK
Type	W	W	W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	Varies	Varies	Varies	Varies	Varies

SFR Page = 0x0; SFR Address = 0xB5

Bit	Name	Description	Write	Read
7	SLEEP	**Sleep Mode Select**	Writing 1 places the device in Sleep Mode.	N/A
6	SUSPEND	**Suspend Mode Select**	Writing 1 places the device in Suspend Mode.	N/A
5	CLEAR	**Wake-up Flag Clear**	Writing 1 clears all wake-up flags.	N/A
4	RSTWK	**Reset Pin Wake-up Flag**	N/A	Set to 1 if a glitch has been detected on $\overline{RST}$.
3	RTCFWK	**SmaRTClock Oscillator Fail Wake-up Source Enable and Flag**	0: Disable wake-up on SmaRTClock Osc. Fail. 1: Enable wake-up on SmaRTClock Osc. Fail.	Set to 1 if the SmaRT-Clock Oscillator has failed.
2	RTCAWK	**SmaRTClock Alarm Wake-up Source Enable and Flag**	0: Disable wake-up on SmaRTClock Alarm. 1: Enable wake-up on SmaRTClock Alarm.	Set to 1 if a SmaRTClock Alarm has occurred.
1	PMATWK	**Port Match Wake-up Source Enable and Flag**	0: Disable wake-up on Port Match Event. 1: Enable wake-up on Port Match Event.	Set to 1 if a Port Match Event has occurred.
0	CPT0WK	**Comparator0 Wake-up Source Enable and Flag**	0: Disable wake-up on Comparator0 rising edge. 1: Enable wake-up on Comparator0 rising edge.	Set to 1 if Comparator0 rising edge caused the last wake-up.

Notes:

1. Read-modify-write operations (ORL, ANL, etc.) should not be used on this register. Wake-up sources must be re-enabled each time the SLEEP or SUSPEND bits are written to 1.
2. The Low Power Internal Oscillator cannot be disabled and the MCU cannot be placed in Suspend or Sleep Mode if any wake-up flags are set to 1. Software should clear all wake-up sources after each reset and after each wake-up from Suspend or Sleep Modes.
3. PMU0 requires two system clocks to update the wake-up source flags after waking from Suspend mode. The wake-up source flags will read ‘0’ during the first two system clocks following the wake from Suspend mode.

SFR Definition 18.2. RSTSRC: Reset Source

Bit	7	6	5	4	3	2	1	0
Name	RTC0RE	FERROR	C0RSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF
Type	R/W	R	R/W	R/W	R	R/W	R/W	R
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Page = 0x0; SFR Address = 0xEF.

Bit	Name	Description	Write	Read
7	RTC0RE	**SmaRTClock Reset Enable and Flag**	0: Disable SmaRTClock as a reset source. 1: Enable SmaRTClock as a reset source.	Set to 1 if SmaRTClock alarm or oscillator fail caused the last reset.
6	FERROR	**Flash Error Reset Flag.**	N/A	Set to 1 if Flash read/write/erase error caused the last reset.
5	C0RSEF	**Comparator0 Reset Enable and Flag.**	0: Disable Comparator0 as a reset source. 1: Enable Comparator0 as a reset source.	Set to 1 if Comparator0 caused the last reset.
4	SWRSF	**Software Reset Force and Flag.**	Writing a 1 forces a system reset.	Set to 1 if last reset was caused by a write to SWRSF.
3	WDTRSF	**Watchdog Timer Reset Flag.**	N/A	Set to 1 if Watchdog Timer overflow caused the last reset.
2	MCDRSF	**Missing Clock Detector (MCD) Enable and Flag.**	0: Disable the MCD. 1: Enable the MCD. The MCD triggers a reset if a missing clock condition is detected.	Set to 1 if Missing Clock Detector timeout caused the last reset.
1	PORSF	**Power-On / Power-Fail Reset Flag, and Power-Fail Reset Enable.**	0: Disable the VDD Supply Monitor as a reset source. 1: Enable the VDD Supply Monitor as a reset source.[3]	Set to 1 anytime a power-on or V_{DD} monitor reset occurs.[2]
0	PINRSF	**HW Pin Reset Flag.**	N/A	Set to 1 if $\overline{RST}$ pin caused the last reset.

Notes:
1. It is safe to use read-modify-write operations (ORL, ANL, etc.) to enable or disable specific interrupt sources.
2. If PORSF read back 1, the value read from all other bits in this register are indeterminate.
3. Writing a 1 to PORSF before the VDD Supply Monitor is stabilized may generate a system reset.

Internal Register Definition 20.7. CAPTUREn: SmaRTClock Timer Capture

Bit	7	6	5	4	3	2	1	0
Name	CAPTURE[31:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SmaRTClock Addresses: CAPTURE0 = 0x00; CAPTURE1 = 0x01; CAPTURE2 =0x02; CAPTURE3: 0x03.

Bit	Name	Function
7:0	CAPTURE[31:0]	**SmaRTClock Timer Capture.** These 4 registers (CAPTURE3–CAPTURE0) are used to read or set the 32-bit SmaRTClock timer. Data is transferred to or from the SmaRTClock timer when the RTC0SET or RTC0CAP bits are set.
Note: The least significant bit of the timer capture value is in CAPTURE0.0.		

Internal Register Definition 20.8. ALARMn: SmaRTClock Alarm Programmed Value

Bit	7	6	5	4	3	2	1	0
Name	ALARM[31:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SmaRTClock Addresses: ALARM0 = 0x08; ALARM1 = 0x09; ALARM2 = 0x0A; ALARM3 = 0x0B

Bit	Name	Function
7:0	ALARM[31:0]	**SmaRTClock Alarm Programmed Value.** These 4 registers (ALARM3–ALARM0) are used to set an alarm event for the SmaRTClock timer. The SmaRTClock alarm should be disabled (RTC0AEN=0) when updating these registers.
Note: The least significant bit of the alarm programmed value is in ALARM0.0.		

23. UART0

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates (details in Section “23.1. Enhanced Baud Rate Generation” on page 258). Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

UART0 has two associated SFRs: Serial Control Register 0 (SCON0) and Serial Data Buffer 0 (SBUF0). The single SBUF0 location provides access to both transmit and receive registers. **Writes to SBUF0 always access the Transmit register. Reads of SBUF0 always access the buffered Receive register; it is not possible to read data from the Transmit register.**

With UART0 interrupts enabled, an interrupt is generated each time a transmit is completed (TI0 is set in SCON0), or a data byte has been received (RI0 is set in SCON0). The UART0 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART0 interrupt (transmit complete or receive complete).

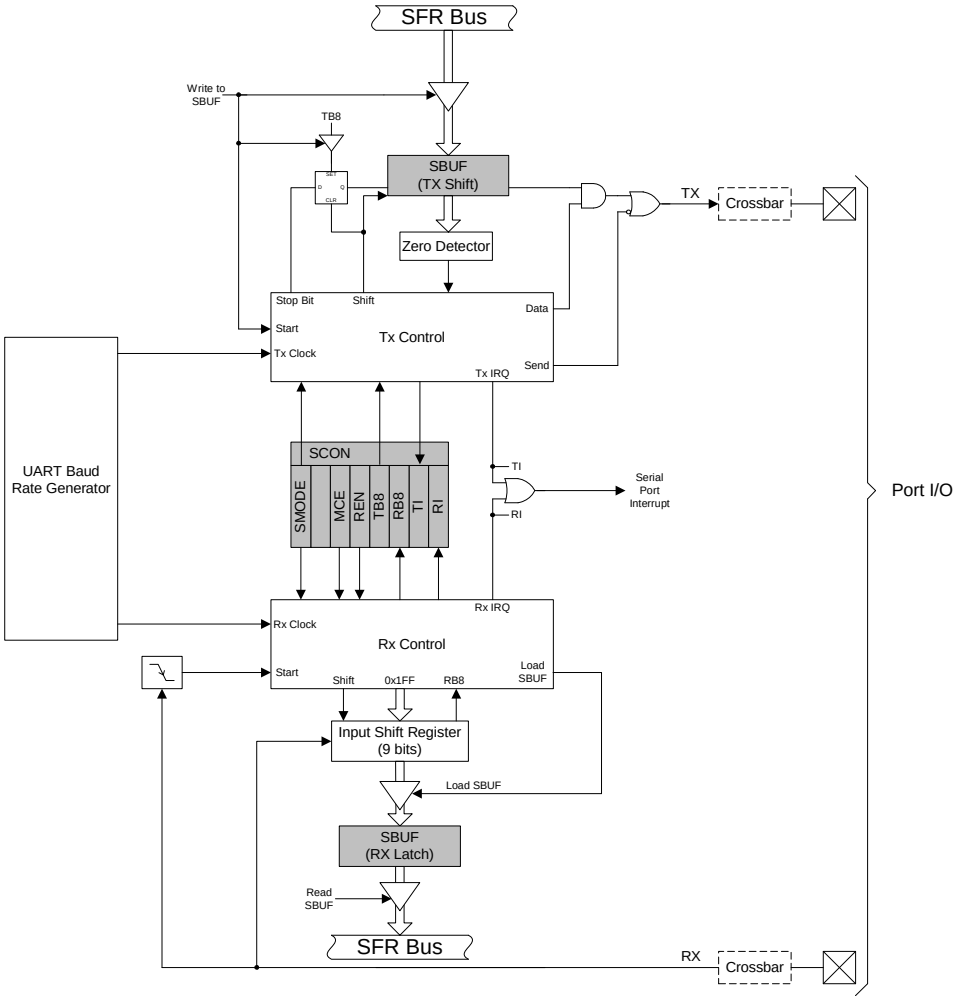

Figure 23.1. UART0 Block Diagram

1 at the end of the transfer. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set. While the SPI0 master transfers data to a slave on the MOSI line, the addressed SPI slave device simultaneously transfers the contents of its shift register to the SPI master on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPI0DAT.

When configured as a master, SPI0 can operate in one of three different modes: multi-master mode, 3-wire single-master mode, and 4-wire single-master mode. The default, multi-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In this mode, NSS is an input to the device, and is used to disable the master SPI0 when another master is accessing the bus. When NSS is pulled low in this mode, MSTEN (SPI0CN.6) and SPIEN (SPI0CN.0) are set to 0 to disable the SPI master device, and a Mode Fault is generated (MODF, SPI0CN.5 = 1). Mode Fault will generate an interrupt if enabled. SPI0 must be manually re-enabled in software under these circumstances. In multi-master systems, devices will typically default to being slave devices while they are not acting as the system master device. In multi-master mode, slave devices can be addressed individually (if needed) using general-purpose I/O pins. Figure 24.2 shows a connection diagram between two master devices in multiple-master mode.

3-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. In this mode, NSS is not used, and is not mapped to an external port pin through the crossbar. Any slave devices that must be addressed in this mode should be selected using general-purpose I/O pins. Figure 24.3 shows a connection diagram between a master device in 3-wire master mode and a slave device.

4-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 1. In this mode, NSS is configured as an output pin, and can be used as a slave-select signal for a single SPI device. In this mode, the output value of NSS is controlled (in software) with the bit NSSMD0 (SPI0CN.2). Additional slave devices can be addressed using general-purpose I/O pins. Figure 24.4 shows a connection diagram for a master device in 4-wire master mode and two slave devices.

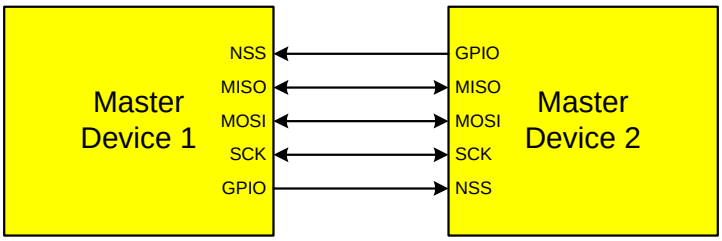

Figure 24.2. Multiple-Master Mode Connection Diagram

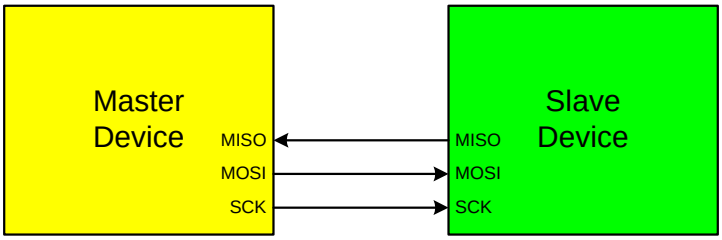

Figure 24.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram

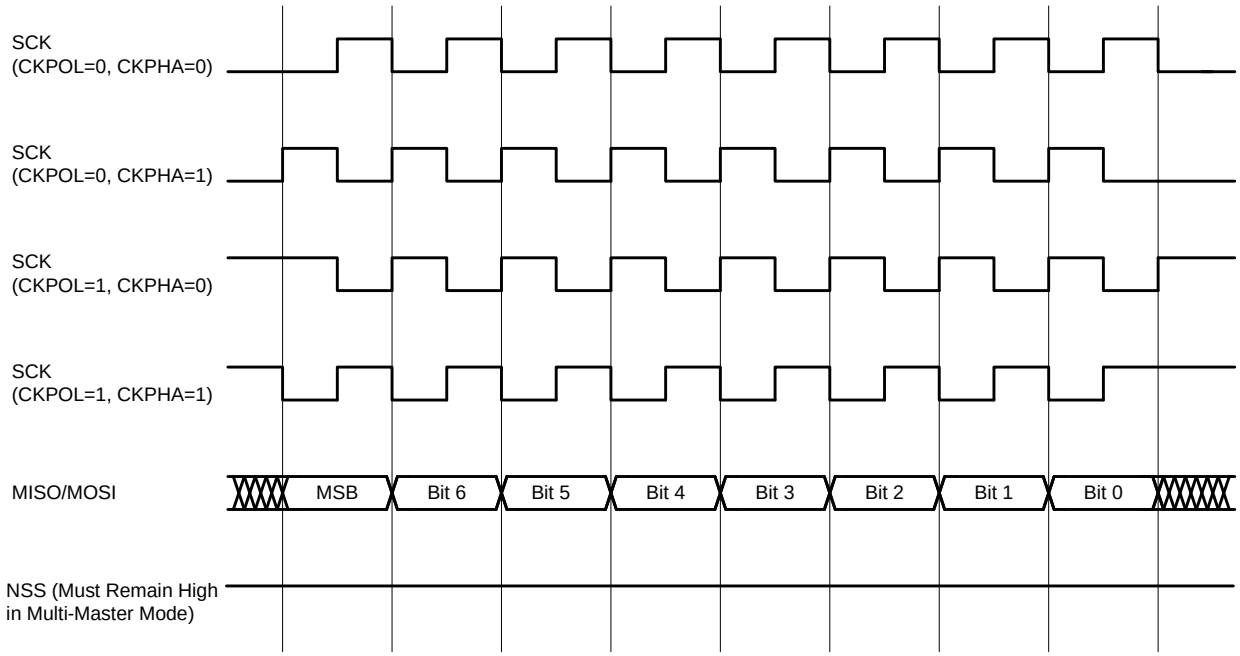

Figure 24.5. Master Mode Data/Clock Timing

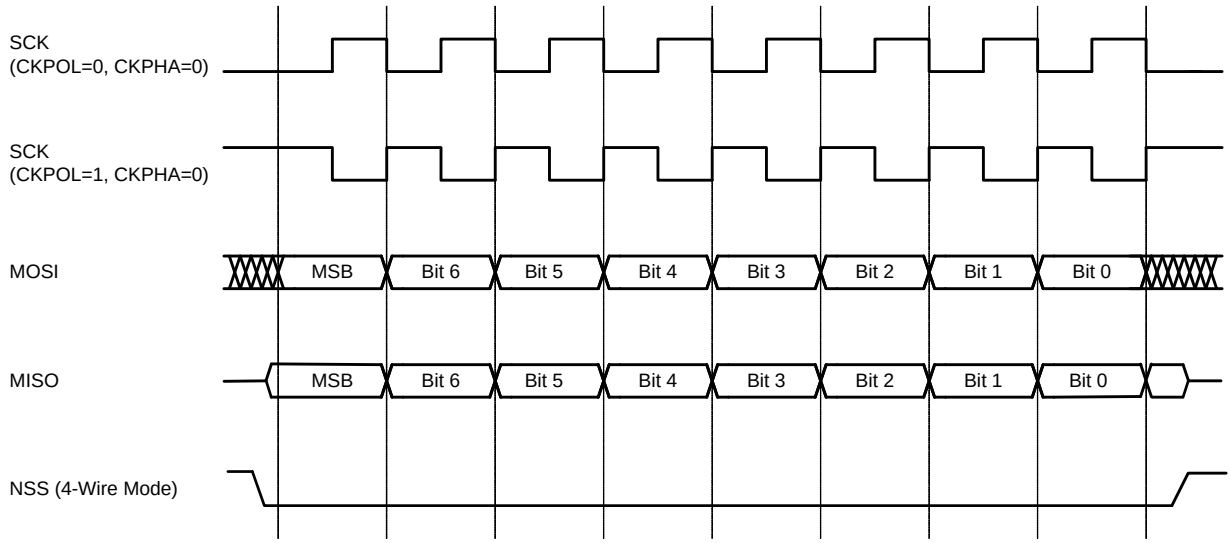

Figure 24.6. Slave Mode Data/Clock Timing (CKPHA = 0)

SFR Definition 25.1. CKCON: Clock Control

Bit	7	6	5	4	3	2	1	0
Name	T3MH	T3ML	T2MH	T2ML	T1M	T0M	SCA[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x8E

Bit	Name	Function
7	T3MH	**Timer 3 High Byte Clock Select.** Selects the clock supplied to the Timer 3 high byte (split 8-bit timer mode only). 0: Timer 3 high byte uses the clock defined by the T3XCLK bit in TMR3CN. 1: Timer 3 high byte uses the system clock.
6	T3ML	**Timer 3 Low Byte Clock Select.** Selects the clock supplied to Timer 3. Selects the clock supplied to the lower 8-bit timer in split 8-bit timer mode. 0: Timer 3 low byte uses the clock defined by the T3XCLK bit in TMR3CN. 1: Timer 3 low byte uses the system clock.
5	T2MH	**Timer 2 High Byte Clock Select.** Selects the clock supplied to the Timer 2 high byte (split 8-bit timer mode only). 0: Timer 2 high byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 high byte uses the system clock.
4	T2ML	**Timer 2 Low Byte Clock Select.** Selects the clock supplied to Timer 2. If Timer 2 is configured in split 8-bit timer mode, this bit selects the clock supplied to the lower 8-bit timer. 0: Timer 2 low byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 low byte uses the system clock.
3	T1M	**Timer 1 Clock Select.** Selects the clock source supplied to Timer 1. Ignored when C/T1 is set to 1. 0: Timer 1 uses the clock defined by the prescale bits SCA[1:0]. 1: Timer 1 uses the system clock.
2	T0M	**Timer 0 Clock Select.** Selects the clock source supplied to Timer 0. Ignored when C/T0 is set to 1. 0: Counter/Timer 0 uses the clock defined by the prescale bits SCA[1:0]. 1: Counter/Timer 0 uses the system clock.
1:0	SCA[1:0]	**Timer 0/1 Prescale Bits.** These bits control the Timer 0/1 Clock Prescaler: 00: System clock divided by 12 01: System clock divided by 4 10: System clock divided by 48 11: External clock divided by 8 (synchronized with the system clock)

SFR Definition 26.4. PCA0CPMn: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address, Page: PCA0CPM0 = 0xDA, 0x0; PCA0CPM1 = 0xDB, 0x0; PCA0CPM2 = 0xDC, 0x0

Bit	Name	Function
7	PWM16n	**16-bit Pulse Width Modulation Enable.** This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected. 1: 16-bit PWM selected.
6	ECOMn	**Comparator Function Enable.** This bit enables the comparator function for PCA module n when set to 1.
5	CAPPn	**Capture Positive Function Enable.** This bit enables the positive edge capture for PCA module n when set to 1.
4	CAPNn	**Capture Negative Function Enable.** This bit enables the negative edge capture for PCA module n when set to 1.
3	MATn	**Match Function Enable.** This bit enables the match function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
2	TOGn	**Toggle Function Enable.** This bit enables the toggle function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWMn	**Pulse Width Modulation Mode Enable.** This bit enables the PWM function for PCA module n when set to 1. When enabled, a pulse width modulated signal is output on the CEXn pin. 8 to 11-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0	ECCFn	**Capture/Compare Flag Interrupt Enable.** This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt. 0: Disable CCFn interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCFn is set.
Note: When the WDTE bit is set to 1, the PCA0CPM5 register cannot be modified, and module 5 acts as the watchdog timer. To change the contents of the PCA0CPM5 register or the function of module 5, the Watchdog Timer must be disabled.		