



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I <sup>2</sup> C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/c8051f981-c-gmr">https://www.e-xfl.com/product-detail/silicon-labs/c8051f981-c-gmr</a>

# C8051F99x-C8051F98x

## 1.1. CIP-51™ Microcontroller Core

### 1.1.1. Fully 8051 Compatible

The C8051F99x-C8051F98x family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052.

### 1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS.

### 1.1.3. Additional Features

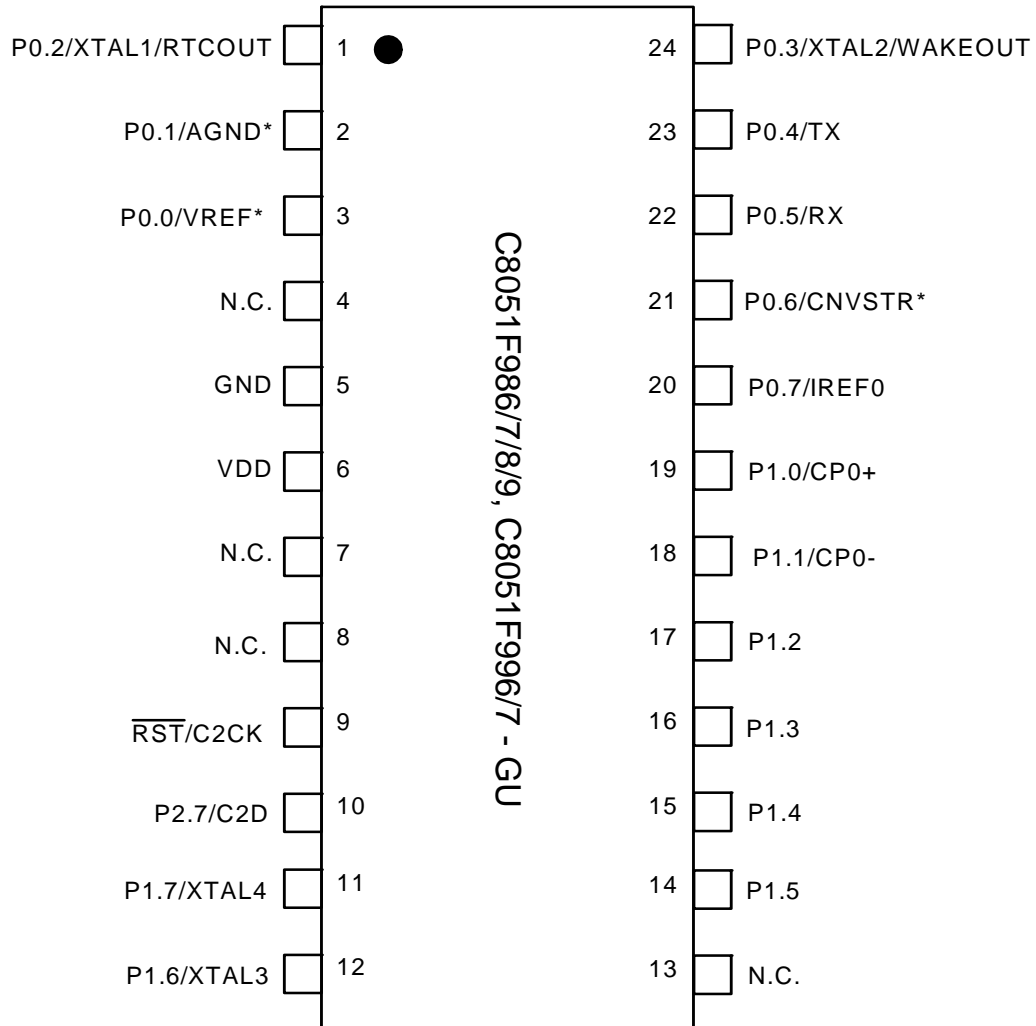
The C8051F99x-C8051F98x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides multiple interrupt sources into the CIP-51 allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip  $V_{DD}$  monitor (forces reset when power supply voltage drops below safe levels), a Watchdog Timer, a Missing Clock Detector, SmaRTClock oscillator fail or alarm, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently disabled in software after a power-on reset during MCU initialization.

The internal oscillator is factory calibrated to 24.5 MHz and is accurate to  $\pm 2\%$  over the full temperature and supply range. The internal oscillator period can also be adjusted by user firmware. An additional 20 MHz low power oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.

# C8051F99x-C8051F98x



**\*Note:** Signal only available on 'F986, 'F988, and 'F996 devices.

**Figure 3.3. QSOP-24 Pinout Diagram (Top View)**

**Table 4.12. Voltage Reference Electrical Characteristics**

$V_{DD}$  = 1.8 to 3.6 V, -40 to +85 °C unless otherwise specified.

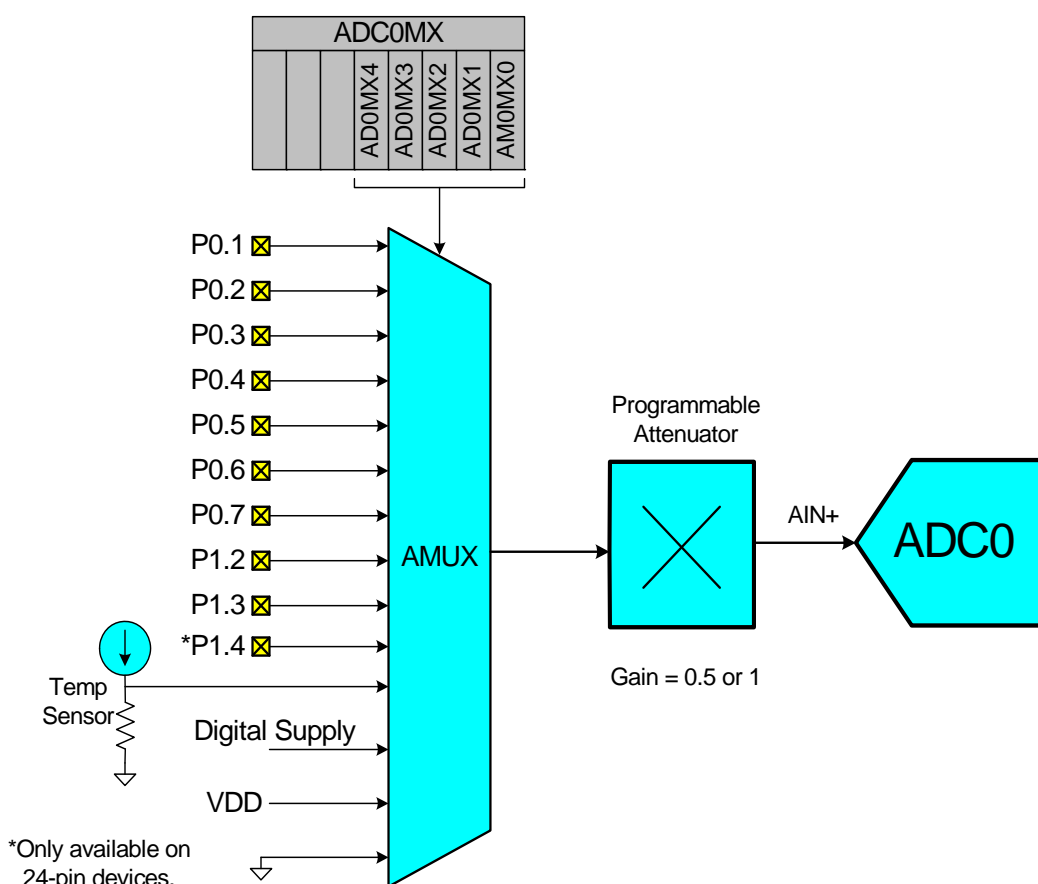
Parameter	Conditions	Min	Typ	Max	Units
<b>Internal High-Speed Reference (REFSL[1:0] = 11)</b>					
Output Voltage	-40 to +85 °C, $V_{DD}$ = 1.8–3.6 V	1.62	1.65	1.68	V
VREF Turn-on Time		—	—	1.5	μs
Supply Current	Normal Power Mode	—	260	—	μA
	Low Power Mode	—	140	—	
<b>External Reference (REFSL[1:0] = 00, REFOE = 0)</b>					
Input Voltage Range		0	—	$V_{DD}$	V
Input Current	Sample Rate = 300 ksps; $V_{REF}$ = 3.0 V	—	5.25	—	μA

# C8051F99x-C8051F98x

## 5.7. ADC0 Analog Multiplexer

ADC0 on C8051F99x-C8051F98x has an analog multiplexer, referred to as AMUX0.

AMUX0 selects the positive inputs to the single-ended ADC0. Any of the following may be selected as the positive input: Port I/O pins, the on-chip temperature sensor, Regulated Digital Supply Voltage (Output of VREG0), VDD Supply, or the positive input may be connected to GND. The ADC0 input channels are selected in the ADC0MX register described in SFR Definition 5.12.



**Figure 5.7. ADC0 Multiplexer Block Diagram**

**Important Note About ADC0 Input Configuration:** Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN and disable the digital driver (PnMDOUT = 0 and Port Latch = 1). To force the Crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP. See Section “21. Port Input/Output” on page 215 for more Port I/O configuration details.

## SFR Definition 5.12. ADC0MX: ADC0 Input Channel Select

Bit	7	6	5	4	3	2	1	0
Name				AD0MX				
Type	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	1

SFR Page = 0x0; SFR Address = 0x96

Bit	Name	Function																																																																				
7:5	Unused	Read = 000b; Write = Don't Care.																																																																				
4:0	AD0MX	<b>AMUX0 Positive Input Selection.</b> Selects the positive input channel for ADC0. <table><tr><td>00000:</td><td>Reserved.</td><td>10000:</td><td>Reserved.</td></tr><tr><td>00001:</td><td>P0.1</td><td>10001:</td><td>Reserved.</td></tr><tr><td>00010:</td><td>P0.2</td><td>10010:</td><td>Reserved.</td></tr><tr><td>00011:</td><td>P0.3</td><td>10011:</td><td>Reserved.</td></tr><tr><td>00100:</td><td>P0.4</td><td>10100:</td><td>Reserved.</td></tr><tr><td>00101:</td><td>P0.5</td><td>10101:</td><td>Reserved.</td></tr><tr><td>00110:</td><td>P0.6</td><td>10110:</td><td>Reserved.</td></tr><tr><td>00111:</td><td>P0.7</td><td>10111:</td><td>Reserved.</td></tr><tr><td>01000:</td><td>Reserved.</td><td>11000:</td><td>Reserved.</td></tr><tr><td>01001:</td><td>Reserved.</td><td>11001:</td><td>Reserved.</td></tr><tr><td>01010:</td><td>P1.2</td><td>11010:</td><td>Reserved.</td></tr><tr><td>01011:</td><td>P1.3</td><td>11011:</td><td>Temperature Sensor</td></tr><tr><td>01100:</td><td>P1.4 (only available on 24-pin devices)</td><td>11100:</td><td>V<sub>DD</sub> Supply Voltage</td></tr><tr><td>01101:</td><td>Reserved.</td><td>11101:</td><td>Digital Supply Voltage (VREG0 Output, 1.7 V Typical)</td></tr><tr><td>01110:</td><td>Reserved.</td><td></td><td></td></tr><tr><td>01111:</td><td>Reserved.</td><td>11110:</td><td>V<sub>DD</sub> Supply Voltage</td></tr><tr><td></td><td></td><td>11111:</td><td>Ground</td></tr></table>	00000:	Reserved.	10000:	Reserved.	00001:	P0.1	10001:	Reserved.	00010:	P0.2	10010:	Reserved.	00011:	P0.3	10011:	Reserved.	00100:	P0.4	10100:	Reserved.	00101:	P0.5	10101:	Reserved.	00110:	P0.6	10110:	Reserved.	00111:	P0.7	10111:	Reserved.	01000:	Reserved.	11000:	Reserved.	01001:	Reserved.	11001:	Reserved.	01010:	P1.2	11010:	Reserved.	01011:	P1.3	11011:	Temperature Sensor	01100:	P1.4 (only available on 24-pin devices)	11100:	V <sub>DD</sub> Supply Voltage	01101:	Reserved.	11101:	Digital Supply Voltage (VREG0 Output, 1.7 V Typical)	01110:	Reserved.			01111:	Reserved.	11110:	V <sub>DD</sub> Supply Voltage			11111:	Ground
00000:	Reserved.	10000:	Reserved.																																																																			
00001:	P0.1	10001:	Reserved.																																																																			
00010:	P0.2	10010:	Reserved.																																																																			
00011:	P0.3	10011:	Reserved.																																																																			
00100:	P0.4	10100:	Reserved.																																																																			
00101:	P0.5	10101:	Reserved.																																																																			
00110:	P0.6	10110:	Reserved.																																																																			
00111:	P0.7	10111:	Reserved.																																																																			
01000:	Reserved.	11000:	Reserved.																																																																			
01001:	Reserved.	11001:	Reserved.																																																																			
01010:	P1.2	11010:	Reserved.																																																																			
01011:	P1.3	11011:	Temperature Sensor																																																																			
01100:	P1.4 (only available on 24-pin devices)	11100:	V <sub>DD</sub> Supply Voltage																																																																			
01101:	Reserved.	11101:	Digital Supply Voltage (VREG0 Output, 1.7 V Typical)																																																																			
01110:	Reserved.																																																																					
01111:	Reserved.	11110:	V <sub>DD</sub> Supply Voltage																																																																			
		11111:	Ground																																																																			

# C8051F99x-C8051F98x

## SFR Definition 5.15. REF0CN: Voltage Reference Control

Bit	7	6	5	4	3	2	1	0
Name			REFGND	REFSL		TEMPE		
Type	R	R	R/W	R/W	R/W	R/W	R	R
Reset	0	0	0	1	1	0	0	0

SFR Page = 0x0; SFR Address = 0xD1

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5	REFGND	<b>Analog Ground Reference.</b> Selects the ADC0 ground reference. 0: The ADC0 ground reference is the GND pin. 1: The ADC0 ground reference is the P0.1/AGND pin.
4:3	REFSL	<b>Voltage Reference Select.</b> Selects the ADC0 voltage reference. 00: The ADC0 voltage reference is the P0.0/VREF pin. 01: The ADC0 voltage reference is the VDD pin. 10: The ADC0 voltage reference is the internal 1.8 V digital supply voltage. 11: The ADC0 voltage reference is the internal 1.65 V high speed voltage reference.
2	TEMPE	<b>Temperature Sensor Enable.</b> Enables/Disables the internal temperature sensor. 0: Temperature Sensor Disabled. 1: Temperature Sensor Enabled.
1:0	Unused	Read = 00b; Write = Don't Care.

## 5.14. Voltage Reference Electrical Specifications

See Table 4.12 on page 61 for detailed Voltage Reference Electrical Specifications.

## 8.14. Capacitive Sense Multiplexer

The input multiplexer can be controlled through two methods. The CS0MX register can be written to through firmware, or the register can be configured automatically using the modules auto-scan functionality (see “8.8. Automatic Scanning (Method 1—CS0SMEN = 0)” ).

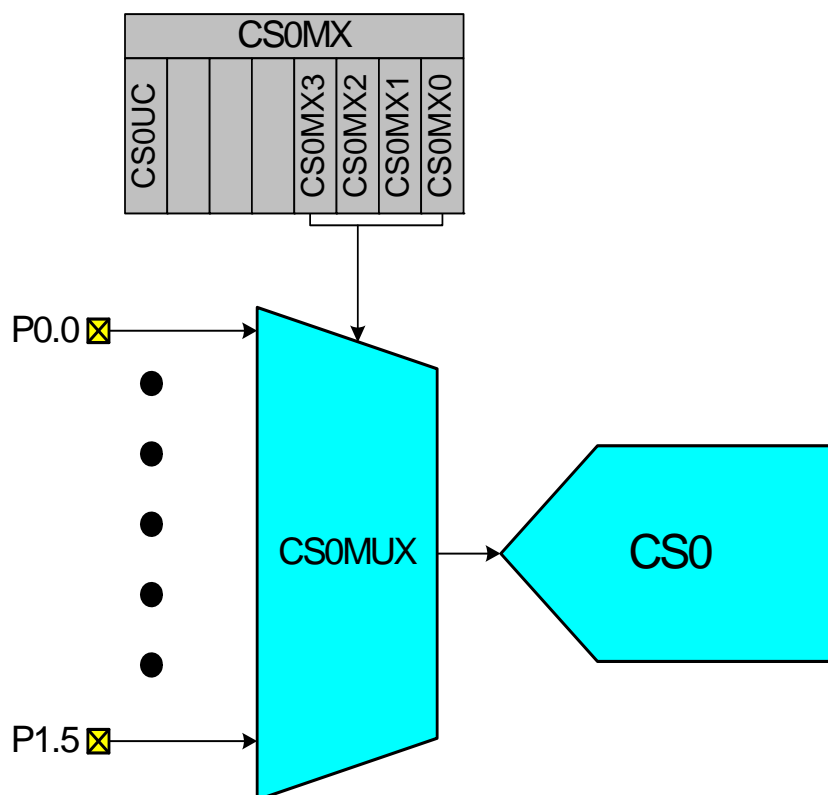


Figure 8.3. CS0 Multiplexer Block Diagram



# C8051F99x-C8051F98x

## SFR Definition 9.6. PSW: Program Status Word

Bit	7	6	5	4	3	2	1	0
Name	CY	AC	F0	RS[1:0]		OV	F1	PARITY
Type	R/W	R/W	R/W	R/W		R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0xD0; Bit-Addressable

Bit	Name	Function
7	CY	<b>Carry Flag.</b> This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to logic 0 by all other arithmetic operations.
6	AC	<b>Auxiliary Carry Flag.</b> This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to logic 0 by all other arithmetic operations.
5	F0	<b>User Flag 0.</b> This is a bit-addressable, general purpose flag for use under software control.
4:3	RS[1:0]	<b>Register Bank Select.</b> These bits select which register bank is used during register accesses. 00: Bank 0, Addresses 0x00-0x07 01: Bank 1, Addresses 0x08-0x0F 10: Bank 2, Addresses 0x10-0x17 11: Bank 3, Addresses 0x18-0x1F
2	OV	<b>Overflow Flag.</b> This bit is set to 1 under the following circumstances: <ul style="list-style-type: none"> <li>• An ADD, ADDC, or SUBB instruction causes a sign-change overflow.</li> <li>• A MUL instruction results in an overflow (result is greater than 255).</li> <li>• A DIV instruction causes a divide-by-zero condition.</li> </ul> The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.
1	F1	<b>User Flag 1.</b> This is a bit-addressable, general purpose flag for use under software control.
0	PARITY	<b>Parity Flag.</b> This bit is set to logic 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

---

## 13.5. Interrupt Register Descriptions

The SFRs used to enable the interrupt sources and set their priority level are described in the following register descriptions. Refer to the data sheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

---

## SFR Definition 14.2. REVID: Revision Identification

---

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xE2

Bit	Name	Function
7:0	REVID[7:0]	<b>Revision Identification.</b> These bits contain a value that can be decoded to determine the silicon revision. For example, 0x00 for Rev A, 0x01 for Rev B, 0x02 for Rev C, etc.



---

## 20.2.2. Using the SmaRTClock Oscillator in Self-Oscillate Mode

When using Self-Oscillate Mode, the XTAL3 and XTAL4 pins are internally shorted together. The following steps show how to configure SmaRTClock for use in Self-Oscillate Mode:

1. Set SmaRTClock to Self-Oscillate Mode (XMODE = 0).
2. Set the desired oscillation frequency:  
For oscillation at about 20 kHz, set BIASX2 = 0.  
For oscillation at about 40 kHz, set BIASX2 = 1.
3. The oscillator starts oscillating instantaneously.
4. Fine tune the oscillation frequency by adjusting the load capacitance (RTC0XCF).

## 20.2.3. Using the Low Frequency Oscillator (LFO)

The low frequency oscillator provides an ultra low power, on-chip clock source to the SmaRTClock. The typical frequency of oscillation is 16.4 kHz  $\pm$ 20%. No external components are required to use the LFO and the XTAL3 and XTAL4 pins do not need to be shorted together.

The following steps show how to configure SmaRTClock for use with the LFO:

1. Enable and select the Low Frequency Oscillator (LFOEN = 1).
2. The LFO starts oscillating instantaneously.

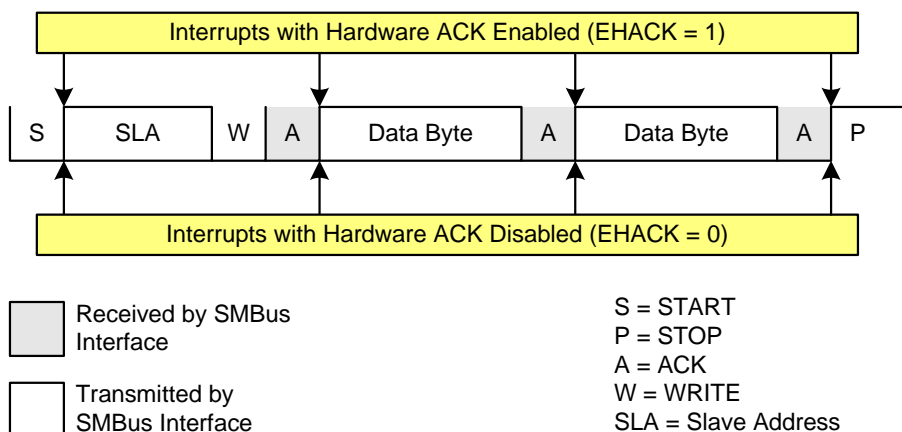
When the LFO is enabled, the SmaRTClock oscillator increments bit 1 of the 32-bit timer (instead of bit 0). This effectively multiplies the LFO frequency by 2, making the RTC timebase behave as if a 32.768 kHz crystal is connected at the output.

## 22.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses an arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames. Note that the position of the ACK interrupt when operating as a receiver depends on whether hardware ACK generation is enabled. As a receiver, the interrupt for an ACK occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled. As a transmitter, interrupts occur **after** the ACK, regardless of whether hardware ACK generation is enabled or not.

### 22.5.1. Write Sequence (Master)

During a write sequence, an SMBus master writes data to a slave device. The master in this transfer will be a transmitter during the address byte, and a transmitter during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. Note that the interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 22.5 shows a typical master write sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that all of the 'data byte transferred' interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.



**Figure 22.5. Typical Master Write Sequence**

# C8051F99x-C8051F98x

Table 22.5. SMBus Status Decoding With Hardware ACK Generation Disabled (EHACK = 0)

Mode	Values Read				Current SMBus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Transmitter	1110	0	0	X	A master START was generated.	Load slave address + R/W into SMB0DAT.	0	0	X	1100
	1100	0	0	0	A master data or address byte was transmitted; NACK received.	Set STA to restart transfer.	1	0	X	1110
						Abort transfer.	0	1	X	—
		0	0	1	A master data or address byte was transmitted; ACK received.	Load next data byte into SMB0DAT.	0	0	X	1100
						End transfer with STOP.	0	1	X	—
						End transfer with STOP and start another transfer.	1	1	X	—
						Send repeated START.	1	0	X	1110
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT).	0	0	X	1000
	1000	1	0	X	A master data byte was received; ACK requested.	Acknowledge received byte; Read SMB0DAT.	0	0	1	1000
						Send NACK to indicate last byte, and send STOP.	0	1	0	—
						Send NACK to indicate last byte, and send STOP followed by START.	1	1	0	1110
						Send ACK followed by repeated START.	1	0	1	1110
						Send NACK to indicate last byte, and send repeated START.	1	0	0	1110
						Send ACK and switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	1	1100
						Send NACK and switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	0	1100

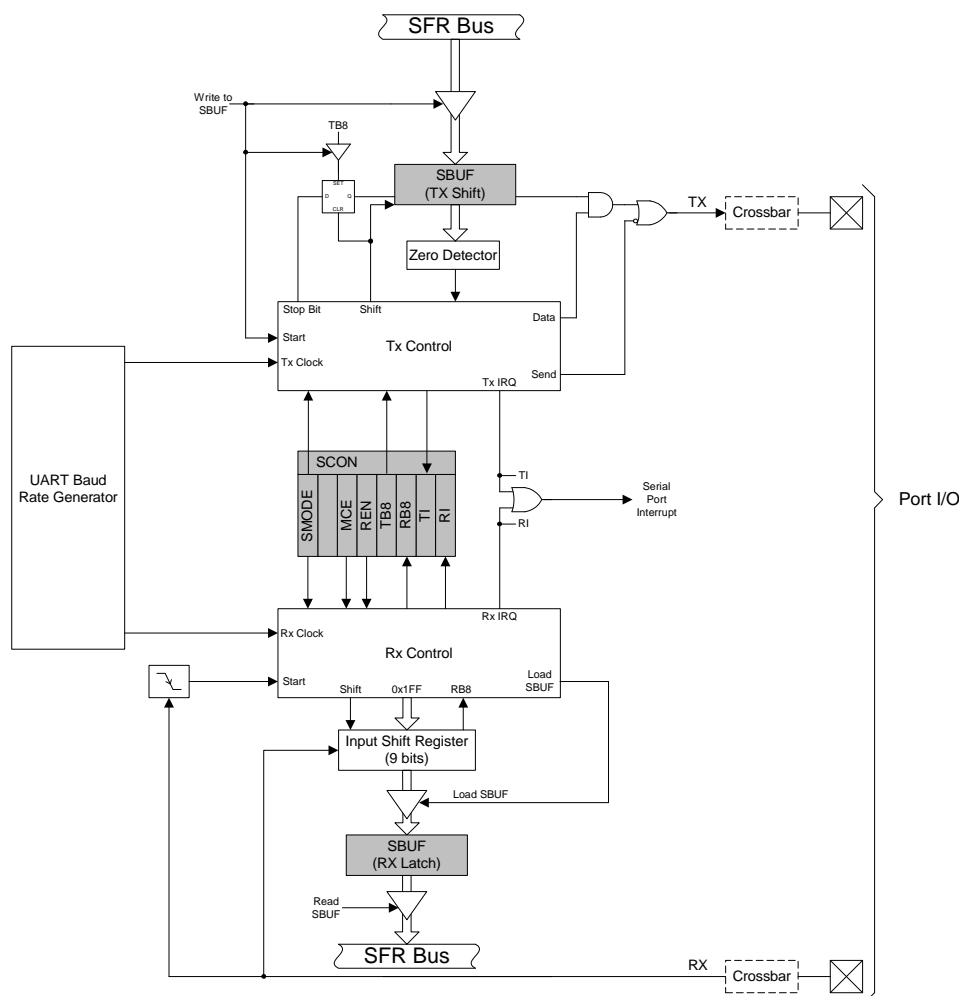
## C8051F99x-C8051F98x

## 23. UART0

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates (details in Section “23.1. Enhanced Baud Rate Generation” on page 258). Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

UART0 has two associated SFRs: Serial Control Register 0 (SCON0) and Serial Data Buffer 0 (SBUF0). The single SBUF0 location provides access to both transmit and receive registers. **Writes to SBUF0 always access the Transmit register. Reads of SBUF0 always access the buffered Receive register; it is not possible to read data from the Transmit register.**

With UART0 interrupts enabled, an interrupt is generated each time a transmit is completed (TI0 is set in SCON0), or a data byte has been received (RI0 is set in SCON0). The UART0 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART0 interrupt (transmit complete or receive complete).



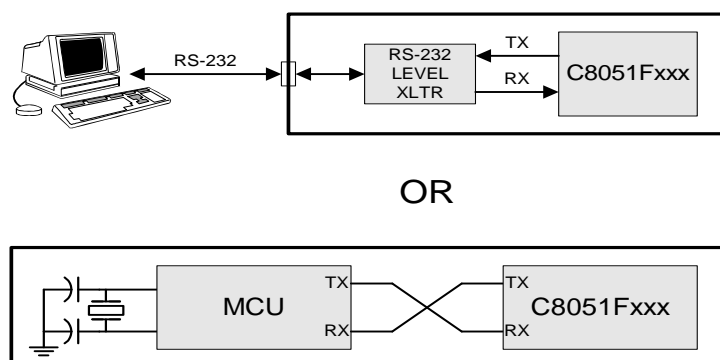
### Figure 23.1. UART0 Block Diagram



# C8051F99x-C8051F98x

## 23.2. Operational Modes

UART0 provides standard asynchronous, full duplex communication. The UART mode (8-bit or 9-bit) is selected by the S0MODE bit (SCON0.7). Typical UART connection options are shown below.



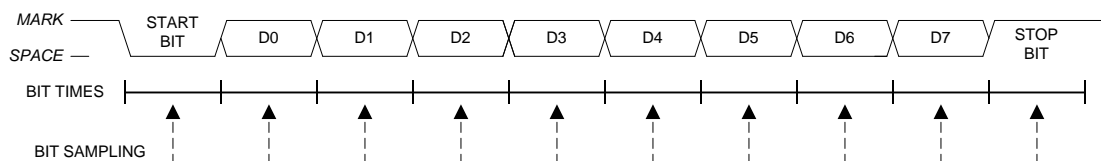
**Figure 23.3. UART Interconnect Diagram**

### 23.2.1. 8-Bit UART

8-Bit UART mode uses a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when software writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if MCE0 is logic 1, the stop bit must be logic 1. In the event of a receive data overrun, the first received 8 bits are latched into the SBUF0 receive register and the following overrun data bits are lost.

If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TI0 or RI0 is set.



**Figure 23.4. 8-Bit UART Timing Diagram**

## 25.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only)

In Mode 3, Timer 0 is configured as two separate 8-bit counter/timers held in TL0 and TH0. The counter/timer in TL0 is controlled using the Timer 0 control/status bits in TCON and TMOD: TR0, C/T0, GATE0 and TF0. TL0 can use either the system clock or an external input signal as its timebase. The TH0 register is restricted to a timer function sourced by the system clock or prescaled clock. TH0 is enabled using the Timer 1 run control bit TR1. TH0 sets the Timer 1 overflow flag TF1 on overflow and thus controls the Timer 1 interrupt.

Timer 1 is inactive in Mode 3. When Timer 0 is operating in Mode 3, Timer 1 can be operated in Modes 0, 1 or 2, but cannot be clocked by external signals nor set the TF1 flag and generate an interrupt. However, the Timer 1 overflow can be used to generate baud rates for the SMBus and/or UART, and/or initiate ADC conversions. While Timer 0 is operating in Mode 3, Timer 1 run control is handled through its mode settings. To run Timer 1 while Timer 0 is in Mode 3, set the Timer 1 Mode as 0, 1, or 2. To disable Timer 1, configure it for Mode 3.

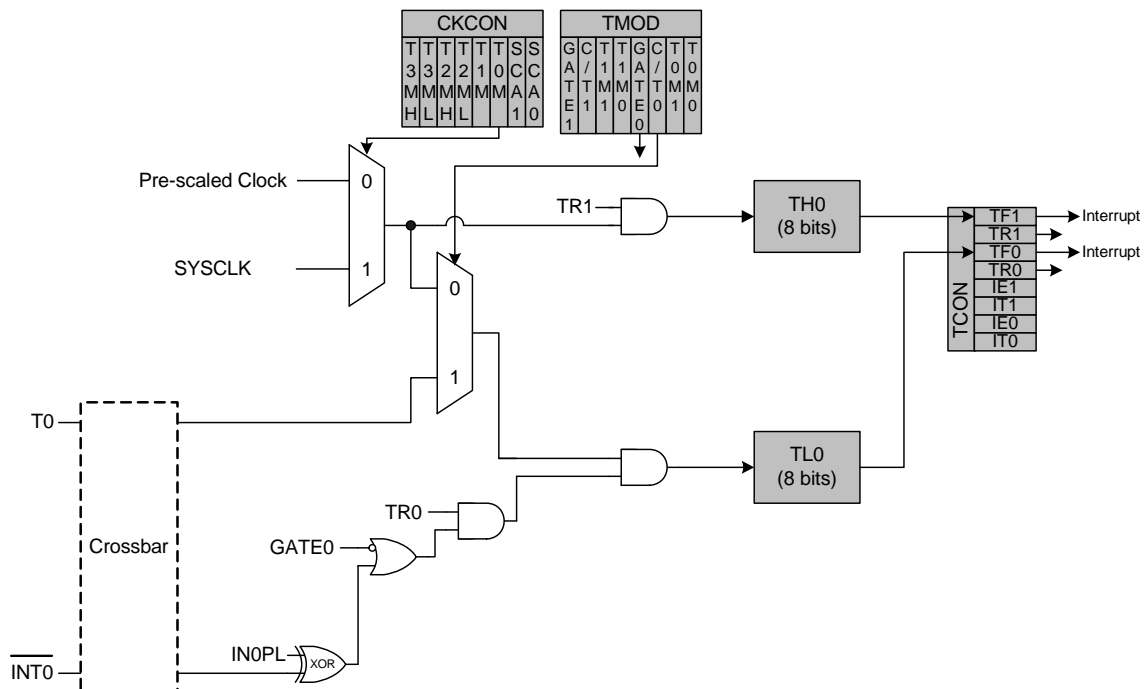


Figure 25.3. T0 Mode 3 Block Diagram

## SFR Definition 25.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x8C

Bit	Name	Function
7:0	TH0[7:0]	<b>Timer 0 High Byte.</b> The TH0 register is the high byte of the 16-bit Timer 0.

## SFR Definition 25.7. TH1: Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x8D

Bit	Name	Function
7:0	TH1[7:0]	<b>Timer 1 High Byte.</b> The TH1 register is the high byte of the 16-bit Timer 1.

## 25.2.3. Comparator 0/SmaRTClock Capture Mode

The Capture Mode in Timer 2 allows either Comparator 0 or the SmaRTClock period to be measured against the system clock or the system clock divided by 12. Comparator 0 and the SmaRTClock period can also be compared against each other. Timer 2 Capture Mode is enabled by setting TF2CEN to 1. Timer 2 should be in 16-bit auto-reload mode when using Capture Mode.

When Capture Mode is enabled, a capture event will be generated either every Comparator 0 rising edge or every 8 SmaRTClock clock cycles, depending on the T2XCLK1 setting. When the capture event occurs, the contents of Timer 2 (TMR2H:TMR2L) are loaded into the Timer 2 reload registers (TMR2RLH:TMR2RLL) and the TF2H flag is set (triggering an interrupt if Timer 2 interrupts are enabled). By recording the difference between two successive timer capture values, the Comparator 0 or SmaRTClock period can be determined with respect to the Timer 2 clock. The Timer 2 clock should be much faster than the capture clock to achieve an accurate reading.

For example, if T2ML = 1b, T2XCLK1 = 0b, and TF2CEN = 1b, Timer 2 will clock every SYSCLK and capture every SmaRTClock clock divided by 8. If the SYSCLK is 24.5 MHz and the difference between two successive captures is 5984, then the SmaRTClock clock is as follows:

$$24.5 \text{ MHz} / (5984 / 8) = 0.032754 \text{ MHz or } 32.754 \text{ kHz.}$$

This mode allows software to determine the exact SmaRTClock frequency in self-oscillate mode and the time between consecutive Comparator 0 rising edges, which is useful for detecting changes in the capacitance of a Touch Sense Switch.

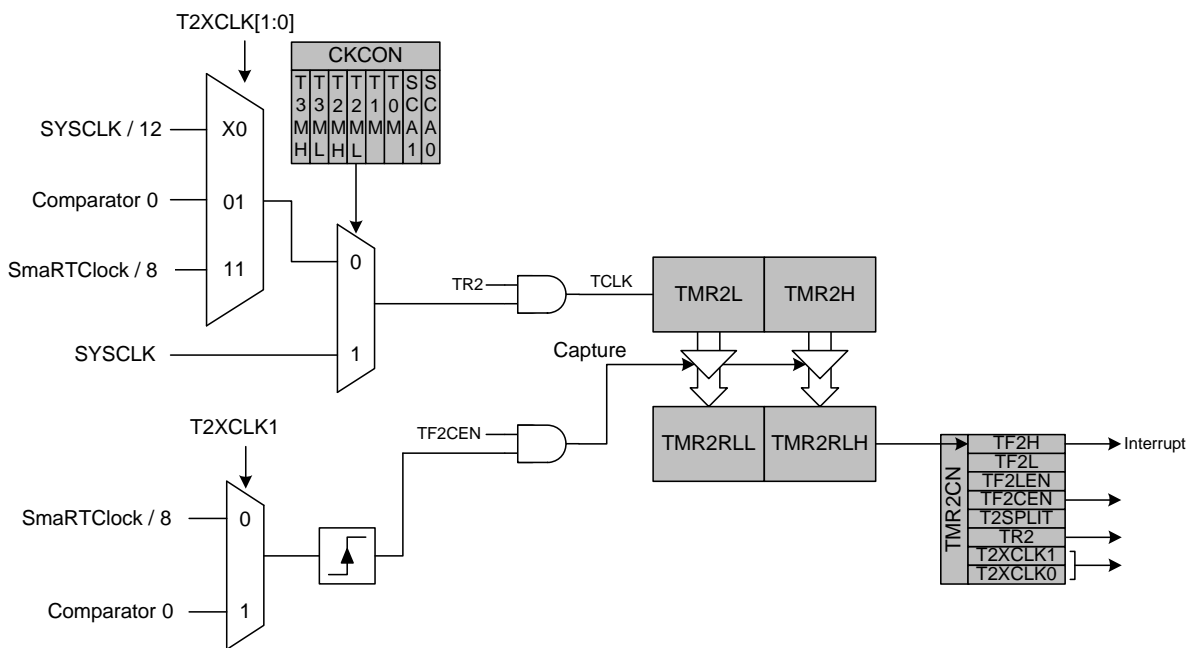
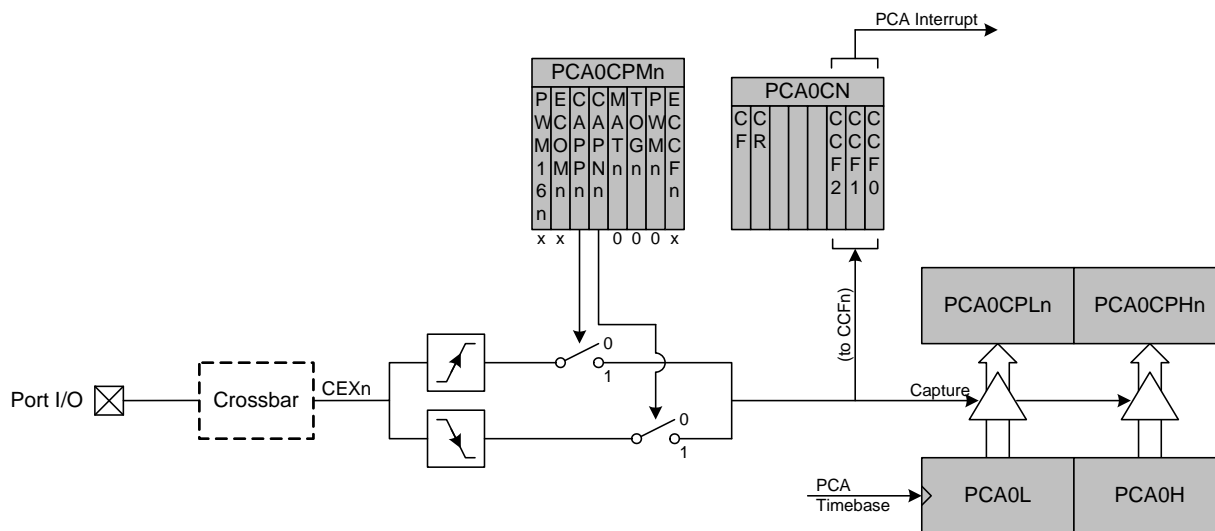


Figure 25.6. Timer 2 Capture Mode Block Diagram

## 26.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEX<sub>n</sub> pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPL<sub>n</sub> and PCA0CPH<sub>n</sub>). The CAPP<sub>n</sub> and CAPN<sub>n</sub> bits in the PCA0CPM<sub>n</sub> register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCF<sub>n</sub>) in PCA0CN is set to logic 1. An interrupt request is generated if the CCF<sub>n</sub> interrupt for that module is enabled. The CCF<sub>n</sub> bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPP<sub>n</sub> and CAPN<sub>n</sub> bits are set to logic 1, then the state of the Port pin associated with CEX<sub>n</sub> can be read directly to determine whether a rising-edge or falling-edge caused the capture.



**Figure 26.4. PCA Capture Mode Diagram**

**Note:** The CEX<sub>n</sub> input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.