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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I <sup>2</sup> C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/c8051f981-gmr">https://www.e-xfl.com/product-detail/silicon-labs/c8051f981-gmr</a>

# C8051F99x-C8051F98x

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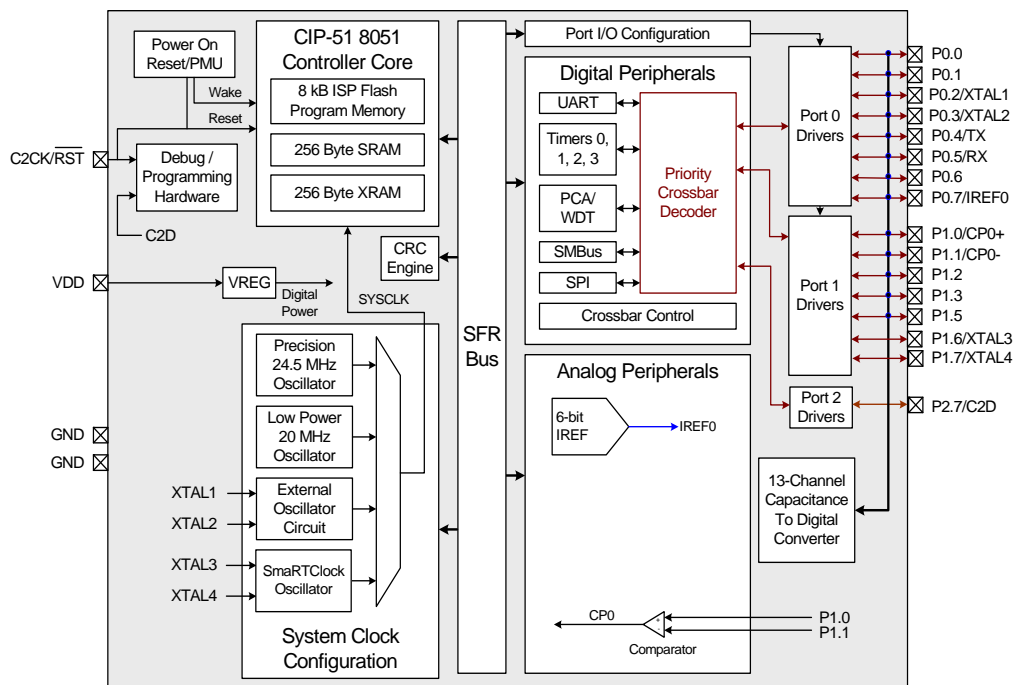


Figure 1.11. C8051F991 Block Diagram

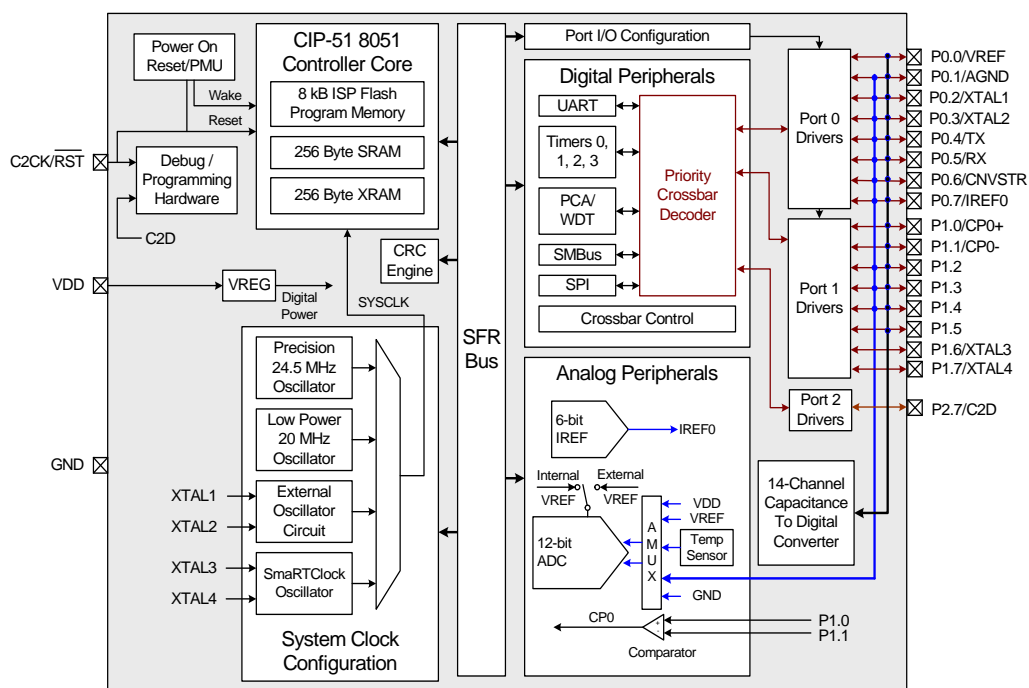
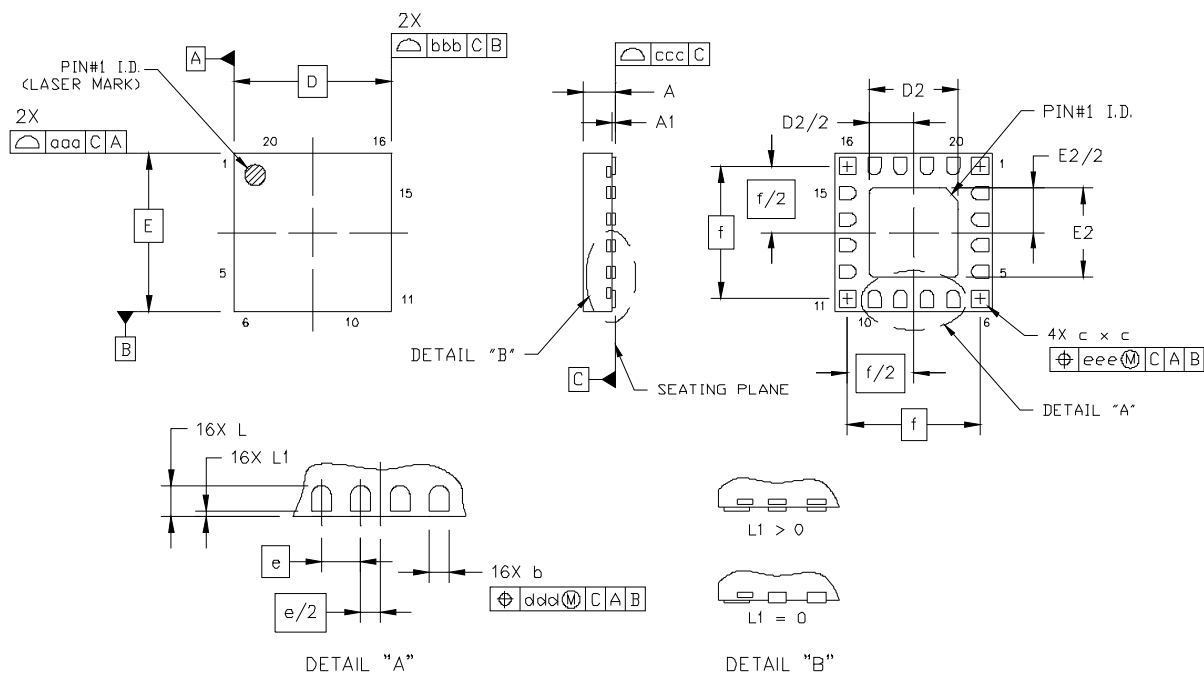


Figure 1.12. C8051F996 Block Diagram

# C8051F99x-C8051F98x



**Figure 3.7. QFN-20 Package Drawing**

**Table 3.2. QFN-20 Package Dimensions**

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.50	0.55	0.60	f	2.53 BSC		
A1	0.00	0.02	0.05	L	0.35	0.40	0.45
b	0.20	0.25	0.30	L1	0.00	—	0.10
c	0.27	0.32	0.375	aaa	—	—	0.05
D	3.00 BSC			bbb	—	—	0.05
D2	1.6	1.70	1.8	ccc		—	0.08
e	0.50 BSC			ddd	—	—	0.10
E	3.00 BSC			eee	—	—	0.10
E2	1.6	1.70	1.8				
<b>Notes:</b>							
1. All dimensions shown are in millimeters (mm) unless otherwise noted.							
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.							

**Table 3.5. PCB Land Pattern**

Dimension	MIN	MAX
C1	3.90	4.00
C2	3.90	4.00
E	0.50 BSC	
X1	0.20	0.30
X2	2.70	2.80
Y1	0.65	0.75
Y2	2.70	2.80

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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**Table 4.3. Port I/O DC Electrical Characteristics**

$V_{DD} = 1.8$  to  $3.6$  V,  $-40$  to  $+85$  °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	High Drive Strength, PnDRV.n = 1				V
	IOH = $-3$ mA, Port I/O push-pull	$V_{DD} - 0.7$	—	—	
	IOH = $-10$ $\mu$ A, Port I/O push-pull	$V_{DD} - 0.1$	—	—	
	IOH = $-10$ mA, Port I/O push-pull		See Chart		
	Low Drive Strength, PnDRV.n = 0				
	IOH = $-1$ mA, Port I/O push-pull	$V_{DD} - 0.7$	—	—	
Output Low Voltage	IOH = $-10$ $\mu$ A, Port I/O push-pull	$V_{DD} - 0.1$	—	—	
	IOH = $-3$ mA, Port I/O push-pull	—	See Chart	—	
	High Drive Strength, PnDRV.n = 1				V
	I <sub>OL</sub> = $8.5$ mA	—	—	0.6	
	I <sub>OL</sub> = $10$ $\mu$ A	—	—	0.1	
	I <sub>OL</sub> = $25$ mA	—	See Chart	—	
Input High Voltage	Low Drive Strength, PnDRV.n = 0				
	I <sub>OL</sub> = $1.4$ mA	—	—	0.6	
	I <sub>OL</sub> = $10$ $\mu$ A	—	—	0.1	
	I <sub>OL</sub> = $4$ mA	—	See Chart	—	
	$V_{DD} = 2.0$ to $3.6$ V	$V_{DD} - 0.6$	—	—	V
	$V_{DD} = 0.9$ to $2.0$ V	$0.7 \times V_{DD}$	—	—	V
Input Low Voltage	$V_{DD} = 2.0$ to $3.6$ V	—	—	0.6	V
	$V_{DD} = 0.9$ to $2.0$ V	—	—	$0.3 \times V_{DD}$	V
Input Leakage Current	Weak Pullup Off	—	—	$\pm 1$	$\mu$ A
	Weak Pullup On, $V_{IN} = 0$ V, $V_{DD} = 1.8$ V	—	4	—	
	Weak Pullup On, $V_{in} = 0$ V, $V_{DD} = 3.6$ V	—	20	35	

## 5. SAR ADC with 16-bit Auto-Averaging Accumulator and Autonomous Low Power Burst Mode

The ADC0 on C8051F980/6 and C8051F990/6 devices is a 300 kps, 10-bit or 75 kps, 12-bit successive-approximation-register (SAR) ADC with integrated track-and-hold and programmable window detector. ADC0 also has an autonomous low power Burst Mode which can automatically enable ADC0, capture and accumulate samples, then place ADC0 in a low power shutdown mode without CPU intervention. It also has a 16-bit accumulator that can automatically oversample and average the ADC results. See Section 5.4 for more details on using the ADC in 12-bit mode. C8051F982 and C8051F988 devices only support the 10-bit mode.

The ADC is fully configurable under software control via Special Function Registers. The ADC0 operates in Single-ended mode and may be configured to measure various different signals using the analog multiplexer described in “5.7. ADC0 Analog Multiplexer” on page 83. The voltage reference for the ADC is selected as described in “5.9. Voltage and Ground Reference Options” on page 88.

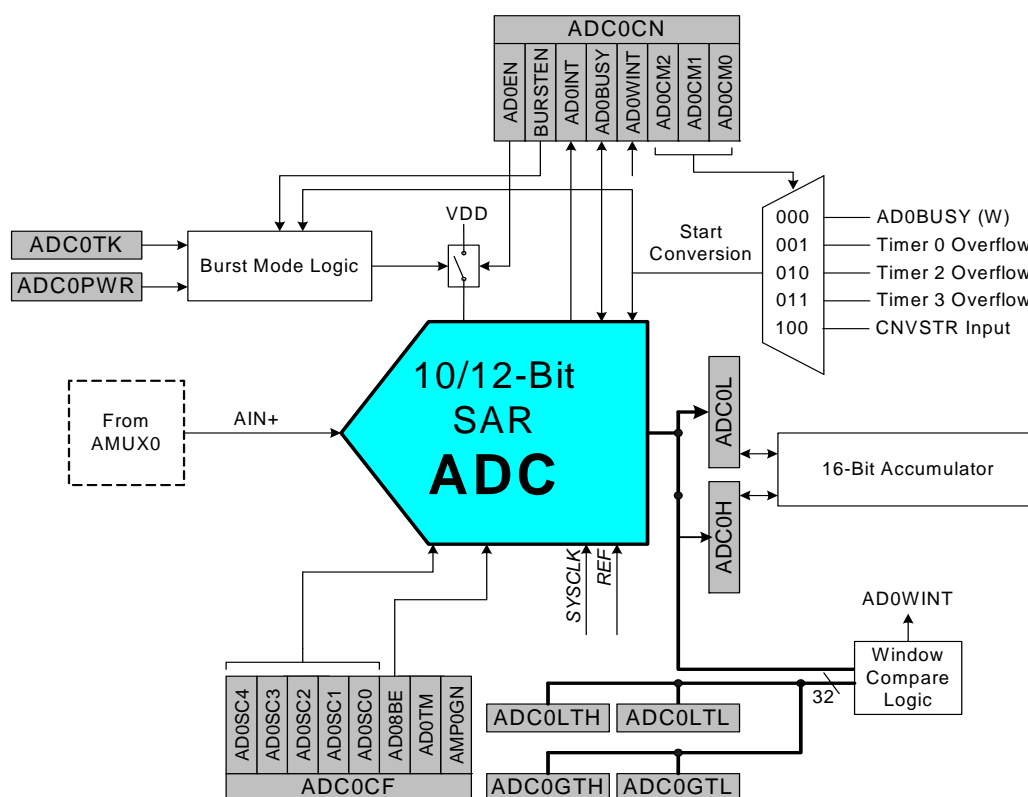


Figure 5.1. ADC0 Functional Block Diagram

## SFR Definition 7.1. CPT0CN: Comparator 0 Control

Bit	7	6	5	4	3	2	1	0
Name	CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0HYP[1:0]		CP0HYN[1:0]	
Type	R/W	R	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0x9B

Bit	Name	Function
7	CP0EN	<b>Comparator0 Enable Bit.</b> 0: Comparator0 Disabled. 1: Comparator0 Enabled.
6	CP0OUT	<b>Comparator0 Output State Flag.</b> 0: Voltage on CP0+ < CP0−. 1: Voltage on CP0+ > CP0−.
5	CP0RIF	<b>Comparator0 Rising-Edge Flag. Must be cleared by software.</b> 0: No Comparator0 Rising Edge has occurred since this flag was last cleared. 1: Comparator0 Rising Edge has occurred.
4	CP0FIF	<b>Comparator0 Falling-Edge Flag. Must be cleared by software.</b> 0: No Comparator0 Falling-Edge has occurred since this flag was last cleared. 1: Comparator0 Falling-Edge has occurred.
3-2	CP0HYP[1:0]	<b>Comparator0 Positive Hysteresis Control Bits.</b> 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = Hysteresis 1. 10: Positive Hysteresis = Hysteresis 2. 11: Positive Hysteresis = Hysteresis 3 (Maximum).
1:0	CP0HYN[1:0]	<b>Comparator0 Negative Hysteresis Control Bits.</b> 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = Hysteresis 1. 10: Negative Hysteresis = Hysteresis 2. 11: Negative Hysteresis = Hysteresis 3 (Maximum).



## SFR Definition 8.3. CS0DH: Capacitive Sense Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	CS0DH[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xEE

Bit	Name	Description
7:0	CS0DH	<b>CS0 Data High Byte.</b> Stores the high byte of the last completed 16-bit Capacitive Sense conversion.

## SFR Definition 8.4. CS0DL: Capacitive Sense Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	CS0DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xED

Bit	Name	Description
7:0	CS0DL	<b>CS0 Data Low Byte.</b> Stores the low byte of the last completed 16-bit Capacitive Sense conversion.

# C8051F99x-C8051F98x

## 10. Memory Organization

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory organization of the C8051F99x-C8051F98x device family is shown in Figure 10.1.

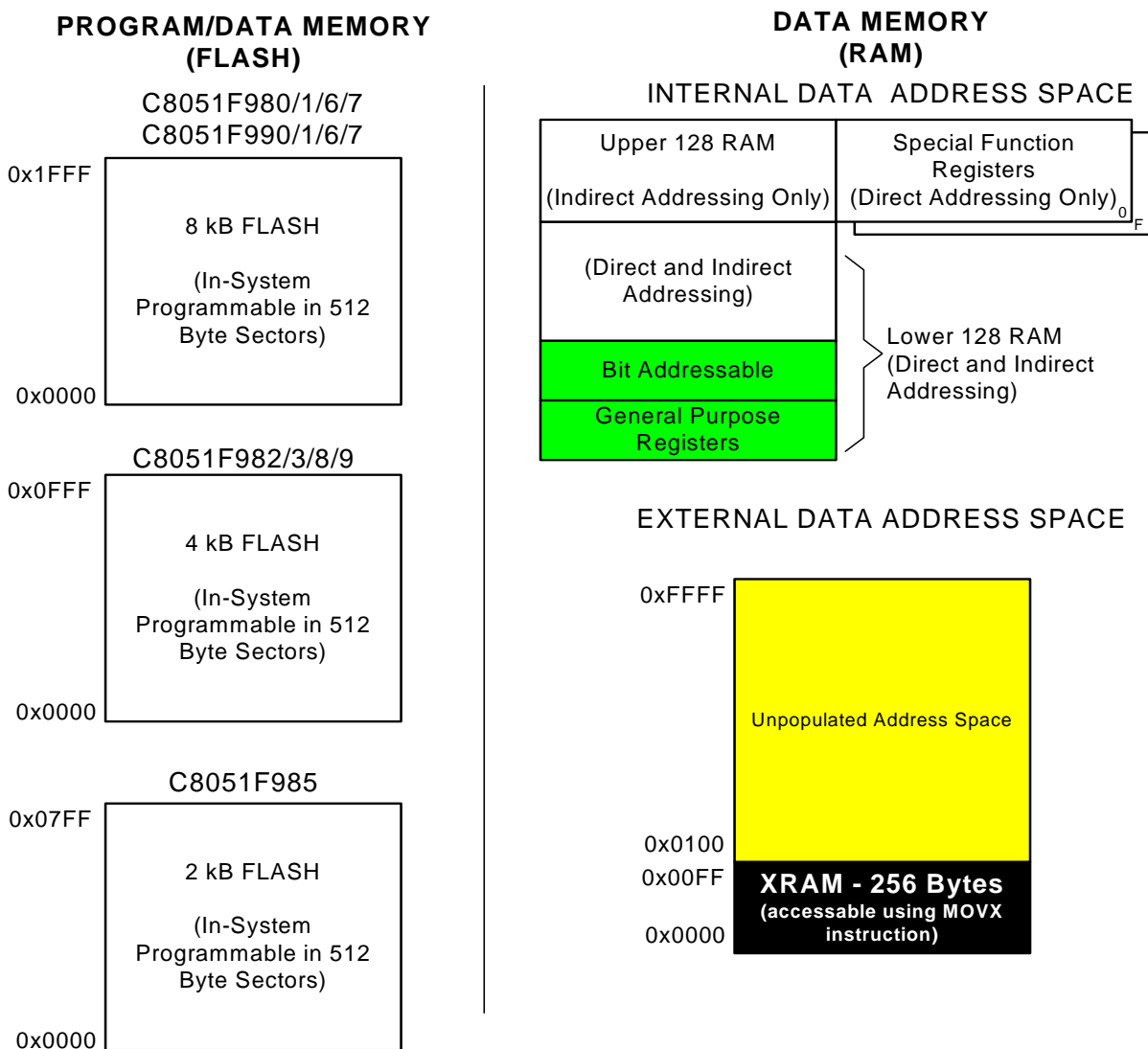


Figure 10.1. C8051F99x-C8051F98x Memory Map

**SFR Definition 13.2. IP: Interrupt Priority**

Bit	7	6	5	4	3	2	1	0
Name		PSPI0	PT2	PS0	PT1	PX1	PT0	PX0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0xB8; Bit-Addressable

Bit	Name	Function
7	Unused	Read = 1b, Write = don't care.
6	PSPI0	<b>Serial Peripheral Interface (SPI0) Interrupt Priority Control.</b> This bit sets the priority of the SPI0 interrupt. 0: SPI0 interrupt set to low priority level. 1: SPI0 interrupt set to high priority level.
5	PT2	<b>Timer 2 Interrupt Priority Control.</b> This bit sets the priority of the Timer 2 interrupt. 0: Timer 2 interrupt set to low priority level. 1: Timer 2 interrupt set to high priority level.
4	PS0	<b>UART0 Interrupt Priority Control.</b> This bit sets the priority of the UART0 interrupt. 0: UART0 interrupt set to low priority level. 1: UART0 interrupt set to high priority level.
3	PT1	<b>Timer 1 Interrupt Priority Control.</b> This bit sets the priority of the Timer 1 interrupt. 0: Timer 1 interrupt set to low priority level. 1: Timer 1 interrupt set to high priority level.
2	PX1	<b>External Interrupt 1 Priority Control.</b> This bit sets the priority of the External Interrupt 1 interrupt. 0: External Interrupt 1 set to low priority level. 1: External Interrupt 1 set to high priority level.
1	PT0	<b>Timer 0 Interrupt Priority Control.</b> This bit sets the priority of the Timer 0 interrupt. 0: Timer 0 interrupt set to low priority level. 1: Timer 0 interrupt set to high priority level.
0	PX0	<b>External Interrupt 0 Priority Control.</b> This bit sets the priority of the External Interrupt 0 interrupt. 0: External Interrupt 0 set to low priority level. 1: External Interrupt 0 set to high priority level.

**SFR Definition 13.6. EIP2: Extended Interrupt Priority 2**

Bit	7	6	5	4	3	2	1	0
Name		PCSEOS	PCSDC	PCSCPT		PRTC0F	PMAT	PWARN
Type	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0xF7

Bit	Name	Function
7	Unused	Read = 0b. Write = Don't care.
6	PCSEOS	<b>Capacitive Sense End of Scan Interrupt Priority Control.</b> 0: Capacitive Sense End of Scan interrupt set to low priority level. 1: Capacitive Sense End of Scan interrupt set to high priority level.
5	PCSDC	<b>Capacitive Sense Digital Comparator Interrupt Priority Control.</b> 0: Capacitive Sense Digital Comparator interrupt set to low priority level. 1: Capacitive Sense Digital Comparator interrupt set to high priority level.
4	PCSCPT	<b>Capacitive Sense Conversion Complete Interrupt Priority Control.</b> 0: Capacitive Sense Conversion Complete interrupt set to low priority level. 1: Capacitive Sense Conversion Complete interrupt set to high priority level.
3	Unused	Read = 0b. Write = Don't care.
2	PRTC0F	<b>SmaRTClock Oscillator Fail Interrupt Priority Control.</b> This bit sets the priority of the SmaRTClock Alarm interrupt. 0: SmaRTClock Alarm interrupt set to low priority level. 1: SmaRTClock Alarm interrupt set to high priority level.
1	PMAT	<b>Port Match Interrupt Priority Control.</b> This bit sets the priority of the Port Match Event interrupt. 0: Port Match interrupt set to low priority level. 1: Port Match interrupt set to high priority level.
0	PWARN	<b>Supply Monitor Early Warning Interrupt Priority Control.</b> This bit sets the priority of the Supply Monitor Early Warning interrupt. 0: Supply Monitor Early Warning interrupt set to low priority level. 1: Supply Monitor Early Warning interrupt set to high priority level.

## 15.4. Suspend Mode

Setting the Suspend Mode Select bit (PMU0CF.6) causes the system clock to be gated off and all internal oscillators disabled. The system clock source must be set to the low power internal oscillator or the precision oscillator prior to entering Suspend Mode. All digital logic (timers, communication peripherals, interrupts, CPU, etc.) stops functioning until one of the enabled wake-up sources occurs.

The following wake-up sources can be configured to wake the device from Suspend Mode:

- CS0 End of Conversion or End of Scan
- SmaRTClock Oscillator Fail
- SmaRTClock Alarm
- Port Match Event
- Comparator0 Rising Edge

**Note:** Upon wake-up from suspend mode, PMU0 requires two system clocks in order to update the PMU0CF wake-up flags. All flags will read back a value of '0' during the first two system clocks following a wake-up from suspend mode.

In addition, a noise glitch on  $\overline{\text{RST}}$  that is not long enough to reset the device will cause the device to exit suspend. In order for the MCU to respond to the pin reset event, software must not place the device back into suspend mode for a period of 15  $\mu\text{s}$ . The PMU0CF register may be checked to determine if the wake-up was due to a falling edge on the  $\overline{\text{RST}}$  pin. If the wake-up source is not due to a falling edge on  $\overline{\text{RST}}$ , there is no time restriction on how soon software may place the device back into suspend mode. A 4.7 k $\Omega$  pullup resistor to VDD is recommended for RST to prevent noise glitches from waking the device.

## 15.5. Sleep Mode

Setting the Sleep Mode Select bit (PMU0CF.7) turns off the internal 1.8 V regulator (VREG0) and switches the power supply of all on-chip RAM to the VDD pin (see Figure 15.1). Power to most digital logic on the chip is disconnected; only PMU0 and the SmaRTClock remain powered. Analog peripherals remain powered in two-cell mode. Only the Comparators remain functional when the device enters Sleep Mode. All other analog peripherals (CS0, ADC0, IREF0, External Oscillator, etc.) should be disabled prior to entering Sleep Mode. The system clock source must be set to the low power internal oscillator prior to entering Sleep Mode.

**Important Note:** The precision internal oscillator may potentially lock up after exiting Sleep mode. Systems using Sleep Mode should switch to the low power oscillator prior to entering Sleep Mode:

1. Switch the system clock to the low power oscillator (CLKSEL = 0x04).
2. Turn off the Precision Oscillator (OSCICN &= ~0x80).
3. Enter Sleep.
4. Exit Sleep.
5. Turn on the Precision Oscillator (OSCICN |= 0x80).
6. Switch the system clock to the Precision Oscillator (CLKSEL = 0x00).

GPIO pins configured as digital outputs will retain their output state during sleep mode. In two-cell mode, they will maintain the same current drive capability in sleep mode as they have in normal mode.

GPIO pins configured as digital inputs can be used during sleep mode as wakeup sources using the port match feature. In two-cell mode, they will maintain the same input level specs in sleep mode as they have in normal mode.

C8051F99x-C8051F98x devices support a wakeup request for external devices. Upon exit from sleep mode, the wake-up request signal is driven low, allowing other devices in the system to wake up from their low power modes.

## 19.1. Programmable Precision Internal Oscillator

All C8051F99x-C8051F98x devices include a programmable precision internal oscillator that may be selected as the system clock. OSCICL is factory calibrated to obtain a 24.5 MHz frequency. See Section “4. Electrical Characteristics” on page 48 for complete oscillator specifications.

The precision oscillator supports a spread spectrum mode which modulates the output frequency in order to reduce the EMI generated by the system. When enabled ( $SSE = 1$ ), the oscillator output frequency is modulated by a stepped triangle wave whose frequency is equal to the oscillator frequency divided by 384 (63.8 kHz using the factory calibration). The deviation from the nominal oscillator frequency is +0%, -1.6%, and the step size is typically 0.26% of the nominal frequency. When using this mode, the typical average oscillator frequency is lowered from 24.5 MHz to 24.3 MHz.

**Important Note:** The precision internal oscillator may potentially lock up after exiting Sleep mode. Systems using Sleep Mode should switch to the low power oscillator prior to entering Sleep Mode:

1. Switch the system clock to the low power oscillator ( $CLKSEL = 0x04$ ).
2. Turn off the Precision Oscillator ( $OSCICN \&= \sim 0x80$ ).
3. Enter Sleep.
4. Exit Sleep.
5. Turn on the Precision Oscillator ( $OSCICN |= 0x80$ ).
6. Switch the system clock to the Precision Oscillator ( $CLKSEL = 0x00$ ).

## 19.2. Low Power Internal Oscillator

All C8051F99x-C8051F98x devices include a low power internal oscillator that defaults as the system clock after a system reset. The low power internal oscillator frequency is  $20 \text{ MHz} \pm 10\%$  and is automatically enabled when selected as the system clock and disabled when not in use. See Section “4. Electrical Characteristics” on page 48 for complete oscillator specifications.

## 19.3. External Oscillator Drive Circuit

All C8051F99x-C8051F98x devices include an external oscillator circuit that may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. Figure 19.1 shows a block diagram of the four external oscillator options. The external oscillator is enabled and configured using the OSCXCN register.

The external oscillator output may be selected as the system clock or used to clock some of the digital peripherals (e.g., Timers, PCA, etc.). See the data sheet chapters for each digital peripheral for details. See Section “4. Electrical Characteristics” on page 48 for complete oscillator specifications.

### 19.3.1. External Crystal Mode

If a crystal or ceramic resonator is used as the external oscillator, the crystal/resonator and a  $10 \text{ M}\Omega$  resistor must be wired across the XTAL1 and XTAL2 pins as shown in Figure 19.1, Option 1. Appropriate loading capacitors should be added to XTAL1 and XTAL2, and both pins should be configured for analog I/O with the digital output drivers disabled.

Figure 19.2 shows the external oscillator circuit for a 20 MHz quartz crystal with a manufacturer recommended load capacitance of 12.5 pF. Loading capacitors are “in series” as seen by the crystal and “in parallel” with the stray capacitance of the XTAL1 and XTAL2 pins. The total value of the each loading capacitor and the stray capacitance of each XTAL pin should equal  $12.5 \text{ pF} \times 2 = 25 \text{ pF}$ . With a stray capacitance of 10 pF per pin, the 15 pF capacitors yield an equivalent series capacitance of 12.5 pF across the crystal.

**Note:** The recommended load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal data sheet when completing these calculations.

## Internal Register Definition 20.5. RTC0XCN: SmaRTClock Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	AGCEN	XMODE	BIASX2	CLKVLD	LFOEN			
Type	R/W	R/W	R/W	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SmaRTClock Address = 0x05

Bit	Name	Function
7	AGCEN	<b>SmaRTClock Oscillator Automatic Gain Control (AGC) Enable.</b> 0: AGC disabled. 1: AGC enabled.
6	XMODE	<b>SmaRTClock Oscillator Mode.</b> Selects Crystal or Self Oscillate Mode. 0: Self-Oscillate Mode selected. 1: Crystal Mode selected.
5	BIASX2	<b>SmaRTClock Oscillator Bias Double Enable.</b> <b>Enables/disables the Bias Double feature.</b> 0: Bias Double disabled. 1: Bias Double enabled.
4	CLKVLD	<b>SmaRTClock Oscillator Crystal Valid Indicator.</b> Indicates if oscillation amplitude is sufficient for maintaining oscillation. 0: Oscillation has not started or oscillation amplitude is too low to maintain oscillation. 1: Sufficient oscillation amplitude detected.
3	LFOEN	<b>Low Frequency Oscillator Enable and Select.</b> Overrides XMODE and selects the internal low frequency oscillator (LFO) as the SmaRTClock oscillator source. 0: XMODE determines SmaRTClock oscillator source. 1: LFO enabled and selected as SmaRTClock oscillator source.
2:0	Unused	Read = 000b; Write = Don't Care.

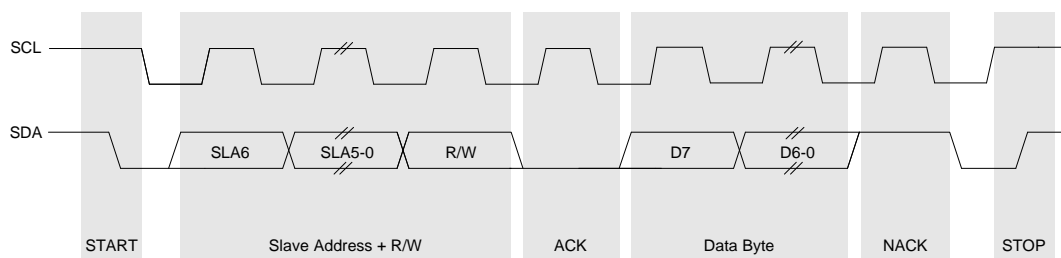
## 22.3. SMBus Operation

Two types of data transfers are possible: data transfers from a master transmitter to an addressed slave receiver (WRITE), and data transfers from an addressed slave transmitter to a master receiver (READ). The master device initiates both types of data transfers and provides the serial clock pulses on SCL. The SMBus interface may operate as a master or a slave, and multiple master devices on the same bus are supported. If two or more masters attempt to initiate a data transfer simultaneously, an arbitration scheme is employed with a single master always winning the arbitration. Note that it is not necessary to specify one device as the Master in a system; any device who transmits a START and a slave address becomes the master for the duration of that transfer.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Bytes that are received (by a master or slave) are acknowledged (ACK) with a low SDA during a high SCL (see Figure 22.3). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

The direction bit (R/W) occupies the least-significant bit position of the address byte. The direction bit is set to logic 1 to indicate a "READ" operation and cleared to logic 0 to indicate a "WRITE" operation.

All transactions are initiated by a master, with one or more addressed slave devices as the target. The master generates the START condition and then transmits the slave address and direction bit. If the transaction is a WRITE operation from the master to the slave, the master transmits the data a byte at a time waiting for an ACK from the slave at the end of each byte. For READ operations, the slave transmits the data waiting for an ACK from the master at the end of each byte. At the end of the data transfer, the master generates a STOP condition to terminate the transaction and free the bus. Figure 22.3 illustrates a typical SMBus transaction.



**Figure 22.3. SMBus Transaction**

### 22.3.1. Transmitter vs. Receiver

On the SMBus communications interface, a device is the "transmitter" when it is sending an address or data byte to another device on the bus. A device is a "receiver" when an address or data byte is being sent to it from another device on the bus. The transmitter controls the SDA line during the address or data byte. After each byte of address or data information is sent by the transmitter, the receiver sends an ACK or NACK bit during the ACK phase of the transfer, during which time the receiver controls the SDA line.



**SFR Definition 23.1. SCON0: Serial Port 0 Control**

Bit	7	6	5	4	3	2	1	0
Name	S0MODE		MCE0	REN0	TB80	RB80	TI0	RI0
Type	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x98; Bit-Addressable

Bit	Name	Function
7	S0MODE	<b>Serial Port 0 Operation Mode.</b> Selects the UART0 Operation Mode. 0: 8-bit UART with Variable Baud Rate. 1: 9-bit UART with Variable Baud Rate.
6	Unused	Read = 1b. Write = Don't Care.
5	MCE0	<b>Multiprocessor Communication Enable.</b> <b>For Mode 0 (8-bit UART): Checks for valid stop bit.</b> 0: Logic level of stop bit is ignored. 1: RI0 will only be activated if stop bit is logic level 1. <b>For Mode 1 (9-bit UART): Multiprocessor Communications Enable.</b> 0: Logic level of ninth bit is ignored. 1: RI0 is set and an interrupt is generated only when the ninth bit is logic 1.
4	REN0	<b>Receive Enable.</b> 0: UART0 reception disabled. 1: UART0 reception enabled.
3	TB80	<b>Ninth Transmission Bit.</b> The logic level of this bit will be sent as the ninth transmission bit in 9-bit UART Mode (Mode 1). Unused in 8-bit mode (Mode 0).
2	RB80	<b>Ninth Receive Bit.</b> RB80 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.
1	TI0	<b>Transmit Interrupt Flag.</b> Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.
0	RI0	<b>Receive Interrupt Flag.</b> Set to 1 by hardware when a byte of data has been received by UART0 (set at the STOP bit sampling time). When the UART0 interrupt is enabled, setting this bit to 1 causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from all ones to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

## SFR Definition 25.11. TMR2L: Timer 2 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xCC

Bit	Name	Function
7:0	TMR2L[7:0]	<b>Timer 2 Low Byte.</b> In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

## SFR Definition 25.12. TMR2H Timer 2 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xCD

Bit	Name	Function
7:0	TMR2H[7:0]	<b>Timer 2 High Byte.</b> In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8-bit mode, TMR2H contains the 8-bit high byte timer value.

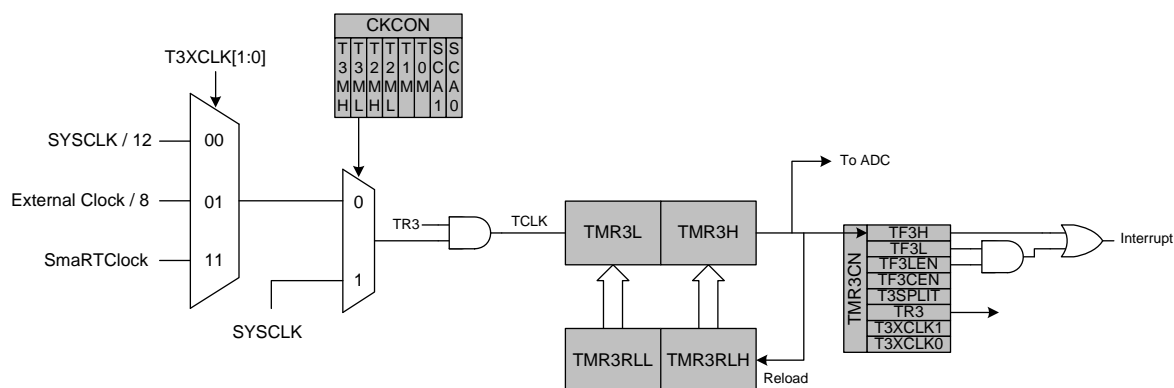
## 25.3. Timer 3

Timer 3 is a 16-bit timer formed by two 8-bit SFRs: TMR3L (low byte) and TMR3H (high byte). Timer 3 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T3SPLIT bit (TMR3CN.3) defines the Timer 3 operation mode. Timer 3 can also be used in Capture Mode to measure the external oscillator source or the SmartClock oscillator period with respect to another oscillator.

Timer 3 may be clocked by the system clock, the system clock divided by 12, external oscillator source divided by 8, or the SmartClock oscillator. The external oscillator source divided by 8 and SmartClock oscillator is synchronized with the system clock.

### 25.3.1. 16-bit Timer with Auto-Reload

When T3SPLIT (TMR3CN.3) is zero, Timer 3 operates as a 16-bit timer with auto-reload. Timer 3 can be clocked by SYSCLK, SYSCLK divided by 12, external oscillator clock source divided by 8, or SmartClock oscillator. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 3 reload registers (TMR3RLH and TMR3RLL) is loaded into the Timer 3 register as shown in Figure 25.7, and the Timer 3 High Byte Overflow Flag (TMR3CN.7) is set. If Timer 3 interrupts are enabled (if EIE1.7 is set), an interrupt will be generated on each Timer 3 overflow. Additionally, if Timer 3 interrupts are enabled and the TF3LEN bit is set (TMR3CN.5), an interrupt will be generated each time the lower 8 bits (TMR3L) overflow from 0xFF to 0x00.



**Figure 25.7. Timer 3 16-Bit Mode Block Diagram**

## 25.3.2. 8-Bit Timers with Auto-Reload

When T3SPLIT is set, Timer 3 operates as two 8-bit timers (TMR3H and TMR3L). Both 8-bit timers operate in auto-reload mode as shown in Figure 25.8. TMR3RLL holds the reload value for TMR3L; TMR3RLH holds the reload value for TMR3H. The TR3 bit in TMR3CN handles the run control for TMR3H. TMR3L is always running when configured for 8-bit Mode.

Each 8-bit timer may be configured to use SYSCCLK, SYSCCLK divided by 12, the external oscillator clock source divided by 8, or the SmaRTClock. The Timer 3 Clock Select bits (T3MH and T3ML in CKCON) select either SYSCCLK or the clock defined by the Timer 3 External Clock Select bits (T3XCLK[1:0] in TMR3CN), as follows:

T3MH	T3XCLK[1:0]	TMR3H Clock Source
0	00	SYSCCLK / 12
0	01	SmaRTClock
0	10	Reserved
0	11	External Clock / 8
1	X	SYSCCLK

T3ML	T3XCLK[1:0]	TMR3L Clock Source
0	00	SYSCCLK / 12
0	01	SmaRTClock
0	10	Reserved
0	11	External Clock / 8
1	X	SYSCCLK

The TF3H bit is set when TMR3H overflows from 0xFF to 0x00; the TF3L bit is set when TMR3L overflows from 0xFF to 0x00. When Timer 3 interrupts are enabled, an interrupt is generated each time TMR3H overflows. If Timer 3 interrupts are enabled and TF3LEN (TMR3CN.5) is set, an interrupt is generated each time either TMR3L or TMR3H overflows. When TF3LEN is enabled, software must check the TF3H and TF3L flags to determine the source of the Timer 3 interrupt. The TF3H and TF3L interrupt flags are not cleared by hardware and must be manually cleared by software.

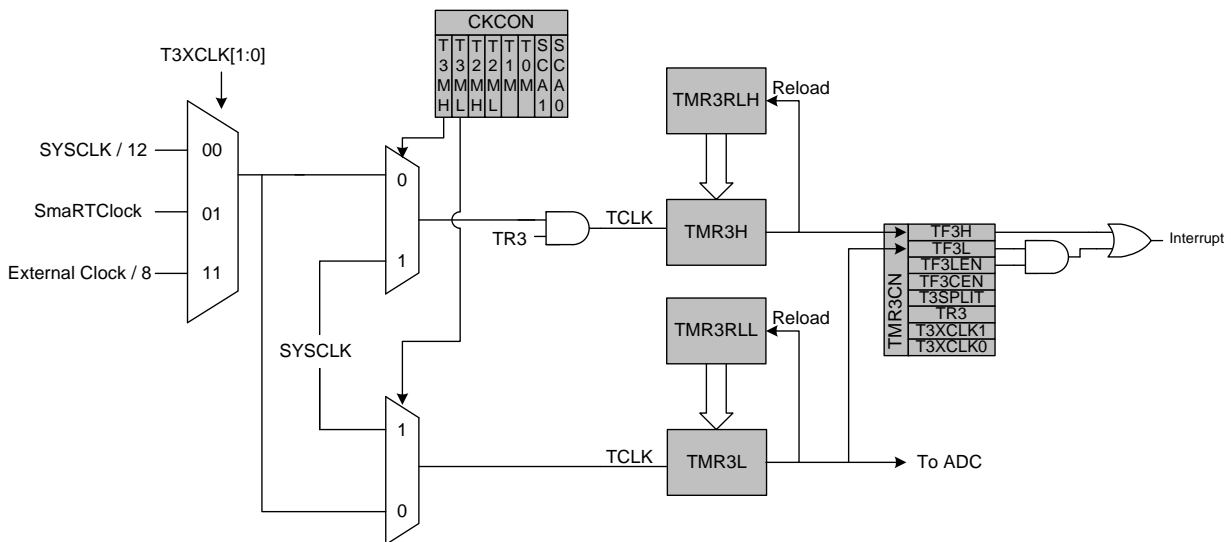


Figure 25.8. Timer 3 8-Bit Mode Block Diagram