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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I <sup>2</sup> C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/c8051f982-c-gm">https://www.e-xfl.com/product-detail/silicon-labs/c8051f982-c-gm</a>

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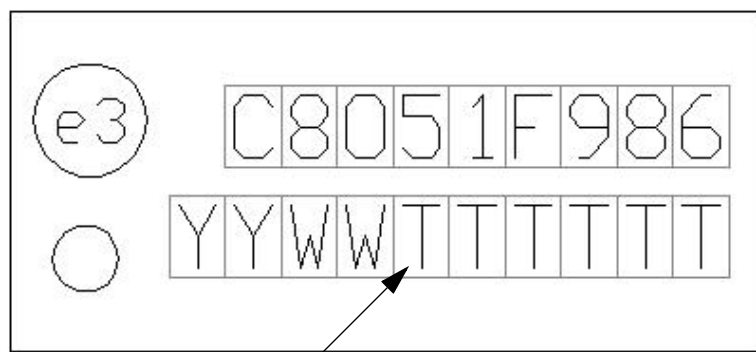
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# C8051F99x-C8051F98x

## 3. Pinout and Package Definitions

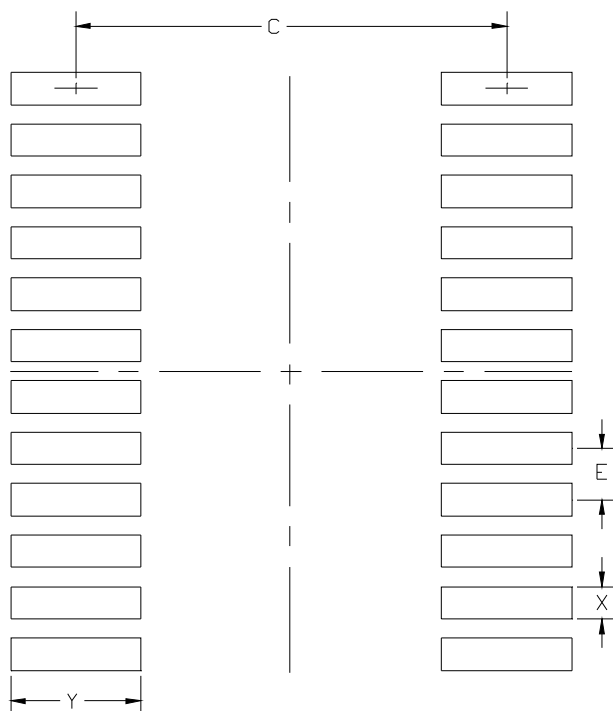
**Table 3.1. Pin Definitions for the C8051F99x-C8051F98x**

Name	Pin Numbers			Type	Description
	'F980/1/2 'F983/5 'F990/1 -GM	'F986/7 'F988/9 'F996/7 -GM	'F986/7 'F988/9 'F996/7 -GU		
V <sub>DD</sub>	4	3	6	P In	Power Supply Voltage. Must be 1.8 to 3.6 V.
GND	3, 12	2	5	G	Required Ground.
$\overline{\text{RST}}$	5	6	9	D I/O	Device Reset. Open-drain output of internal POR or V <sub>DD</sub> monitor. An external source can initiate a system reset by driving this pin low for at least 15 $\mu$ s. A 1 k $\Omega$ to 5 k $\Omega$ pullup to V <sub>DD</sub> is recommended. See Section "18. Reset Sources" on page 181 Section for a complete description.
C2CK				D I/O	Clock signal for the C2 Debug Interface.
P2.7/	6	7	10	D I/O	Port 2.7. This pin can only be used as GPIO. The Crossbar cannot route signals to this pin and it cannot be configured as an analog input. See Port I/O Section for a complete description.
C2D				D I/O	Bi-directional data signal for the C2 Debug Interface.
P1.6/	8	9	12	D I/O	Port 1.6. See Port I/O Section for a complete description.
XTAL3				A In	SmaRTClock Oscillator Crystal Input. See Section 20 for a complete description.
P1.7/	7	8	11	D I/O	Port 1.7. See Port I/O Section for a complete description.
XTAL4				A Out	SmaRTClock Oscillator Crystal Output. See Section 20 for a complete description.
P0.0/	2	24	3	D I/O or A In	Port 0.0. See Port I/O Section for a complete description.
V <sub>REF</sub> *				A In	External V <sub>REF</sub> Input. See Section "5.9. Voltage and Ground Reference Options" on page 88.
*Note: Available only on the C8051F980/2/6/8 and C8051F990/6 devices.					



First character of the trace code identifies the silicon revision

**Figure 3.6. QSOP-24 Package Marking Diagram**



**Figure 3.12. QSOP-24 Landing Diagram**

**Table 3.7. PCB Land Pattern**

Dimension	MIN	MAX
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

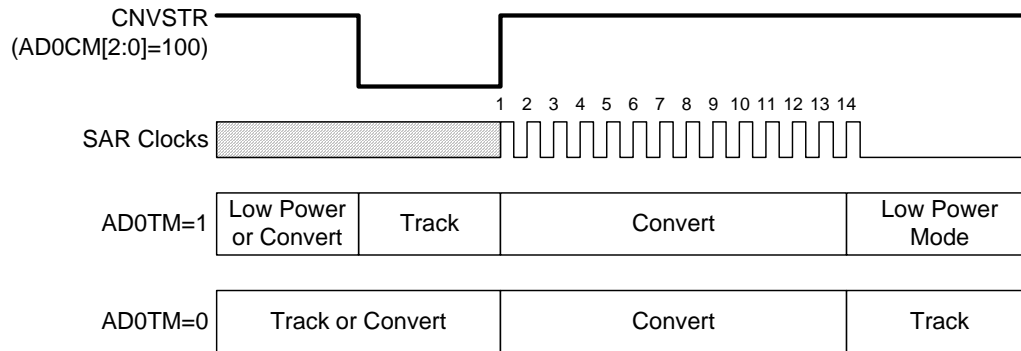
**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 5.2.2. Tracking Modes

Each ADC0 conversion must be preceded by a minimum tracking time in order for the converted result to be accurate. The minimum tracking time is given in Table 4.10. The AD0TM bit in register ADC0CN controls the ADC0 track-and-hold mode. In its default state when Burst Mode is disabled, the ADC0 input is continuously tracked, except when a conversion is in progress. When the AD0TM bit is logic 1, ADC0 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR signal is used to initiate conversions in low-power tracking mode, ADC0 tracks only when CNVSTR is low; conversion begins on the rising edge of CNVSTR (see Figure 5.2). Tracking can also be disabled (shutdown) when the device is in low power standby or sleep modes. Low-power track-and-hold mode is also useful when AMUX settings are frequently changed, due to the settling time requirements described in “5.2.4. Settling Time Requirements” on page 71.

### A. ADC0 Timing for External Trigger Source



### B. ADC0 Timing for Internal Trigger Source

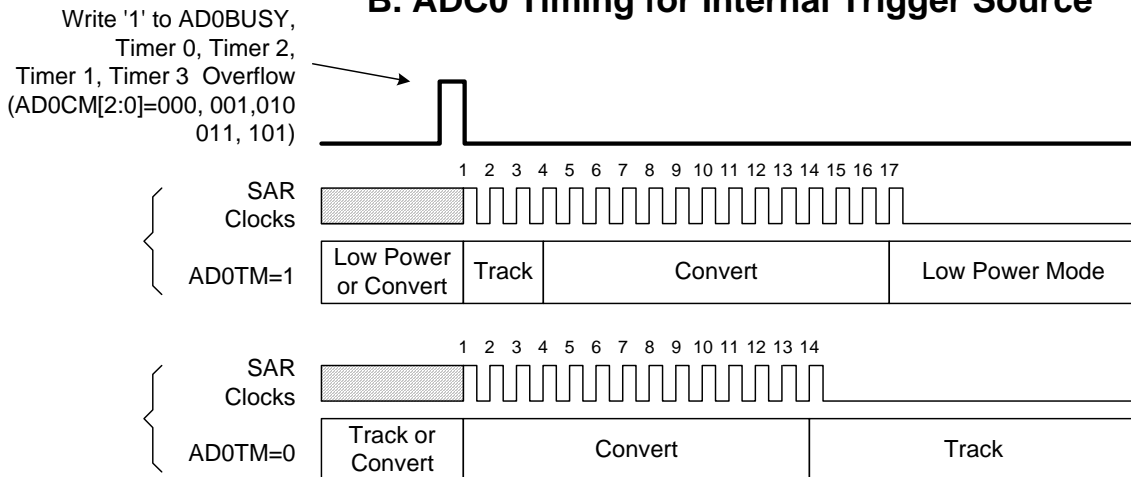


Figure 5.2. 10-Bit ADC Track and Conversion Example Timing (BURSTEN = 0)

# C8051F99x-C8051F98x

## SFR Definition 5.3. ADC0AC: ADC0 Accumulator Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD012BE	AD0AE	AD0SJST[2:0]			AD0RPT[2:0]		
Type	R/W	W	R/W			R/W		
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xBA

Bit	Name	Function
7	AD012BE	<b>ADC0 12-Bit Mode Enable.</b> Enables 12-bit Mode on C8051F980/6 and C8051F990/6 devices. 0: 12-bit Mode Disabled. 1: 12-bit Mode Enabled.
6	AD0AE	<b>ADC0 Accumulate Enable.</b> Enables multiple conversions to be accumulated when burst mode is disabled. 0: ADC0H:ADC0L contain the result of the latest conversion when Burst Mode is disabled. 1: ADC0H:ADC0L contain the accumulated conversion results when Burst Mode is disabled. Software must write 0x0000 to ADC0H:ADC0L to clear the accumulated result. This bit is write-only. Always reads 0b.
5:3	AD0SJST[2:0]	<b>ADC0 Accumulator Shift and Justify.</b> Specifies the format of data read from ADC0H:ADC0L. 000: Right justified. No shifting applied. 001: Right justified. Shifted right by 1 bit. 010: Right justified. Shifted right by 2 bits. 011: Right justified. Shifted right by 3 bits. 100: Left justified. No shifting applied. All remaining bit combinations are reserved.
2:0	AD0RPT[2:0]	<b>ADC0 Repeat Count.</b> Selects the number of conversions to perform and accumulate in Burst Mode. This bit field must be set to 000 if Burst Mode is disabled. 000: Perform and Accumulate 1 conversion. 001: Perform and Accumulate 4 conversions. 010: Perform and Accumulate 8 conversions. 011: Perform and Accumulate 16 conversions. 100: Perform and Accumulate 32 conversions. 101: Perform and Accumulate 64 conversions. All remaining bit combinations are reserved.

## SFR Definition 5.10. ADC0LTH: ADC0 Less-Than High Byte

Bit	7	6	5	4	3	2	1	0
Name	AD0LT[15:8]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC6

Bit	Name	Function
7:0	AD0LT[15:8]	<b>ADC0 Less-Than High Byte.</b> Most Significant Byte of the 16-bit Less-Than window compare register.

## SFR Definition 5.11. ADC0LTL: ADC0 Less-Than Low Byte

Bit	7	6	5	4	3	2	1	0
Name	AD0LT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC5

Bit	Name	Function
7:0	AD0LT[7:0]	<b>ADC0 Less-Than Low Byte.</b> Least Significant Byte of the 16-bit Less-Than window compare register.

**Note:** In 8-bit mode, this register should be set to 0x00.



## 8.9. Automatic Scanning (Method 2—CS0SMEN = 1)

When CS0SMEN is enabled, CS0 uses an alternate autoscanning method that uses the contents of CS0SCAN0 and CS0SCAN1 to determine which channels to include in the scan. This maximizes flexibility for application development and can result in more power efficient scanning. The following procedure can be used to configure the device for Automatic Scanning with CS0SMEN = 1.

1. Set the CS0SMEN bit to 1.
2. Select the start of conversion mode (CS0CM[2:0]) if not already configured. Mode 101b is the mode of choice for most systems.
3. Configure the CS0SCAN0 and CS0SCAN1 registers to enable channels in the scan.
4. Configure the CS0THH:CS0THL digital comparator threshold and polarity.
5. Enable wake from suspend on end of scan (CS0WOI = 1) if this functionality is desired.
6. Set CS0SS to point to the first channel in the scan. Note: CS0SS uses the same bit mapping as the CS0MX register.
7. Issue a start of conversion (BUSY = 1).
8. Enable the CS0 Wakeup Source and place the device in Suspend mode (optional).

If using Mode 101b, scanning will stop once a “touch” has been detected using the digital comparator. The CS0MX register will contain the channel mux value of the channel that caused the interrupt. Setting the busy bit when servicing the interrupt will cause the scan to continue where it left off. Scanning will also stop after all channels have been sampled and no “touches” have been detected. If the CS0WOI bit is set, a wake from suspend event will be generated. Note: When automatic scanning is enabled, the contents of the CS0MX register are only valid when the digital comparator interrupt is set and BUSY = 0.

## 8.10. CS0 Comparator

The CS0 comparator compares the latest capacitive sense conversion result with the value stored in CS0THH:CS0THL. If the result is less than or equal to the stored value, the CS0CMPF bit(CS0CN:0) is set to 0. If the result is greater than the stored value, CS0CMPF is set to 1.

If the CS0 conversion accumulator is configured to accumulate multiple conversions, a comparison will not be made until the last conversion has been accumulated.

An interrupt will be generated if CS0 greater-than comparator interrupts are enabled by setting the ECSDC bit (EIE2.5) when the comparator sets CS0CMPF to 1.

If auto-scan is running when the comparator sets the CS0CMPF bit, no further auto-scan initiated conversions will start until firmware sets CS0BUSY to 1.

A CS0 greater-than comparator event can wake a device from suspend mode. This feature is useful in systems configured to continuously sample one or more capacitive sense channels. The device will remain in the low-power suspend state until the captured value of one of the scanned channels causes a CS0 greater-than comparator event to occur. It is not necessary to have CS0 comparator interrupts enabled in order to wake a device from suspend with a greater-than event.

For a summary of behavior with different CS0 comparator, auto-scan, and auto accumulator settings, please see Table 8.1.

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## SFR Definition 13.1. IE: Interrupt Enable

Bit	7	6	5	4	3	2	1	0
Name	EA	ESPI0	ET2	ES0	ET1	EX1	ET0	EX0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0xA8; Bit-Addressable

Bit	Name	Function
7	EA	<b>Enable All Interrupts.</b> Globally enables/disables all interrupts. It overrides individual interrupt mask settings. 0: Disable all interrupt sources. 1: Enable each interrupt according to its individual mask setting.
6	ESPI0	<b>Enable Serial Peripheral Interface (SPI0) Interrupt.</b> This bit sets the masking of the SPI0 interrupts. 0: Disable all SPI0 interrupts. 1: Enable interrupt requests generated by SPI0.
5	ET2	<b>Enable Timer 2 Interrupt.</b> This bit sets the masking of the Timer 2 interrupt. 0: Disable Timer 2 interrupt. 1: Enable interrupt requests generated by the TF2L or TF2H flags.
4	ES0	<b>Enable UART0 Interrupt.</b> This bit sets the masking of the UART0 interrupt. 0: Disable UART0 interrupt. 1: Enable UART0 interrupt.
3	ET1	<b>Enable Timer 1 Interrupt.</b> This bit sets the masking of the Timer 1 interrupt. 0: Disable all Timer 1 interrupt. 1: Enable interrupt requests generated by the TF1 flag.
2	EX1	<b>Enable External Interrupt 1.</b> This bit sets the masking of External Interrupt 1. 0: Disable external interrupt 1. 1: Enable interrupt requests generated by the $\overline{\text{INT1}}$ input.
1	ET0	<b>Enable Timer 0 Interrupt.</b> This bit sets the masking of the Timer 0 interrupt. 0: Disable all Timer 0 interrupt. 1: Enable interrupt requests generated by the TF0 flag.
0	EX0	<b>Enable External Interrupt 0.</b> This bit sets the masking of External Interrupt 0. 0: Disable external interrupt 0. 1: Enable interrupt requests generated by the $\overline{\text{INT0}}$ input.

---

## 15.7. Determining the Event that Caused the Last Wakeup

When waking from idle mode, the CPU will vector to the interrupt which caused it to wake up. When waking from stop mode, the RSTSRC register may be read to determine the cause of the last reset.

Upon exit from suspend or sleep mode, the wake-up flags in the PMU0CF and PMU0FL registers can be read to determine the event which caused the device to wake up. After waking up, the wake-up flags will continue to be updated if any of the wake-up events occur. Wake-up flags are always updated, even if they are not enabled as wake-up sources.

All wake-up flags enabled as wake-up sources in PMU0CF and PMU0FL must be cleared before the device can enter suspend or sleep mode. After clearing the wake-up flags, each of the enabled wake-up events should be checked in the individual peripherals to ensure that a wake-up event did not occur while the wake-up flags were being cleared.

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## SFR Definition 15.3. PMU0MD: Power Management Unit Mode

Bit	7	6	5	4	3	2	1	0
Name	RTCOE	WAKEOE	MONDIS					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xB5

Bit	Name	Function
7	RTCOE	<b>Buffered SmaRTClock Output Enable.</b> Enables the buffered SmaRTClock oscillator output on P0.2. 0: Buffered SmaRTClock output not enabled. 1: Buffered SmaRTClock output is enabled.
6	WAKEOE	<b>Wakeup Request Output Enable.</b> Enables the Sleep Mode wake-up request signal on P0.3. 0: Wake-up request signal is not enabled. 1: Wake-up request signal is enabled.
5	MONDIS*	<b>POR Supply Monitor Disable.</b> Writing a 1 to this bit disables the POR supply monitor.
4:0	Unused	Read = 00000b. Write = Don't Care.

**Notes:** The POR Supply Monitor should not be disabled if the supply voltage is greater than 2.4 V. The lowest power sleep mode current, 10 nA typical, can only be achieved when the supply voltage is less than 2.4 V. The lowest power sleep mode for voltages above 2.4 V is 50 nA typical with the POR Supply Monitor enabled.

## 20.2. SmarTClock Clocking Sources

The SmarTClock peripheral is clocked from its own timebase, independent of the system clock. The SmarTClock timebase can be derived from an external CMOS clock, the internal LFO, or the SmarT-Clock oscillator circuit, which has two modes of operation: Crystal Mode, and Self-Oscillate Mode. The oscillation frequency is 32.768 kHz in Crystal Mode and can be programmed in the range of 10 kHz to 40 kHz in Self-Oscillate Mode. The internal LFO frequency is 16.4 kHz  $\pm$ 20%. The frequency of the SmarTClock oscillator can be measured with respect to another oscillator using an on-chip timer. See Section “25. Timers” on page 278 for more information on how this can be accomplished.

**Note:** The SmarTClock timebase can be selected as the system clock and routed to a port pin. See Section “19. Clocking Sources” on page 188 for information on selecting the system clock source and Section “21. Port Input/Output” on page 215 for information on how to route the system clock to a port pin. The SmarTClock timebase can also be routed to a port pin while the device is in its ultra low power sleep mode. See the PMU0MD register description for details.

### 20.2.1. Using the SmarTClock Oscillator with a Crystal or External CMOS Clock

When using Crystal Mode, a 32.768 kHz crystal should be connected between XTAL3 and XTAL4. No other external components are required. The following steps show how to start the SmarTClock crystal oscillator in software:

1. Configure the XTAL3 and XTAL4 pins for Analog I/O.
2. Set SmarTClock to Crystal Mode (XMODE = 1).
3. Disable Automatic Gain Control (AGCEN) and enable Bias Doubling (BIASX2) for fast crystal startup.
4. Set the desired loading capacitance (RTC0XCF).
5. Enable power to the SmarTClock oscillator circuit (RTC0EN = 1).
6. Wait 20 ms.
7. Poll the SmarTClock Clock Valid Bit (CLKVLD) until the crystal oscillator stabilizes.
8. Poll the SmarTClock Load Capacitance Ready Bit (LOADRDY) until the load capacitance reaches its programmed value.
9. Enable Automatic Gain Control (AGCEN) and disable Bias Doubling (BIASX2) for maximum power savings.
10. Enable the SmarTClock missing clock detector.
11. Wait 2 ms.
12. Clear the PMU0CF wake-up source flags.

In Crystal Mode, the SmarTClock oscillator may be driven by an external CMOS clock. The CMOS clock should be applied to XTAL3. XTAL4 should be left floating. In this mode, the external CMOS clock is ac coupled into the SmarTClock and should have a minimum voltage swing of 400 mV. The CMOS clock signal voltage should not exceed VDD or drop below GND. Bias levels closer to VDD will result in lower I/O power consumption because the XTAL3 pin has a built-in weak pull-up. The SmarTClock oscillator should be configured to its lowest bias setting with AGC disabled. The CLKVLD bit is indeterminate when using a CMOS clock, however, the OSCFAIL bit may be checked 2 ms after SmarTClock oscillator is powered on to ensure that there is a valid clock on XTAL3.

### 21.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the Crossbar for pin assignment; however, some digital functions bypass the Crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in PnSKIP set to 1.** Table 21.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

**Table 21.2. Port I/O Assignment for Digital Functions**

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
UART0, SPI0, SMBus, CP0 Outputs, System Clock Output, PCA0, Timer0 and Timer1 External Inputs.	Any Port pin available for assignment by the Crossbar. This includes P0.0–P1.7 pins which have their PnSKIP bit set to 0. <b>Note:</b> The Crossbar will always assign UART0 and SPI1 pins to fixed locations.	XBR0, XBR1, XBR2
Any pin used for GPIO	P0.0–P1.7, P2.7	P0SKIP, P1SKIP

### 21.2.3. Assigning Port I/O Pins to External Digital Event Capture Functions

External digital event capture functions can be used to trigger an interrupt or wake the device from a low power mode when a transition occurs on a digital I/O pin. The digital event capture functions do not require dedicated pins and will function on both GPIO pins (PnSKIP = 1) and pins in use by the Crossbar (PnSKIP = 0). External digital event capture functions cannot be used on pins configured for analog I/O. Table 21.3 shows all available external digital event capture functions.

**Table 21.3. Port I/O Assignment for External Digital Event Capture Functions**

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
External Interrupt 0	P0.0–P0.7	IT01CF
External Interrupt 1	P0.0–P0.7	IT01CF
Port Match	P0.0–P1.7	P0MASK, P0MAT P1MASK, P1MAT

# C8051F99x-C8051F98x

## 21.4. Port Match

Port match functionality allows system events to be triggered by a logic value change on P0 or P1. A software controlled value stored in the PnMAT registers specifies the expected or normal logic values of P0 and P1. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows Software to be notified if a certain change or pattern occurs on P0 or P1 input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which P0 and P1 pins should be compared against the PnMAT registers. A Port mismatch event is generated if (P0 & P0MASK) does not equal (PnMAT & P0MASK) or if (P1 & P1MASK) does not equal (PnMAT & P1MASK).

A Port mismatch event may be used to generate an interrupt or wake the device from a low power mode. See Section "13. Interrupt Handler" on page 138 and Section "15. Power Management" on page 162 for more details on interrupt and wake-up sources.

### SFR Definition 21.4. P0MASK: Port0 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P0MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0xC7

Bit	Name	Function
7:0	P0MASK[7:0]	<b>Port0 Mask Value.</b> Selects the P0 pins to be compared with the corresponding bits in P0MAT. 0: P0.n pin pad logic value is ignored and cannot cause a Port Mismatch event. 1: P0.n pin pad logic value is compared to P0MAT.n.

### SFR Definition 21.5. P0MAT: Port0 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P0MAT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

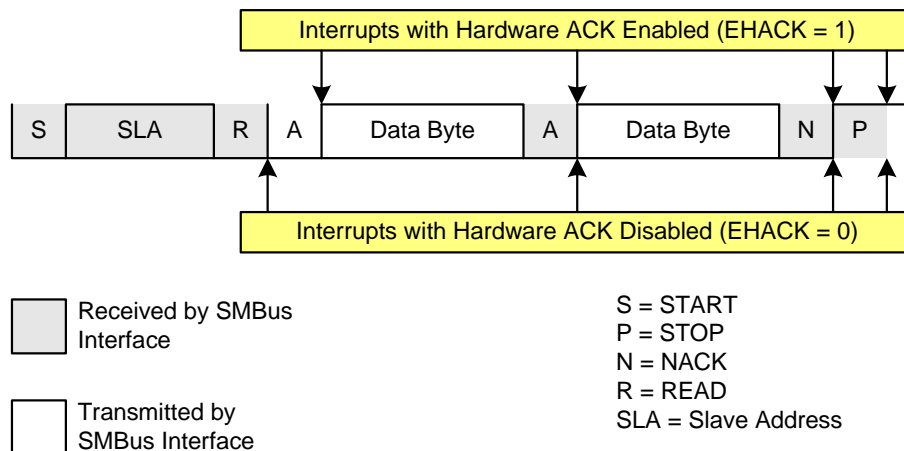
SFR Page= 0x0; SFR Address = 0xD7

Bit	Name	Function
7:0	P0MAT[7:0]	<b>Port 0 Match Value.</b> Match comparison value used on Port 0 for bits in P0MASK which are set to 1. 0: P0.n pin logic value is compared with logic LOW. 1: P0.n pin logic value is compared with logic HIGH.

#### 22.5.4. Read Sequence (Slave)

During a read sequence, an SMBus master reads data from a slave device. The slave in this transfer will be a receiver during the address byte, and a transmitter during all data bytes. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode (to receive the slave address) when a START followed by a slave address and direction bit (READ in this case) is received. If hardware ACK generation is disabled, upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. The software must respond to the received slave address with an ACK, or ignore the received slave address with a NACK. If hardware ACK generation is enabled, the hardware will apply the ACK for a slave address which matches the criteria set up by SMB0ADR and SMB0ADM. The interrupt will occur after the ACK cycle.

If the received slave address is ignored (by software or hardware), slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are transmitted. If the received slave address is acknowledged, data should be written to SMB0DAT to be transmitted. The interface enters Slave Transmitter Mode, and transmits one or more bytes of data. After each byte is transmitted, the master sends an acknowledge bit; if the acknowledge bit is an ACK, SMB0DAT should be written with the next data byte. If the acknowledge bit is a NACK, SMB0DAT should not be written to before SI is cleared (Note: an error condition may be generated if SMB0DAT is written following a received NACK while in Slave Transmitter Mode). The interface exits Slave Transmitter Mode after receiving a STOP. Note that the interface will switch to Slave Receiver Mode if SMB0DAT is not written following a Slave Transmitter interrupt. Figure 22.8 shows a typical slave read sequence. Two transmitted data bytes are shown, though any number of bytes may be transmitted. Notice that all of the 'data byte transferred' interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.



**Figure 22.8. Typical Slave Read Sequence**

#### 22.6. SMBus Status Decoding

The current SMBus status can be easily decoded using the SMB0CN register. The appropriate actions to take in response to an SMBus event depend on whether hardware slave address recognition and ACK generation is enabled or disabled. Table 22.5 describes the typical actions when hardware slave address recognition and ACK generation is disabled. Table 22.6 describes the typical actions when hardware slave address recognition and ACK generation is enabled. In the tables, STATUS VECTOR refers to the four upper bits of SMB0CN: MASTER, TXMODE, STA, and STO. The shown response options are only the typical responses; application-specific procedures are allowed as long as they conform to the SMBus specification. Highlighted responses are allowed by hardware but do not conform to the SMBus specification.



## 23. UART0

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates (details in Section “23.1. Enhanced Baud Rate Generation” on page 258). Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

UART0 has two associated SFRs: Serial Control Register 0 (SCON0) and Serial Data Buffer 0 (SBUF0). The single SBUF0 location provides access to both transmit and receive registers. **Writes to SBUF0 always access the Transmit register. Reads of SBUF0 always access the buffered Receive register; it is not possible to read data from the Transmit register.**

With UART0 interrupts enabled, an interrupt is generated each time a transmit is completed (TI0 is set in SCON0), or a data byte has been received (RI0 is set in SCON0). The UART0 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART0 interrupt (transmit complete or receive complete).

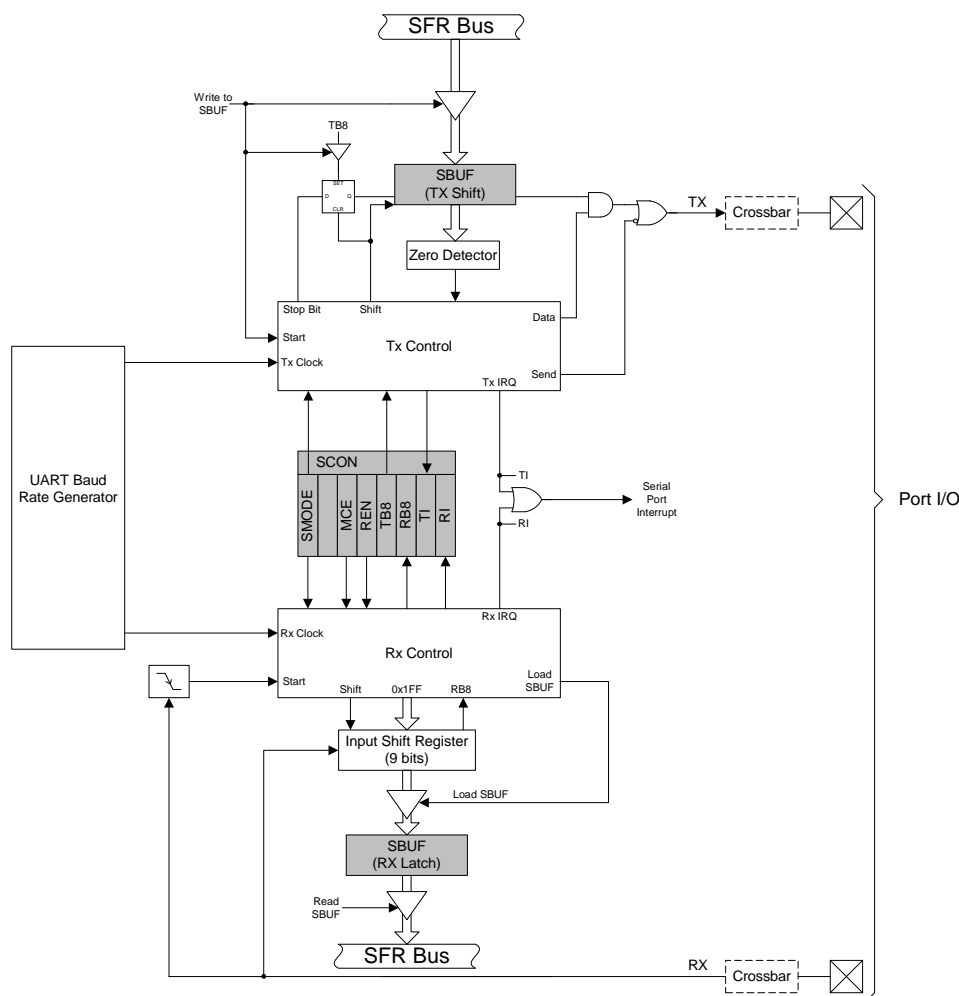
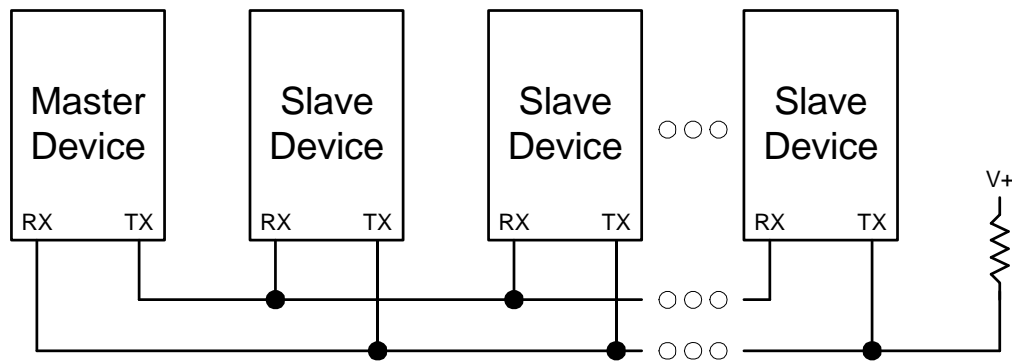


Figure 23.1. UART0 Block Diagram



**Figure 23.6. UART Multi-Processor Mode Interconnect Diagram**

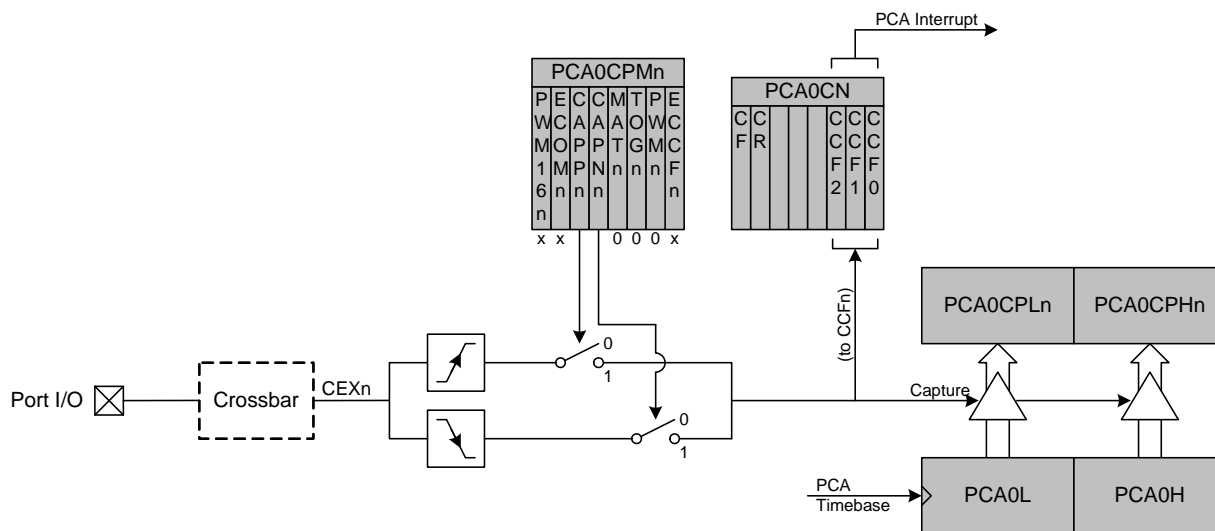
# C8051F99x-C8051F98x

**Table 24.1. SPI Slave Timing Parameters**

Parameter	Description	Min	Max	Units
<b>Master Mode Timing</b> (See Figure 24.8 and Figure 24.9)				
$T_{MCKH}$	SCK High Time	$1 \times T_{SYSCLK}$	—	ns
$T_{MCKL}$	SCK Low Time	$1 \times T_{SYSCLK}$	—	ns
$T_{MIS}$	MISO Valid to SCK Shift Edge	$1 \times T_{SYSCLK} + 20$	—	ns
$T_{MIH}$	SCK Shift Edge to MISO Change	0	—	ns
<b>Slave Mode Timing</b> (See Figure 24.10 and Figure 24.11)				
$T_{SE}$	NSS Falling to First SCK Edge	$2 \times T_{SYSCLK}$	—	ns
$T_{SD}$	Last SCK Edge to NSS Rising	$2 \times T_{SYSCLK}$	—	ns
$T_{SEZ}$	NSS Falling to MISO Valid	—	$4 \times T_{SYSCLK}$	ns
$T_{SDZ}$	NSS Rising to MISO High-Z	—	$4 \times T_{SYSCLK}$	ns
$T_{CKH}$	SCK High Time	$5 \times T_{SYSCLK}$	—	ns
$T_{CKL}$	SCK Low Time	$5 \times T_{SYSCLK}$	—	ns
$T_{SIS}$	MOSI Valid to SCK Sample Edge	$2 \times T_{SYSCLK}$	—	ns
$T_{SIH}$	SCK Sample Edge to MOSI Change	$2 \times T_{SYSCLK}$	—	ns
$T_{SOH}$	SCK Shift Edge to MISO Change	—	$4 \times T_{SYSCLK}$	ns
$T_{SLH}$	Last SCK Edge to MISO Change (CKPHA = 1 ONLY)	$6 \times T_{SYSCLK}$	$8 \times T_{SYSCLK}$	ns
<b>Note:</b> $T_{SYSCLK}$ is equal to one period of the device system clock (SYSCLK).				

## 26.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEX<sub>n</sub> pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPL<sub>n</sub> and PCA0CPH<sub>n</sub>). The CAPP<sub>n</sub> and CAPN<sub>n</sub> bits in the PCA0CPM<sub>n</sub> register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCF<sub>n</sub>) in PCA0CN is set to logic 1. An interrupt request is generated if the CCF<sub>n</sub> interrupt for that module is enabled. The CCF<sub>n</sub> bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPP<sub>n</sub> and CAPN<sub>n</sub> bits are set to logic 1, then the state of the Port pin associated with CEX<sub>n</sub> can be read directly to determine whether a rising-edge or falling-edge caused the capture.



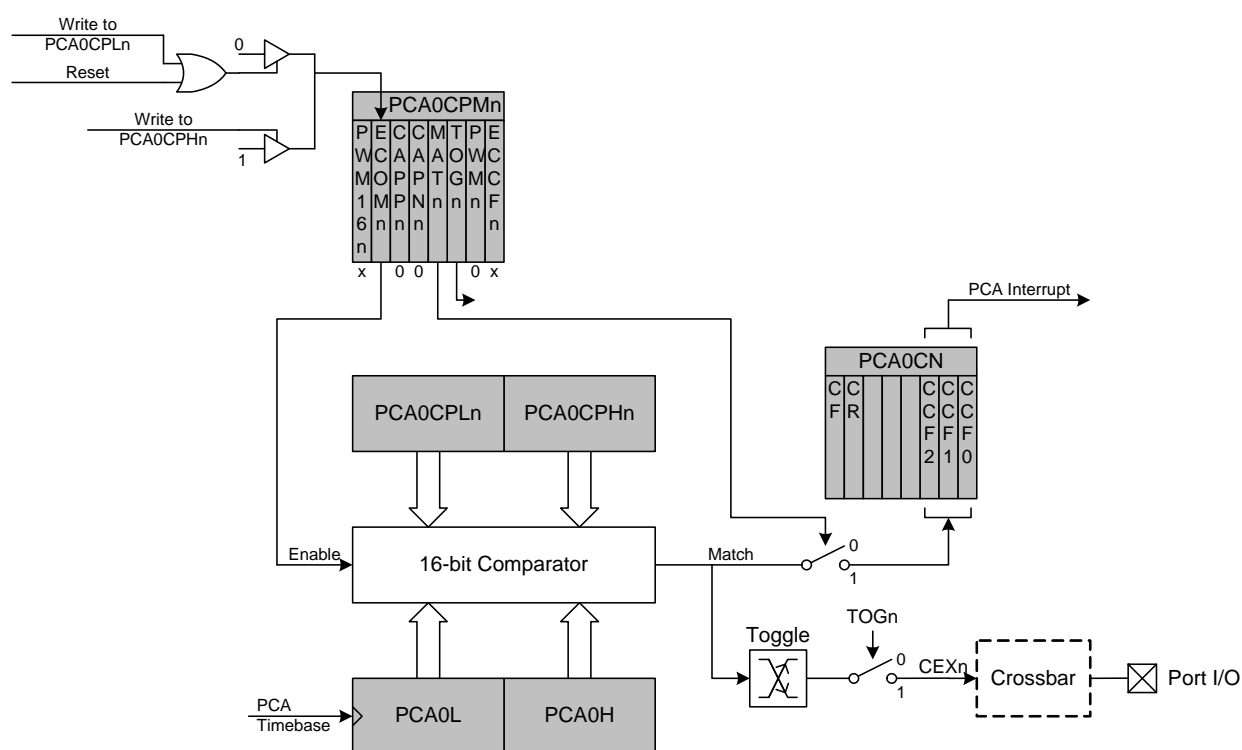
**Figure 26.4. PCA Capture Mode Diagram**

**Note:** The CEX<sub>n</sub> input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

## 26.3.3. High-Speed Output Mode

In High-Speed Output mode, a module's associated CEX<sub>n</sub> pin is toggled each time a match occurs between the PCA Counter and the module's 16-bit capture/compare register (PCA0CPH<sub>n</sub> and PCA0CPL<sub>n</sub>). When a match occurs, the Capture/Compare Flag (CCF<sub>n</sub>) in PCA0CN is set to logic 1. An interrupt request is generated if the CCF<sub>n</sub> interrupt for that module is enabled. The CCF<sub>n</sub> bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the TOG<sub>n</sub>, MAT<sub>n</sub>, and ECOM<sub>n</sub> bits in the PCA0CPM<sub>n</sub> register enables the High-Speed Output mode. If ECOM<sub>n</sub> is cleared, the associated pin will retain its state, and not toggle on the next match event.

**Important Note About Capture/Compare Registers:** When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPL<sub>n</sub> clears the ECOM<sub>n</sub> bit to 0; writing to PCA0CPH<sub>n</sub> sets ECOM<sub>n</sub> to 1.



**Figure 26.6. PCA High-Speed Output Mode Diagram**

## 26.3.4. Frequency Output Mode

Frequency Output Mode produces a programmable-frequency square wave on the module's associated CEX<sub>n</sub> pin. The capture/compare module high byte holds the number of PCA clocks to count before the output is toggled. The frequency of the square wave is then defined by Equation 26.1.

$$F_{CEXn} = \frac{F_{PCA}}{2 \times PCA0CPHn}$$

Note: A value of 0x00 in the PCA0CPH<sub>n</sub> register is equal to 256 for this equation.

**Equation 26.1. Square Wave Frequency Output**