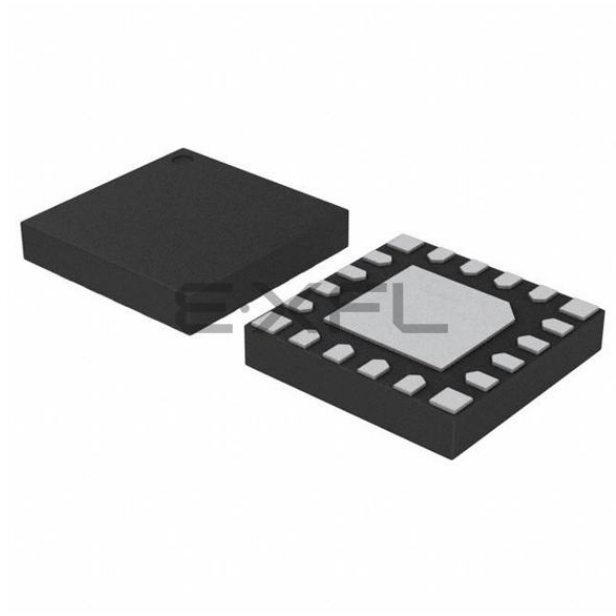

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f985-c-gm

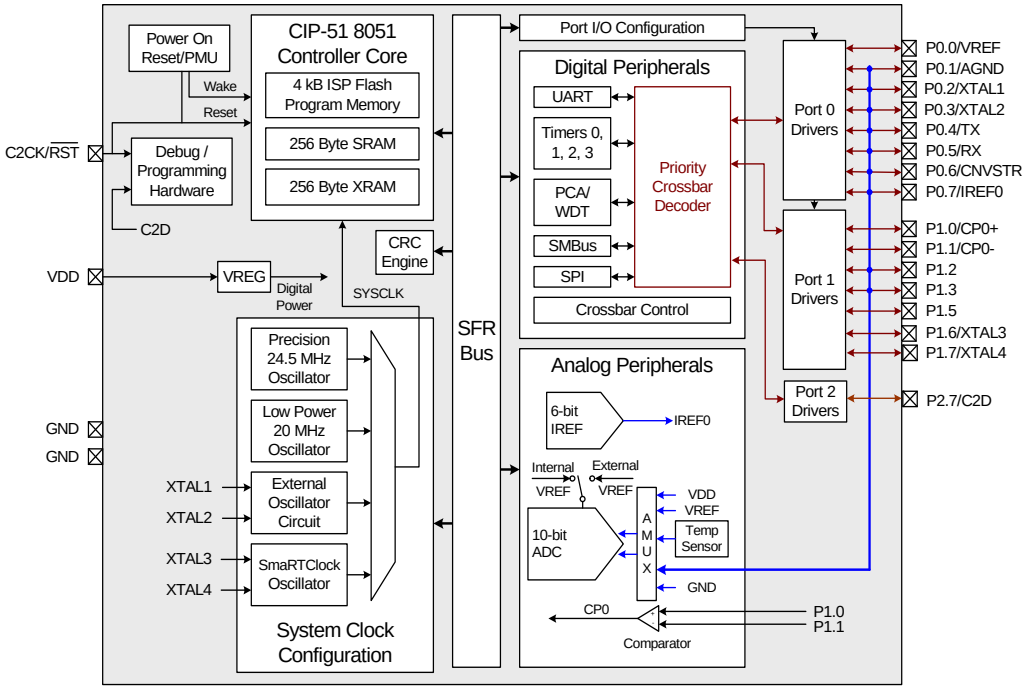

Figure 1.3. C8051F982 Block Diagram

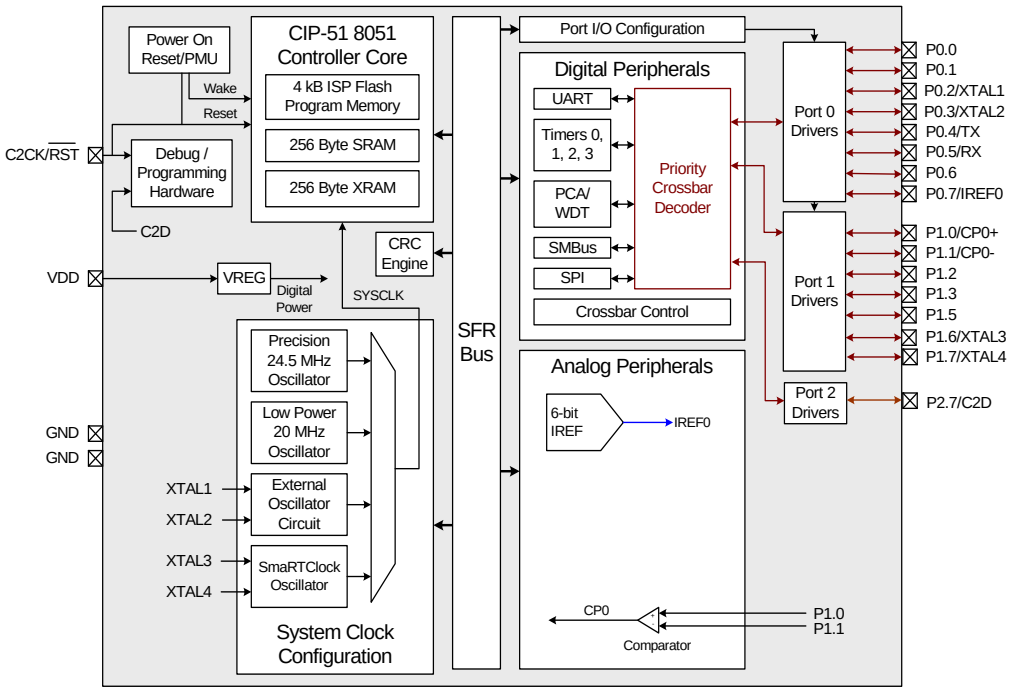

Figure 1.4. C8051F983 Block Diagram

SFR Definition 5.4. ADC0PWR: ADC0 Burst Mode Power-Up Time

Bit	7	6	5	4	3	2	1	0
Name	AD0LPM				AD0PWR[3:0]			
Type	R/W	R	R	R	R/W			
Reset	0	0	0	0	1	1	1	1

SFR Page = All; SFR Address = 0xBB

Bit	Name	Function
7	AD0LPM	**ADC0 Low Power Mode Enable.** Enables Low Power Mode Operation. 0: Low Power Mode disabled. 1: Low Power Mode enabled.
6:4	Unused	Read = 0000b; Write = Don't Care.
3:0	AD0PWR[3:0]	**ADC0 Burst Mode Power-Up Time.** Sets the time delay required for ADC0 to power up from a low power state. For BURSTEN = 0: ADC0 power state controlled by AD0EN. For BURSTEN = 1 and AD0EN = 1: ADC0 remains enabled and does not enter a low power state after all conversions are complete. Conversions can begin immediately following the start-of-conversion signal. For BURSTEN = 1 and AD0EN = 0: ADC0 enters a low power state after all conversions are complete. Conversions can begin a programmed delay after the start-of-conversion signal. The ADC0 Burst Mode Power-Up time is programmed according to the following equation: $AD0PWR = \frac{Tstartup}{400ns} - 1$ or $Tstartup = (AD0PWR + 1)400ns$ **Note:** Setting AD0PWR to 0x04 provides a typical tracking time of 2 us for the first sample taken after the start of conversion.

7.6. Comparator0 Analog Multiplexer

Comparator0 on C8051F99x-C8051F98x devices has an analog input multiplexer to connect Port I/O pins and internal signals the comparator inputs; CP0+/CP0- are the positive and negative input multiplexers for Comparator0.

The comparator input multiplexers directly support capacitive touch switches. When the Capacitive Touch Sense Compare input is selected on the positive or negative multiplexer, any Port I/O pin connected to the other multiplexer can be directly connected to a capacitive touch switch with no additional external components. The Capacitive Touch Sense Compare provides the appropriate reference level for detecting when the capacitive touch switches have charged or discharged through the on-chip Rsense resistor. The Comparator outputs can be routed to Timer2 or Timer3 for capturing sense capacitor's charge and discharge time. See Section "25. Timers" on page 278 for details.

Any of the following may be selected as comparator inputs: Port I/O pins, Capacitive Touch Sense Compare, VDD Supply Voltage, Regulated Digital Supply Voltage (Output of VREG0) or ground. The Comparator's supply voltage divided by 2 is also available as an input; the resistors used to divide the voltage only draw current when this setting is selected. The Comparator input multiplexers are configured using the CPT0MX register described in SFR Definition 7.3.

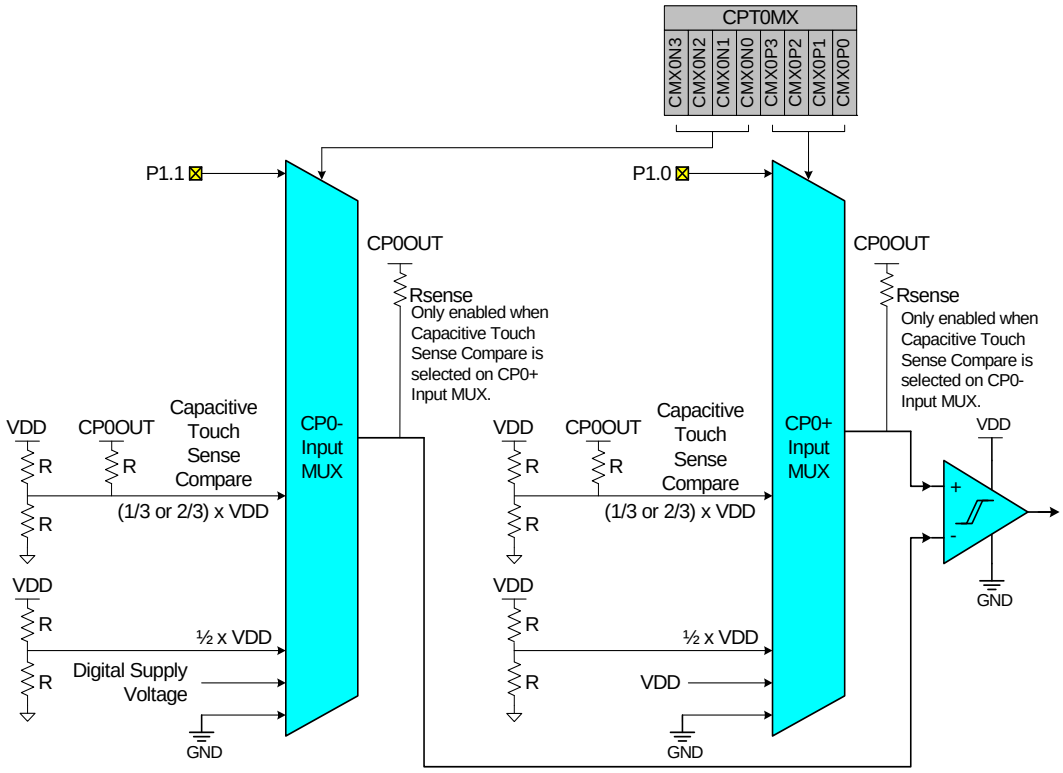

Figure 7.3. CP0 Multiplexer Block Diagram

Important Note About Comparator Input Configuration: Port pins selected as comparator inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN and disable the digital driver (PnMDOUT = 0 and Port Latch = 1). To force the Crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP. See Section "21. Port Input/Output" on page 215 for more Port I/O configuration details.

8.11. CS0 Conversion Accumulator

CS0 can be configured to accumulate multiple conversions on an input channel. The number of samples to be accumulated is configured using the CS0ACU2:0 bits (CS0CF2:0). The accumulator can accumulate 1, 4, 8, 16, 32, or 64 samples. After the defined number of samples have been accumulated, the result is divided by either 1, 4, 8, 16, 32, or 64 (depending on the CS0ACU[2:0] setting) and copied to the CS0DH:CS0DL SFRs.

Table 8.1. Operation with Auto-scan and Accumulate

Auto-Scan Enabled	Accumulator Enabled	CS0 Conversion Complete Interrupt Behavior	CS0 Greater Than Interrupt Behavior	CS0MX Behavior
N	N	CS0INT Interrupt serviced after 1 conversion completes	Interrupt serviced after 1 conversion completes if value in CS0DH:CS0DL is greater than CS0THH:CS0THL	CS0MX unchanged.
N	Y	CS0INT Interrupt serviced after *M* conversions complete	Interrupt serviced after *M* conversions complete if value in CS0DH:CS0DL (post accumulate and divide) is greater than CS0THH:CS0THL	CS0MX unchanged.
Y	N	CS0INT Interrupt serviced after 1 conversion completes	Interrupt serviced after conversion completes if value in CS0DH:CS0DL is greater than CS0THH:CS0THL; Auto-Scan stopped	If greater-than comparator detects conversion value is greater than CS0THH:CS0THL, CS0MX is left unchanged; otherwise, CS0MX updates to the next channel (CS0MX + 1) and wraps back to CS0SS after passing CS0SE.
Y	Y	CS0INT Interrupt serviced after *M* conversions complete	Interrupt serviced after *M* conversions complete if value in CS0DH:CS0DL (post accumulate and divide) is greater than CS0THH:CS0THL; Auto-Scan stopped	If greater-than comparator detects conversion value is greater than CS0THH:CS0THL, CS0MX is left unchanged; otherwise, CS0MX updates to the next channel (CS0MX + 1) and wraps back to CS0SS after passing CS0SE.

Note: M = Accumulator setting (1x, 4x, 8x, 16x, 32x, 64x).

SFR Definition 8.12. CS0MD2: Capacitive Sense Mode 2

Bit	7	6	5	4	3	2	1	0
Name	CS0CR[1:0]		CS0DT[2:0]			CS0IA[2:0]		
Type	R/W		R/W			R/W		
Reset	0	1	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xF3

Bit	Name	Description
7:6	CS0CR[1:0]	**CS0 Conversion Rate.** These bits control the conversion rate of the CS0 module. See the electrical specifications table for specific timing. 00: Conversions last 12 internal CS0 clocks and are 12 bits in length. 01: Conversions last 13 internal CS0 clocks and are 13 bits in length. 10: Conversions last 14 internal CS0 clocks and are 14 bits in length. 11: Conversions last 16 internal CS0 clocks.and are 16 bits in length.
5:3	CS0DT[2:0]	**CS0 Discharge Time.** These bits adjust the primary CS0 reset time. For most touch-sensitive switches, the default (fastest) value is sufficient. See the discussion in Section 8.13 for more information. 000: Discharge time is 0.75 µs (recommended for most switches) 001: Discharge time is 1.0 µs 010: Discharge time is 1.2 µs 011: Discharge time is 1.5 µs 100: Discharge time is 2 µs 101: Discharge time is 3 µs 110: Discharge time is 6 µs 111: Discharge time is 12 µs
2:0	CS0IA[2:0]	**CS0 Output Current Adjustment.** These bits allow the user to adjust the output current used to charge up the capacitive sensor element. For most touch-sensitive switches, the default (highest) current is sufficient. See the discussion in Section 8.13 for more information. 000: Full Current 001: 1/8 Current 010: 1/4 Current 011: 3/8 Current 100: 1/2 Current 101: 5/8 Current 110: 3/4 Current 111: 7/8 Current

SFR Definition 8.13. CS0MD3: Capacitive Sense Mode 3

Bit	7	6	5	4	3	2	1	0
Name				CS0RP[1:0]		CS0LP[2:0]		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xF3

Bit	Name	Description
7:5	Unused	Read = 000b; Write = Don't care
4:3	CS0RP[1:0]	**CS0 Ramp Selection.** These bits are used to compensate CS0 conversions for circuits requiring slower ramp times. For most touch-sensitive switches, the default (fastest) value is sufficient. See the discussion in Section 8.13 for more information. 00: Ramp time is less than 1.5 µs. 01: Ramp time is between 1.5 µs and 3 µs. 10: Ramp time is between 3 µs and 6 µs. 11: Ramp time is greater than 6 µs.
2:0	CS0LP[2:0]	**CS0 Low Pass Filter Selection.** These bits set the internal corner frequency of the CS0 low-pass filter. Higher values of CS0LP result in a lower internal corner frequency. For most touch-sensitive switches, the default setting of 000b should be used. If the CS0RP bits are adjusted from their default value, the CS0LP bits should normally be set to 001b. Settings higher than 001b will result in attenuated readings from the CS0 module and should be used only under special circumstances. See the discussion in Section 8.13 for more information.

Table 9.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
CLR A	Clear A	1	1
CPL A	Complement A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through Carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through Carry	1	1
SWAP A	Swap nibbles of A	1	1
Data Transfer			
MOV A, Rn	Move Register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move indirect RAM to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to Register	1	1
MOV Rn, direct	Move direct byte to Register	2	2
MOV Rn, #data	Move immediate to Register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move Register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2
Boolean Manipulation			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit to Carry	2	2

Table 12.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page
P1SKIP	0xD5	0x0	Port 1 Skip	231
P2	0xA0	All	Port 2 Latch	233
P2DRV	0x9D	0xF	Port 2 Drive Strength	234
P2MDOUT	0xA6	0x0	Port 2 Output Mode Configuration	234
PCA0CN	0xD8	0x0	PCA0 Control	313
PCA0CPH0	0xFC	0x0	PCA0 Capture 0 High	318
PCA0CPH1	0xEA	0x0	PCA0 Capture 1 High	318
PCA0CPH2	0xEC	0x0	PCA0 Capture 2 High	318
PCA0CPL0	0xFB	0x0	PCA0 Capture 0 Low	318
PCA0CPL1	0xE9	0x0	PCA0 Capture 1 Low	318
PCA0CPL2	0xEB	0x0	PCA0 Capture 2 Low	318
PCA0CPM0	0xDA	0x0	PCA0 Module 0 Mode Register	316
PCA0CPM1	0xDB	0x0	PCA0 Module 1 Mode Register	316
PCA0CPM2	0xDC	0x0	PCA0 Module 2 Mode Register	316
PCA0H	0xFA	0x0	PCA0 Counter High	317
PCA0L	0xF9	0x0	PCA0 Counter Low	317
PCA0MD	0xD9	0x0	PCA0 Mode	314
PCA0PWM	0xDF	0x0	PCA0 PWM Configuration	315
PCON	0x87	All	Power Control	171
PMU0CF	0xB5	0x0	PMU0 Configuration	168
PMU0FL	0xCE	0x0	PMU0 Flag Register	169
PMU0MD	0xB5	0xF	PMU0 Mode	170
PSCTL	0x8F	All	Program Store R/W Control	159
PSW	0xD0	All	Program Status Word	127
REF0CN	0xD1	0x0	Voltage Reference Control	90
REG0CN	0xC9	0x0	Voltage Regulator (REG0) Control	180
REVID	0xE2	0xF	Revision ID	155
RSTSRC	0xEF	0x0	Reset Source Configuration/Status	187
RTC0ADR	0xAC	0x0	RTC0 Address	202
RTC0DAT	0xAD	0x0	RTC0 Data	202
RTC0KEY	0xAE	0x0	RTC0 Key	201
SBUF0	0x99	0x0	UART0 Data Buffer	263
SCON0	0x98	0x0	UART0 Control	262
SFRPAGE	0xA7	All	SFR Page	134
SMB0ADM	0xF5	0x0	SMBus Slave Address Mask	247
SMB0ADR	0xF4	0x0	SMBus Slave Address	247
SMB0CF	0xC1	0x0	SMBus0 Configuration	242
SMB0CN	0xC0	0x0	SMBus0 Control	244
SMB0DAT	0xC2	0x0	SMBus0 Data	248
SP	0x81	All	Stack Pointer	126
SPI0CFG	0xA1	0x0	SPI0 Configuration	272
SPI0CKR	0xA2	0x0	SPI0 Clock Rate Control	274
SPI0CN	0xF8	0x0	SPI0 Control	273
SPI0DAT	0xA3	0x0	SPI0 Data	274

SFR Definition 16.5. CRC0CNT: CRC0 Automatic Flash Sector Count

Bit	7	6	5	4	3	2	1	0
Name				CRC0CNT[4:0]				
Type	R	R	R	R/W				
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0x9A

Bit	Name	Function
7:5	Unused	Read = 000b; Write = Don't Care.
4:0	CRC0CNT[4:0]	**Automatic CRC Calculation Block Count.** These bits specify the number of Flash blocks to include in an automatic CRC calculation. The last address of the last Flash block included in the automatic CRC calculation is (CRC0ST+CRC0CNT) x Block Size - 1. **Notes:** **1.** The block size is 256 bytes. **2.** The maximum number of blocks that may be computed in a single operation is 31. To compute a CRC on all 32 blocks, perform one operation on 31 blocks, then perform a second operation on 1 block without clearing the CRC result.

19.4. Special Function Registers for Selecting and Configuring the System Clock

The clocking sources on C8051F99x-C8051F98x devices are enabled and configured using the OSCICN, OSCICL, OSCXCN and the SmaRTClock internal registers. See Section “20. SmaRTClock (Real Time Clock)” on page 197 for SmaRTClock register descriptions. The system clock source for the MCU can be selected using the CLKSEL register. To minimize active mode current, the oneshot timer which sets Flash read time should by bypassed when the system clock is greater than 10 MHz. See the FLSCL register description for details.

The clock selected as the system clock can be divided by 1, 2, 4, 8, 16, 32, 64, or 128. When switching between two clock divide values, the transition may take up to 128 cycles of the undivided clock source. The CLKRDY flag can be polled to determine when the new clock divide value has been applied. The clock divider must be set to "divide by 1" when entering Suspend or Sleep Mode.

The system clock source may also be switched on-the-fly. The switchover takes effect after one clock period of the slower oscillator.

SFR Definition 19.1. CLKSEL: Clock Select

Bit	7	6	5	4	3	2	1	0
Name	CLKRDY	CLKDIV[2:0]				CLKSEL[2:0]		
Type	R	R/W			R/W	R/W		
Reset	1	0	0	0	0	0	1	0

SFR Page = All; SFR Address = 0xA9

Bit	Name	Function
7	CLKRDY	**System Clock Divider Clock Ready Flag.** 0: The selected clock divide setting has not been applied to the system clock. 1: The selected clock divide setting has been applied to the system clock.
6:4	CLKDIV[2:0]	**System Clock Divider Bits.** Selects the clock division to be applied to the undivided system clock source. 000: System clock is divided by 1. 001: System clock is divided by 2. 010: System clock is divided by 4. 011: System clock is divided by 8. 100: System clock is divided by 16. 101: System clock is divided by 32. 110: System clock is divided by 64. 111: System clock is divided by 128.
3	Unused	Read = 0b. Must Write 0b.
2:0	CLKSEL[2:0]	**System Clock Select.** Selects the oscillator to be used as the undivided system clock source. 000: Precision Internal Oscillator. 001: External Oscillator. 010: Low Power Oscillator divided by 8. 011: SmaRTClock Oscillator. 100: Low Power Oscillator. All other values reserved.

Internal Register Definition 20.4. RTC0CN: SmaRTClock Control

Bit	7	6	5	4	3	2	1	0
Name	RTC0EN	MCLKEN	OSCFAIL	RTC0TR	RTC0AEN	ALRM	RTC0SET	RTC0CAP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	Varies	0	0	0	0	0

SmaRTClock Address = 0x04

Bit	Name	Function		
7	RTC0EN	**SmaRTClock Enable.** Enables/disables the SmaRTClock oscillator and associated bias currents. 0: SmaRTClock oscillator disabled. 1: SmaRTClock oscillator enabled.		
6	MCLKEN	**Missing SmaRTClock Detector Enable.** Enables/disables the missing SmaRTClock detector. 0: Missing SmaRTClock detector disabled. 1: Missing SmaRTClock detector enabled.		
5	OSCFAIL	**SmaRTClock Oscillator Fail Event Flag.** Set by hardware when a missing SmaRTClock detector timeout occurs. Must be cleared by software. The value of this bit is not defined when the SmaRTClock oscillator is disabled.		
4	RTC0TR	**SmaRTClock Timer Run Control.** Controls if the SmaRTClock timer is running or stopped (holds current value). 0: SmaRTClock timer is stopped. 1: SmaRTClock timer is running.		
3	RTC0AEN	**SmaRTClock Alarm Enable.** Enables/disables the SmaRTClock alarm function. Also clears the ALRM flag. 0: SmaRTClock alarm disabled. 1: SmaRTClock alarm enabled.		
2	ALRM	**SmaRTClock Alarm Event Flag and Auto Reset Enable.** Reads return the state of the alarm event flag. Writes enable/disable the Auto Reset function.	Read: 0: SmaRTClock alarm event flag is de-asserted. 1: SmaRTClock alarm event flag is asserted.	Write: 0: Disable Auto Reset. 1: Enable Auto Reset.
1	RTC0SET	**SmaRTClock Timer Set.** Writing 1 initiates a SmaRTClock timer set operation. This bit is cleared to 0 by hardware to indicate that the timer set operation is complete.		
0	RTC0CAP	**SmaRTClock Timer Capture.** Writing 1 initiates a SmaRTClock timer capture operation. This bit is cleared to 0 by hardware to indicate that the timer capture operation is complete.		
Note: The ALRM flag will remain asserted for a maximum of one SmaRTClock cycle. See Section “Power Management” on page 162 for information on how to capture a SmaRTClock Alarm event using a flag which is not automatically cleared by hardware.				

SFR Definition 21.1. XBR0: Port I/O Crossbar Register 0

Bit	7	6	5	4	3	2	1	0
Name			CP0AE	CP0E	SYSCKE	SMB0E	SPI0E	URT0E
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xE1

Bit	Name	Function
7:6	Unused	Read = 00b. Write = Don't Care.
5	CP0AE	**Comparator0 Asynchronous Output Enable.** 0: Asynchronous CP0 output unavailable at Port pin. 1: Asynchronous CP0 output routed to Port pin.
4	CP0E	**Comparator0 Output Enable.** 0: CP1 output unavailable at Port pin. 1: CP1 output routed to Port pin.
3	SYSCKE	**$\overline{\text{SYSCLK}}$ Output Enable.** 0: $\overline{\text{SYSCLK}}$ output unavailable at Port pin. 1: $\overline{\text{SYSCLK}}$ output routed to Port pin.
2	SMB0E	**SMBus I/O Enable.** 0: SMBus I/O unavailable at Port pin. 1: SDA and SCL routed to Port pins.
1	SPI0E	**SPI0 I/O Enable.** 0: SPI0 I/O unavailable at Port pin. 1: SCK, MISO, and MOSI (for SPI0) routed to Port pins. NSS (for SPI0) routed to Port pin only if SPI0 is configured to 4-wire mode.
0	URT0E	**UART0 Output Enable.** 0: UART I/O unavailable at Port pin. 1: TX0 and RX0 routed to Port pins P0.4 and P0.5.
Note: SPI0 can be assigned either 3 or 4 Port I/O pins.		

SFR Definition 21.3. XBR2: Port I/O Crossbar Register 2

Bit	7	6	5	4	3	2	1	0
Name	WEAKPUD	XBARE						
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xE3

Bit	Name	Function
7	WEAKPUD	**Port I/O Weak Pullup Disable.** 0: Weak Pullups enabled (except for Port I/O pins configured for analog mode). 1: Weak Pullups disabled.
6	XBARE	**Crossbar Enable.** 0: Crossbar disabled. 1: Crossbar enabled.
5:0	Unused	Read = 000000b; Write = Don't Care.
Note: The Crossbar must be enabled (XBARE = 1) to use any Port pin as a digital output.		

SFR Definition 25.3. TMOD: Timer Mode

Bit	7	6	5	4	3	2	1	0
Name	GATE1	C/T1	T1M[1:0]		GATE0	C/T0	T0M[1:0]	
Type	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x89

Bit	Name	Function
7	GATE1	**Timer 1 Gate Control.** 0: Timer 1 enabled when TR1 = 1 irrespective of $\overline{\text{INT1}}$ logic level. 1: Timer 1 enabled only when TR1 = 1 AND $\overline{\text{INT1}}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 13.7).
6	C/T1	**Counter/Timer 1 Select.** 0: Timer: Timer 1 incremented by clock defined by T1M bit in register CKCON. 1: Counter: Timer 1 incremented by high-to-low transitions on external pin (T1).
5:4	T1M[1:0]	**Timer 1 Mode Select.** These bits select the Timer 1 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Timer 1 Inactive
3	GATE0	**Timer 0 Gate Control.** 0: Timer 0 enabled when TR0 = 1 irrespective of $\overline{\text{INT0}}$ logic level. 1: Timer 0 enabled only when TR0 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 13.7).
2	C/T0	**Counter/Timer 0 Select.** 0: Timer: Timer 0 incremented by clock defined by T0M bit in register CKCON. 1: Counter: Timer 0 incremented by high-to-low transitions on external pin (T0).
1:0	T0M[1:0]	**Timer 0 Mode Select.** These bits select the Timer 0 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Two 8-bit Counter/Timers

SFR Definition 25.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x8C

Bit	Name	Function
7:0	TH0[7:0]	**Timer 0 High Byte.** The TH0 register is the high byte of the 16-bit Timer 0.

SFR Definition 25.7. TH1: Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x8D

Bit	Name	Function
7:0	TH1[7:0]	**Timer 1 High Byte.** The TH1 register is the high byte of the 16-bit Timer 1.

25.3.3. SmaRTClock/External Oscillator Capture Mode

The Capture Mode in Timer 3 allows either SmaRTClock or the external oscillator period to be measured against the system clock or the system clock divided by 12. SmaRTClock and the external oscillator period can also be compared against each other.

Setting TF3CEN to 1 enables the SmaRTClock/External Oscillator Capture Mode for Timer 3. In this mode, T3SPLIT should be set to 0, as the full 16-bit timer is used.

When Capture Mode is enabled, a capture event will be generated either every SmaRTClock rising edge or every 8 external clock cycles, depending on the T3XCLK1 setting. When the capture event occurs, the contents of Timer 3 (TMR3H:TMR3L) are loaded into the Timer 3 reload registers (TMR3RLH:TMR3RLL) and the TF3H flag is set (triggering an interrupt if Timer 3 interrupts are enabled). By recording the difference between two successive timer capture values, the SmaRTClock or external clock period can be determined with respect to the Timer 3 clock. The Timer 3 clock should be much faster than the capture clock to achieve an accurate reading.

For example, if T3ML = 1b, T3XCLK1 = 0b, and TF3CEN = 1b, Timer 3 will clock every SYSCLK and capture every SmaRTClock rising edge. If SYSCLK is 24.5 MHz and the difference between two successive captures is 350 counts, then the SmaRTClock period is as follows:

350 x (1 / 24.5 MHz) = 14.2 µs.

This mode allows software to determine the exact frequency of the external oscillator in C and RC mode or the time between consecutive SmaRTClock rising edges, which is useful for determining the SmaRTClock frequency.

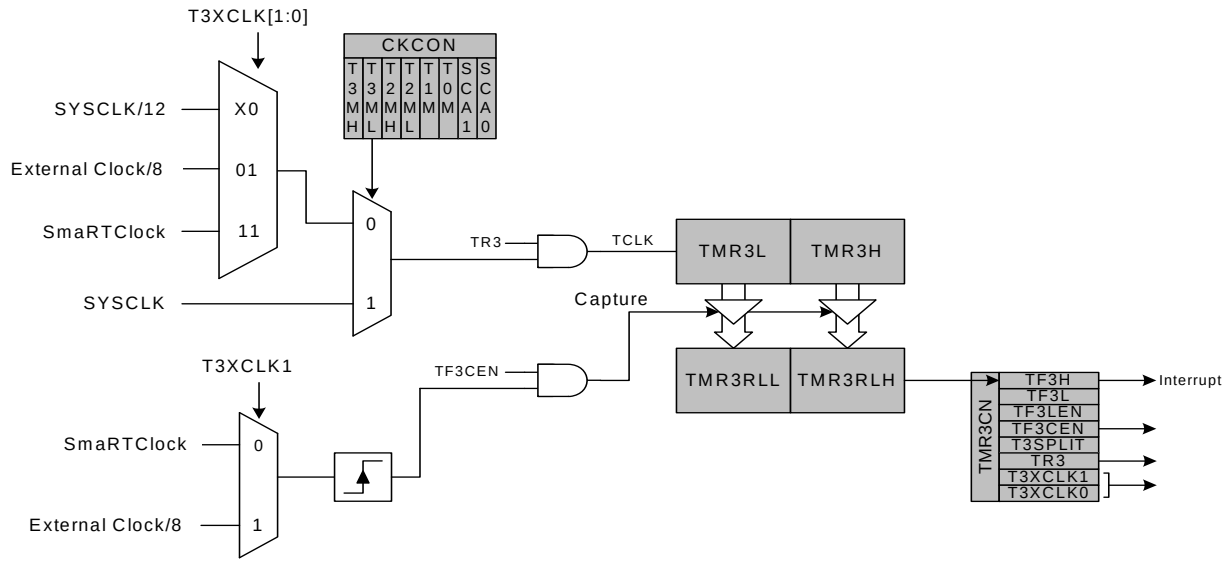

Figure 25.9. Timer 3 Capture Mode Block Diagram

SFR Definition 25.14. TMR3RLL: Timer 3 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x92

Bit	Name	Function
7:0	TMR3RLL[7:0]	**Timer 3 Reload Register Low Byte.** TMR3RLL holds the low byte of the reload value for Timer 3.

SFR Definition 25.15. TMR3RLH: Timer 3 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x93

Bit	Name	Function
7:0	TMR3RLH[7:0]	**Timer 3 Reload Register High Byte.** TMR3RLH holds the high byte of the reload value for Timer 3.

26.3.6. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. 16-bit PWM mode is independent of the other (8/9/10/11-bit) PWM modes. In this mode, the 16-bit capture/compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is asserted high; when the 16-bit counter overflows, CEXn is asserted low. To output a varying duty cycle, new value writes should be synchronized with PCA CCFn match interrupts. 16-Bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. If the MATn bit is set to 1, the CCFn flag for the module will be set each time a 16-bit comparator match (rising edge) occurs. The CF flag in PCA0CN can be used to detect the overflow (falling edge). The duty cycle for 16-Bit PWM Mode is given by Equation 26.4.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(65536 - PCA0CPn)}{65536}$$

Equation 26.4. 16-Bit PWM Duty Cycle

Using Equation 26.4, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

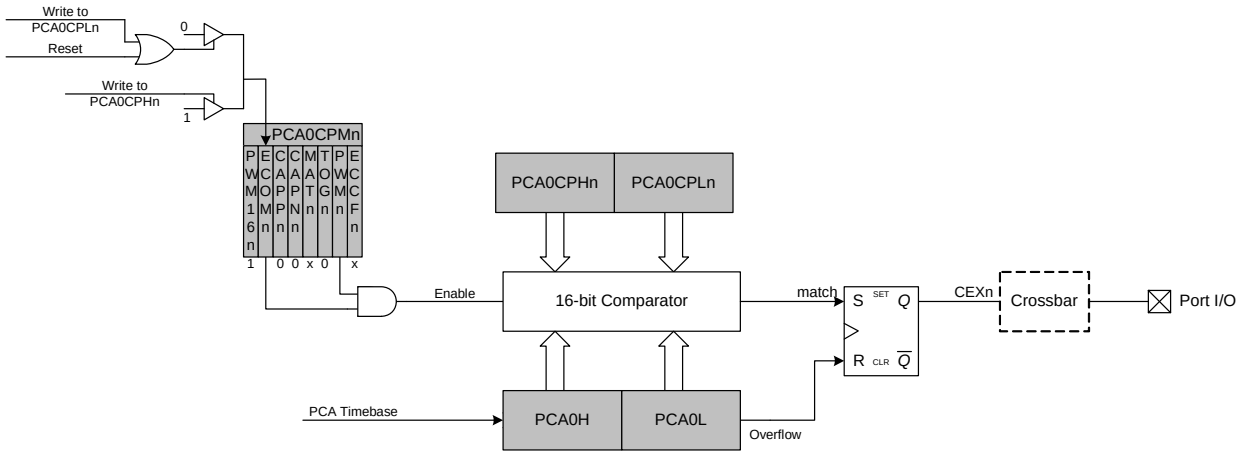

Figure 26.10. PCA 16-Bit PWM Mode

The 8-bit offset held in PCA0CPH2 is compared to the upper byte of the 16-bit PCA counter. This offset value is the number of PCA0L overflows before a reset. Up to 256 PCA clocks may pass before the first PCA0L overflow occurs, depending on the value of the PCA0L when the update is performed. The total offset is then given (in PCA clocks) by Equation 26.5, where PCA0L is the value of the PCA0L register at the time of the update.

$$Offset = (256 \times PCA0CPL2) + (256 - PCA0L)$$

Equation 26.5. Watchdog Timer Offset in PCA Clocks

The WDT reset is generated when PCA0L overflows while there is a match between PCA0CPH2 and PCA0H. Software may force a WDT reset by writing a 1 to the CCF2 flag (PCA0CN.2) while the WDT is enabled.

26.4.2. Watchdog Timer Usage

To configure the WDT, perform the following tasks:

1. Disable the WDT by writing a 0 to the WDTE bit.
2. Select the desired PCA clock source (with the CPS2–CPS0 bits).
3. Load PCA0CPL2 with the desired WDT update offset value.
4. Configure the PCA Idle mode (set CIDL if the WDT should be suspended while the CPU is in Idle mode).
5. Enable the WDT by setting the WDTE bit to 1.
6. Reset the WDT timer by writing to PCA0CPH2.

The PCA clock source and Idle mode select cannot be changed while the WDT is enabled. The watchdog timer is enabled by setting the WDTE or WDLCK bits in the PCA0MD register. When WDLCK is set, the WDT cannot be disabled until the next system reset. If WDLCK is not set, the WDT is disabled by clearing the WDTE bit.

The WDT is enabled following any reset. The PCA0 counter clock defaults to the system clock divided by 12, PCA0L defaults to 0x00, and PCA0CPL2 defaults to 0x00. Using Equation 26.5, this results in a WDT timeout interval of 256 PCA clock cycles, or 3072 system clock cycles. Table 26.3 lists some example timeout intervals for typical system clocks.

Table 26.3. Watchdog Timer Timeout Intervals[1]

System Clock (Hz)	PCA0CPL2	Timeout Interval (ms)
24,500,000	255	32.1
24,500,000	128	16.2
24,500,000	32	4.1
3,062,500[2]	255	257
3,062,500[2]	128	129.5
3,062,500[2]	32	33.1
32,000	255	24576
32,000	128	12384
32,000	32	3168

Notes:
1. Assumes SYSCLK/12 as the PCA clock source, and a PCA0L value of 0x00 at the update time.
2. Internal SYSCLK reset frequency = Internal Oscillator divided by 8.