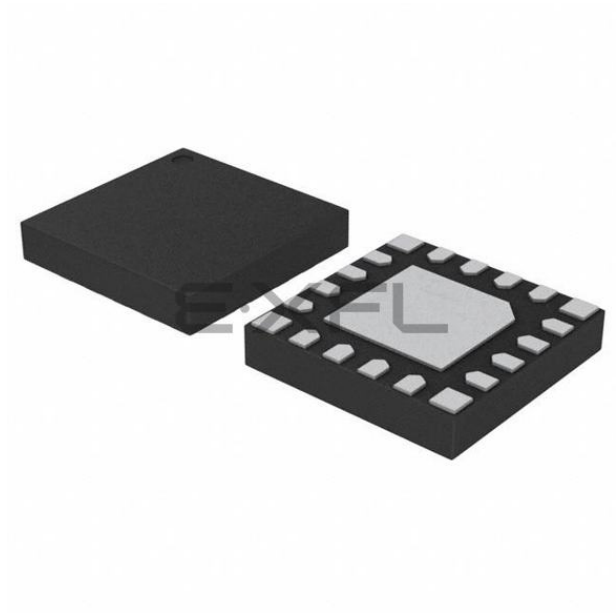

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f985-gm

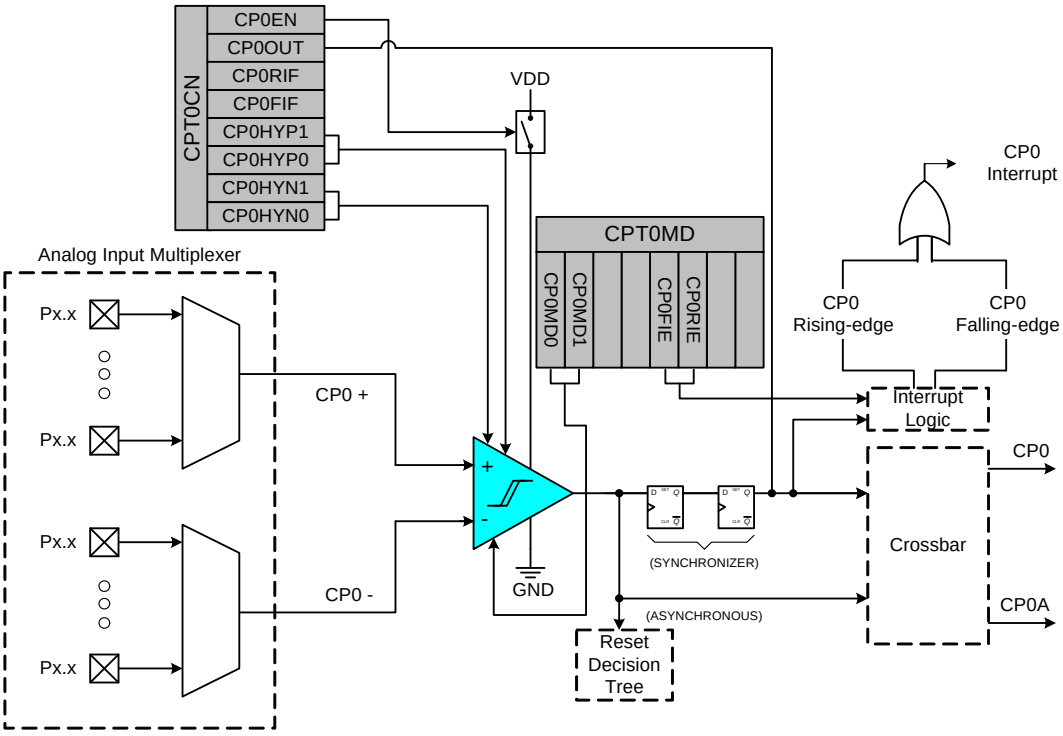

Figure 1.18. Comparator 0 Functional Block Diagram

Table 4.4. Reset Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{RST}$ Output Low Voltage	I_{OL} = 1.4 mA,	—	—	0.6	V
$\overline{RST}$ Input High Voltage	V_{DD} = 12.0 to 3.6 V	V_{DD} – 0.6	—	—	V
	V_{DD} = 10.9 to 2.0 V	0.7 x V_{DD}	—	—	V
$\overline{RST}$ Input Low Voltage	V_{DD} = 12.0 to 3.6 V	—	—	0.6	V
	V_{DD} = 10.9 to 2.0 V	—	—	0.3 x V_{DD}	V
$\overline{RST}$ Input Pullup Current	$\overline{RST}$ = 10.0 V, V_{DD} = 1.8 V	—	4	—	µA
	$\overline{RST}$ = 10.0 V, V_{DD} = 13.6 V	—	20	30	
V_{DD} Monitor Threshold (V_{RST})	Early Warning	1.8	1.85	1.9	V
	Reset Trigger (all power modes except Sleep)	1.7	1.75	1.8	
V_{DD} Ramp Time for Power On	V_{DD} Ramp from 0–1.8 V	—	—	3	ms
POR Monitor Threshold (V_{POR})	Brownout Condition (V_{DD} Falling)	0.75	1.0	1.3	V
	Recovery from Brownout (V_{DD} Rising)	—	1.75	—	
Missing Clock Detector Timeout	Time from last system clock rising edge to reset initiation	100	650	1000	µs
Minimum System Clock w/ Missing Clock Detector Enabled	System clock frequency which triggers a missing clock detector timeout	—	7	10	kHz
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	—	10	—	µs
Minimum $\overline{RST}$ Low Time to Generate a System Reset		15	—	—	µs
V_{DD} Monitor Turn-on Time		—	300	—	ns
V_{DD} Monitor Supply Current		—	7	—	µA

5. SAR ADC with 16-bit Auto-Averaging Accumulator and Autonomous Low Power Burst Mode

The ADC0 on C8051F980/6 and C8051F990/6 devices is a 300 ksps, 10-bit or 75 ksps, 12-bit successive-approximation-register (SAR) ADC with integrated track-and-hold and programmable window detector. ADC0 also has an autonomous low power Burst Mode which can automatically enable ADC0, capture and accumulate samples, then place ADC0 in a low power shutdown mode without CPU intervention. It also has a 16-bit accumulator that can automatically oversample and average the ADC results. See Section 5.4 for more details on using the ADC in 12-bit mode. C8051F982 and C8051F988 devices only support the 10-bit mode.

The ADC is fully configurable under software control via Special Function Registers. The ADC0 operates in Single-ended mode and may be configured to measure various different signals using the analog multiplexer described in “5.7. ADC0 Analog Multiplexer” on page 83. The voltage reference for the ADC is selected as described in “5.9. Voltage and Ground Reference Options” on page 88.

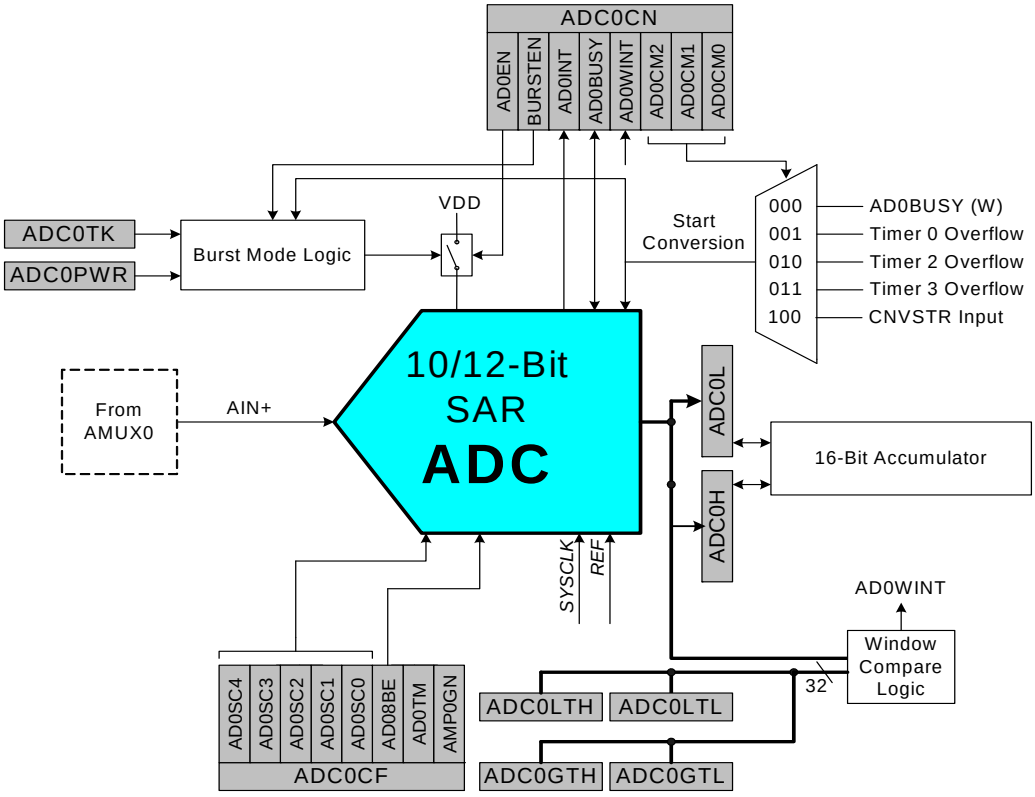

Figure 5.1. ADC0 Functional Block Diagram

8.4. CS0 Multiple Channel Enable

CS0 has the capability of measuring the total capacitance of multiple channels using a single conversion. When the multiple channel feature is enabled (CS0MCEN = 1), Channels selected by CS0SCAN0/1 are internally shorted together and the combined node is selected as the CS0 input. This mode can be used to detect a capacitance change on multiple channels using a single conversion and is useful for implementing “wake-on-multiple channels”.

8.5. CS0 Gain Adjustment

The gain of the CS0 circuit can be adjusted in integer increments from 1x to 8x (8x is the default). High gain gives the best sensitivity and resolution for small capacitors, such as those typically implemented as touch-sensitive PCB features. To measure larger capacitance values, the gain should be lowered accordingly. The bits CS0CG[2:0] in register CS0MD set the gain value.

8.6. Wake from Suspend

CS0 has the capability of waking the device from a low power suspend mode upon detection of a “touch” using the digital comparator. When the CS0SMEN is set to 1, CS0 may also wake up the device after an end of scan event when CS0CM[2:0] are set to 101b or after each conversion when CS0CM[2:0] are set to 110b or 111b. If the accumulate feature is enabled, the device wakes up after all samples have been accumulated. The CS0WOI bit in the CS0MD1 register can be used to configure desire wake from suspend behavior.

8.7. Using CS0 in Applications that Utilize Sleep Mode

To achieve maximum power efficiency, CS0 should be enabled only when taking a conversion and disabled at all other times. CS0 must be disabled by software prior to entering Sleep Mode.

9. CIP-51 Microcontroller

The MCU system controller core is the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The MCU family has a superset of all the peripherals included with a standard 8051. The CIP-51 also includes on-chip debug hardware (see description in Section 27) and interfaces directly with the analog and digital subsystems providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 9.1 for a block diagram). The CIP-51 includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 25 MIPS Peak Throughput with 25 MHz Clock
- 0 to 25 MHz Clock Frequency
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- On-chip Debug Logic
- Program and Data Memory Security

9.1. Performance

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute and usually have a maximum system clock of 12 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

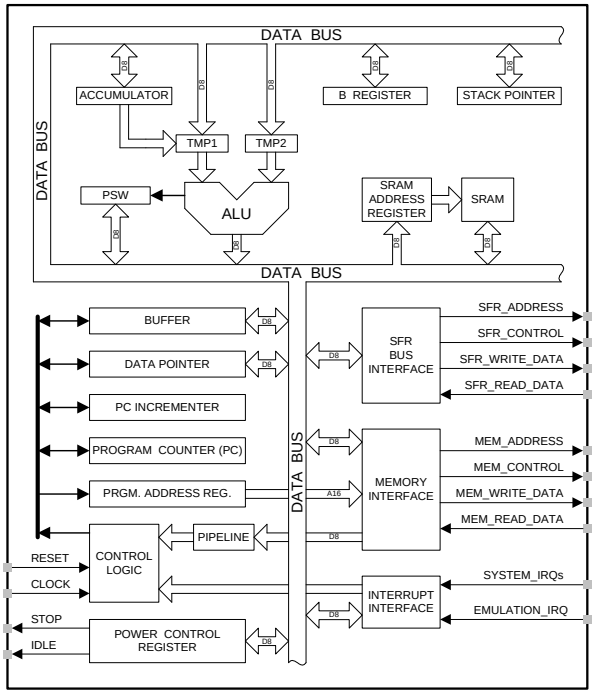

Figure 9.1. CIP-51 Block Diagram

12. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the C8051F99x-C8051F98x's resources and peripherals. The CIP-51 controller core duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the C8051F99x-C8051F98x. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 12.1 and Table 12.2 list the SFRs implemented in the C8051F99x-C8051F98x device family.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g., P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 12.3, for a detailed description of each register.

Table 12.1. Special Function Register (SFR) Memory Map (Page 0x0)

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	CS0THL	CS0THH	VDM0CN
F0	B	P0MDIN	P1MDIN	CS0MD2	SMB0ADR	SMB0ADM	EIP1	EIP2
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	CS0DL	CS0DH	RSTSRC
E0	ACC	XBR0	XBR1	XBR2	IT01CF	FLWR	EIE1	EIE2
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	CS0SS	CS0SE	PCA0PWM
D0	PSW	REF0CN	CS0SCAN0	CS0SCAN1	P0SKIP	P1SKIP	IREF0CN	P0MAT
C8	TMR2CN	REG0CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H	PMU0FL	P1MAT
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	P0MASK
B8	IP	IREF0CN	ADC0AC	ADC0PWR	ADC0TK	ADC0L	ADC0H	P1MASK
B0	CS0CN	OSCXCN	OSCICN	OSCICL		PMU0CF	FLSCL	FLKEY
A8	IE	CLKSEL	CS0CF	CS0MX	RTC0ADR	RTC0DAT	RTC0KEY	CS0MD1
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	SFRPAGE
98	SCON0	SBUF0	CRC0CNT	CPT0CN	CRC0FLIP	CPT0MD	CRC0AUTO	CPT0MX
90	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	ADC0MX	ADC0CF
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH	CRC0CN	CRC0IN	CRC0DAT	PCON
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

(bit addressable)

Table 12.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page
TCON	0x88	0x0	Timer/Counter Control	284
TH0	0x8C	0x0	Timer/Counter 0 High	287
TH1	0x8D	0x0	Timer/Counter 1 High	287
TL0	0x8A	0x0	Timer/Counter 0 Low	286
TL1	0x8B	0x0	Timer/Counter 1 Low	286
TMOD	0x89	0x0	Timer/Counter Mode	285
TMR2CN	0xC8	0x0	Timer/Counter 2 Control	291
TMR2H	0xCD	0x0	Timer/Counter 2 High	293
TMR2L	0xCC	0x0	Timer/Counter 2 Low	293
TMR2RLH	0xCB	0x0	Timer/Counter 2 Reload High	292
TMR2RLL	0xCA	0x0	Timer/Counter 2 Reload Low	292
TMR3CN	0x91	0x0	Timer/Counter 3 Control	297
TMR3H	0x95	0x0	Timer/Counter 3 High	299
TMR3L	0x94	0x0	Timer/Counter 3 Low	299
TMR3RLH	0x93	0x0	Timer/Counter 3 Reload High	298
TMR3RLL	0x92	0x0	Timer/Counter 3 Reload Low	298
TOFFH	0x8E	0xF	Temperature Offset High	87
TOFFL	0x8D	0xF	Temperature Offset Low	87
VDM0CN	0xFF	0x0	VDD Monitor Control	184
XBR0	0xE1	0x0	Port I/O Crossbar Control 0	222
XBR1	0xE2	0x0	Port I/O Crossbar Control 1	223
XBR2	0xE3	0x0	Port I/O Crossbar Control 2	224

14.3. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to 1 before software can modify the Flash memory; both PSWE and PSEE must be set to 1 before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. See **Section "10. Memory Organization" on page 128** for the location of the security byte. The Flash security mechanism allows the user to lock *n* 512-byte Flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where *n* is the 1s complement number represented by the Security Lock Byte. **The page containing the Flash Security Lock Byte is unlocked when no other Flash pages are locked (all bits of the Lock Byte are 1) and locked when any other Flash pages are locked (any bit of the Lock Byte is 0).**

Security Lock Byte:	1111 1011b
ones Complement:	0000 0100b
Flash pages locked:	5 (First four Flash pages + Lock Byte Page)

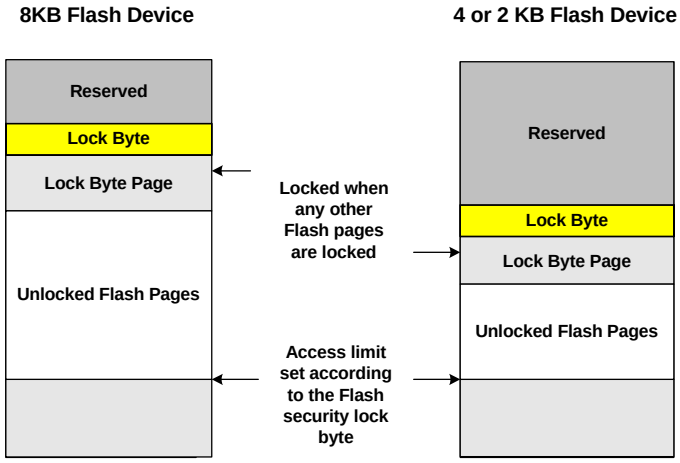

Figure 14.1. Flash Program Memory Map (8 kB and smaller devices)

The level of Flash security depends on the Flash access method. The three Flash access methods that can be restricted are reads, writes, and erases from the C2 debug interface, user firmware executing on unlocked pages, and user firmware executing on locked pages. Table 14.1 summarizes the Flash security features of the C8051F99x-C8051F98x devices.

SFR Definition 14.2. REVID: Revision Identification

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xE2

Bit	Name	Function
7:0	REVID[7:0]	**Revision Identification.** These bits contain a value that can be decoded to determine the silicon revision. For example, 0x00 for Rev A, 0x01 for Rev B, 0x02 for Rev C, etc.

15. Power Management

C8051F99x-C8051F98x devices support 5 power modes: Normal, Idle, Stop, Suspend, and Sleep. The power management unit (PMU0) allows the device to enter and wake-up from the available power modes. A brief description of each power mode is provided in Table 15.1. Detailed descriptions of each mode can be found in the following sections.

Table 15.1. Power Modes

Power Mode	Description	Wake-Up Sources	Power Savings
Normal	Device fully functional	N/A	Excellent MIPS/mW
Idle	All peripherals fully functional. Very easy to wake up.	Any Interrupt	Good No Code Execution
Stop	Legacy 8051 low power mode. A reset is required to wake up.	Any Reset	Good No Code Execution Precision Oscillator Disabled
Suspend	Similar to Stop Mode, but very fast wake-up time and code resumes execution at the next instruction.	CS0, SmaRTClock, Port Match, Comparator0, $\overline{\text{RST}}$ pin	Very Good No Code Execution All Internal Oscillators Disabled System Clock Gated
Sleep	Ultra Low Power and flexible wake-up sources. Code resumes execution at the next instruction. Comparator0 only functional in two-cell mode.	SmaRTClock, Port Match, Comparator0, $\overline{\text{RST}}$ pin	Excellent Power Supply Gated All Oscillators except SmaRT-Clock Disabled

In battery powered systems, the system should spend as much time as possible in sleep mode in order to preserve battery life. When a task with a fixed number of clock cycles needs to be performed, the device should switch to normal mode, finish the task as quickly as possible, and return to sleep mode. Idle mode and suspend modes provide a very fast wake-up time; however, the power savings in these modes will not be as much as in sleep mode. Stop mode is included for legacy reasons; the system will be more power efficient and easier to wake up when idle, suspend, or sleep mode are used.

Although switching power modes is an integral part of power management, enabling/disabling individual peripherals as needed will help lower power consumption in all power modes. Each analog peripheral can be disabled when not in use or placed in a low power mode. Digital peripherals such as timers or serial busses draw little power whenever they are not in use. Digital peripherals draw no power in sleep mode.

15.1. Normal Mode

The MCU is fully functional in normal mode. Figure 15.1 shows the on-chip power distribution to various peripherals. There are two supply voltages powering various sections of the chip: V_{DD} and the 1.8 V internal core supply. All analog peripherals are directly powered from the V_{DD} pin. All digital peripherals and the CIP-51 core are powered from the 1.8 V internal core supply. RAM, PMU0 and the SmaRTClock are always powered directly from the V_{DD} pin in sleep mode and powered from the core supply in all other power modes.

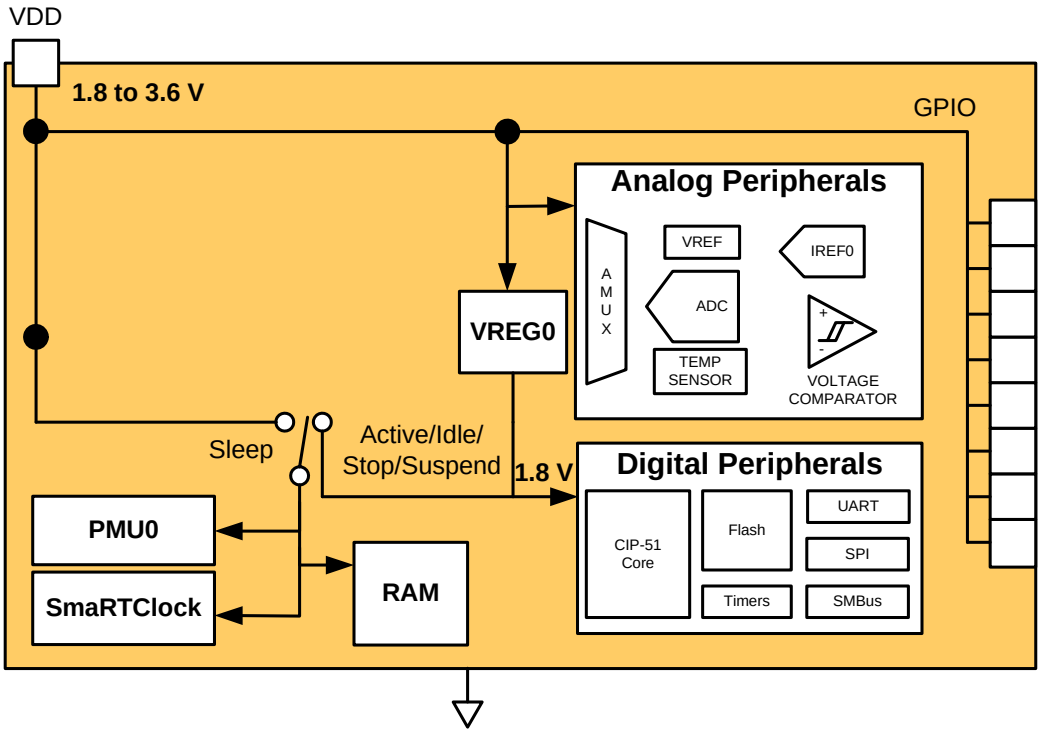

Figure 15.1. C8051F99x-C8051F98x Power Distribution

19. Clocking Sources

C8051F99x-C8051F98x devices include a programmable precision internal oscillator, an external oscillator drive circuit, a low power internal oscillator, and a SmaRTClock real time clock oscillator. The precision internal oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 19.1. The external oscillator can be configured using the OSCXCN register. The low power internal oscillator is automatically enabled and disabled when selected and deselected as a clock source. SmaRTClock operation is described in the SmaRTClock oscillator chapter.

The system clock (SYSCLK) can be derived from the precision internal oscillator, external oscillator, low power internal oscillator, low power internal oscillator divided by 8, or SmaRTClock oscillator. The global clock divider can generate a system clock that is 1, 2, 4, 8, 16, 32, 64, or 128 times slower that the selected input clock source. Oscillator electrical specifications can be found in the Electrical Specifications Chapter.

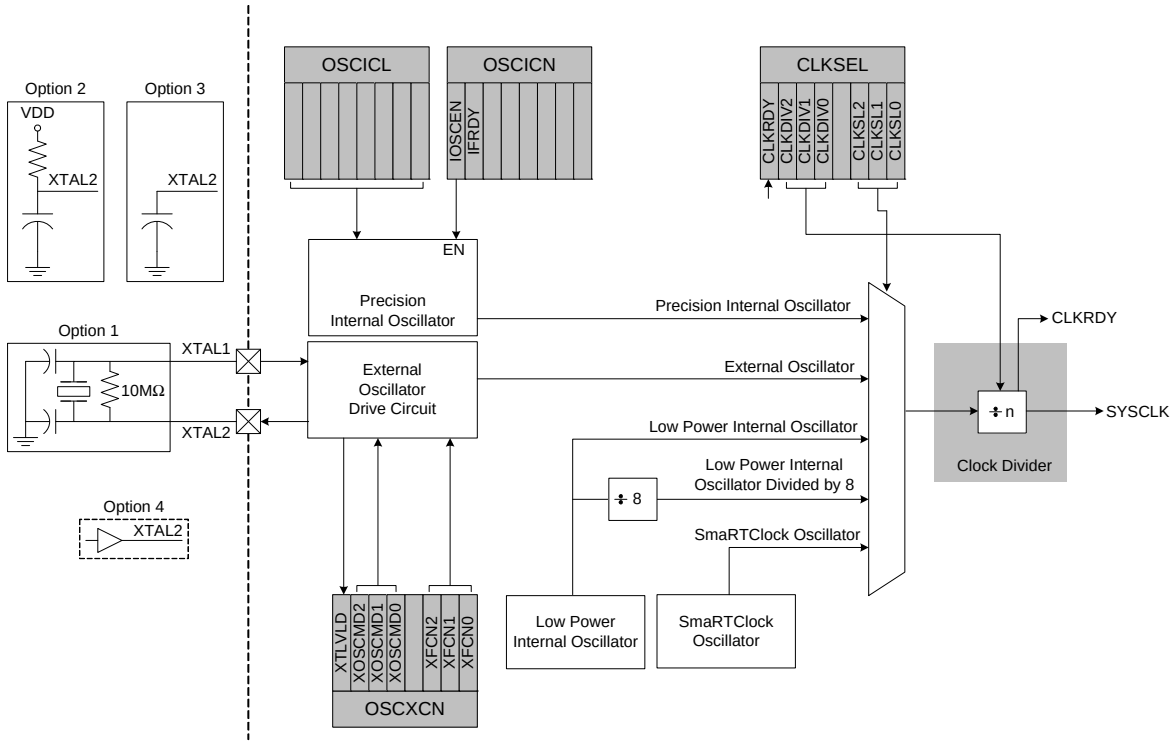

Figure 19.1. Clocking Sources Block Diagram

The proper way of changing the system clock when both the clock source and the clock divide value are being changed is as follows:

If switching from a fast “undivided” clock to a slower “undivided” clock:

1. Change the clock divide value.
2. Poll for CLKRDY > 1.
3. Change the clock source.

If switching from a slow “undivided” clock to a faster “undivided” clock:

1. Change the clock source.
2. Change the clock divide value.
3. Poll for CLKRDY > 1.

20.2.2. Using the SmaRTClock Oscillator in Self-Oscillate Mode

When using Self-Oscillate Mode, the XTAL3 and XTAL4 pins are internally shorted together. The following steps show how to configure SmaRTClock for use in Self-Oscillate Mode:

1. Set SmaRTClock to Self-Oscillate Mode (XMODE = 0).
2. Set the desired oscillation frequency:
   For oscillation at about 20 kHz, set BIASX2 = 0.
   For oscillation at about 40 kHz, set BIASX2 = 1.
3. The oscillator starts oscillating instantaneously.
4. Fine tune the oscillation frequency by adjusting the load capacitance (RTC0XCF).

20.2.3. Using the Low Frequency Oscillator (LFO)

The low frequency oscillator provides an ultra low power, on-chip clock source to the SmaRTClock. The typical frequency of oscillation is 16.4 kHz ±20%. No external components are required to use the LFO and the XTAL3 and XTAL4 pins do not need to be shorted together.

The following steps show how to configure SmaRTClock for use with the LFO:

1. Enable and select the Low Frequency Oscillator (LFOEN = 1).
2. The LFO starts oscillating instantaneously.

When the LFO is enabled, the SmaRTClock oscillator increments bit 1 of the 32-bit timer (instead of bit 0). This effectively multiplies the LFO frequency by 2, making the RTC timebase behave as if a 32.768 kHz crystal is connected at the output.

SFR Definition 21.15. P1MDIN: Port1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = 0x0; SFR Address = 0xF2

Bit	Name	Function
7:0	P1MDIN[7:0]	**Analog Configuration Bits for P1.7–P1.0 (respectively).** Port pins configured for analog mode have their weak pullup and digital receiver disabled. The digital driver is not explicitly disabled. 0: Corresponding P1.n pin is configured for analog mode. 1: Corresponding P1.n pin is not configured for analog mode.

SFR Definition 21.16. P1MDOUT: Port1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xA5

Bit	Name	Function
7:0	P1MDOUT[7:0]	**Output Configuration Bits for P1.7–P1.0 (respectively).** These bits control the digital driver even when the corresponding bit in register P1MDIN is logic 0. 0: Corresponding P1.n Output is open-drain. 1: Corresponding P1.n Output is push-pull.

Setting the EXTHOLD bit extends the minimum setup and hold times for the SDA line. The minimum SDA setup time defines the absolute minimum time that SDA is stable before SCL transitions from low-to-high. The minimum SDA hold time defines the absolute minimum time that the current SDA value remains stable after SCL transitions from high-to-low. EXTHOLD should be set so that the minimum setup and hold times meet the SMBus Specification requirements of 250 ns and 300 ns, respectively. Table 22.2 shows the minimum setup and hold times for the two EXTHOLD settings. Setup and hold time extensions are typically necessary when SYSCLK is above 10 MHz.

Table 22.2. Minimum SDA Setup and Hold Times

EXTHOLD	Minimum SDA Setup Time	Minimum SDA Hold Time
0	T_{low} – 4 system clocks or 1 system clock + s/w delay*	3 system clocks
1	11 system clocks	12 system clocks

***Note:** Setup Time for ACK bit transmissions and the MSB of all data transfers. When using software acknowledgement, the s/w delay occurs between the time SMB0DAT or ACK is written and when SI is cleared. Note that if SI is cleared in the same write that defines the outgoing ACK value, s/w delay is zero.

With the SMBTOE bit set, Timer 3 should be configured to overflow after 25 ms in order to detect SCL low timeouts (see Section “22.3.4. SCL Low Timeout” on page 238). The SMBus interface will force Timer 3 to reload while SCL is high, and allow Timer 3 to count when SCL is low. The Timer 3 interrupt service routine should be used to reset SMBus communication by disabling and re-enabling the SMBus.

SMBus Free Timeout detection can be enabled by setting the SMBFTE bit. When this bit is set, the bus will be considered free if SDA and SCL remain high for more than 10 SMBus clock source periods (see Figure 22.4).

22.4.4. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

SFR Definition 22.5. SMB0DAT: SMBus Data

Bit	7	6	5	4	3	2	1	0
Name	SMB0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC2

Bit	Name	Function
7:0	SMB0DAT[7:0]	**SMBus Data.** The SMB0DAT register contains a byte of data to be transmitted on the SMBus serial interface or a byte that has just been received on the SMBus serial interface. The CPU can read from or write to this register whenever the SI serial interrupt flag (SMB0CN.0) is set to logic 1. The serial data in the register remains stable as long as the SI flag is set. When the SI flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.

26.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

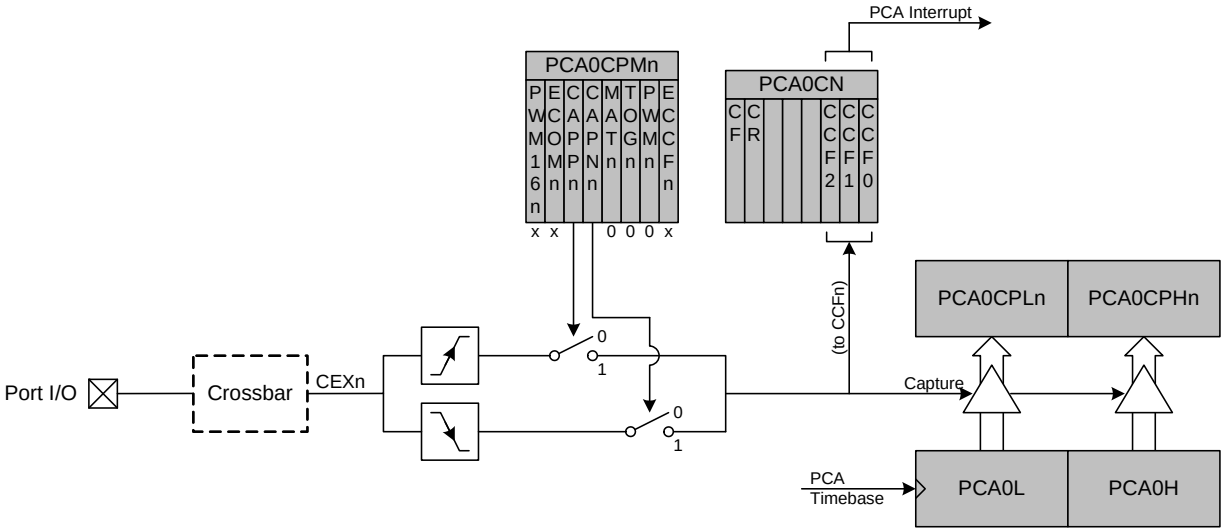

Figure 26.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

C2 Register Definition 27.4. FPCTL: C2 Flash Programming Control

Bit	7	6	5	4	3	2	1	0
Name	FPCTL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0x02

Bit	Name	Function
7:0	FPCTL[7:0]	**Flash Programming Control Register.** This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 27.5. FPDAT: C2 Flash Programming Data

Bit	7	6	5	4	3	2	1	0
Name	FPDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xB4

Bit	Name	Function	
7:0	FPDAT[7:0]	**C2 Flash Programming Data Register.** This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.	
		Code	**Command**
		0x06	Flash Block Read
		0x07	Flash Block Write
		0x08	Flash Page Erase
		0x03	Device Erase

Document Change List

Revision 0.3 to Revision 0.4

- QFN-20 package and landing diagram updated.

Revision 0.4 to Revision 1.0

- IREF0CF register description updated.
- Updated ADC0 Chapter Text.
- Corrected an error in the Product Selector Guide.
- Updated SmaRTClock chapter to indicate how the Alarm value should be set when using Auto Reset and the LFO.
- Updated electrical specifications to fill TBDs and updated power specifications based on Rev B characterization data.
- Added a note to the OSCICL register description.
- Added a note to the CRC0CN register description.
- Updated equation in the CRC0CNT register description.
- Updated Power On Reset description.

Revision 1.0 to Revision 1.1

- Removed references to AN338.

Revision 1.1 to Revision 1.2

- Removed QuickSense references.
- Updated part numbers to Revision C in “Ordering Information” on page 31 and added Figure 3.4, Figure 3.5, and Figure 3.6 to identify the silicon revision.
- Updated REVID register (SFR Definition 14.2) and REVID C2 register (C2 Register Definition 27.3) with the 0x02 value for Revision C.
- Updated Figure “7.3 CP0 Multiplexer Block Diagram” on page 98 to remove the bar over the CPnOUT signals.
- Updated the “Reset Sources” on page 181 chapter to reflect the correct state of the $\overline{\text{RST}}$ pin during power-on reset.
- Updated Figure “1.14 Port I/O Functional Block Diagram” on page 26 and Figure “21.1 Port I/O Functional Block Diagram” on page 215 to mention P1.4 is not available on 20-pin devices.
- Removed references to the EMI0CN register, which does not exist.
- Updated Figure “8.2 Auto-Scan Example” on page 103 to refer to the correct pins.
- Updated POR Monitor Threshold (V_{POR}) Brownout Condition (VDD Falling) specification minimum, typical, and maximum values.
- Updated the reset value of the CLKSEL register (SFR Definition 19.1).
- Updated description of WEAKPUD in SFR Definition 21.3.
- Corrected SFR addresses for P0DRV (SFR Definition 21.12), P1DRV (SFR Definition 21.17), P2DRV (SFR Definition 21.20), PMU0MD (SFR Definition 15.3), FLSCL (SFR Definition 14.5), REF0CN (SFR Definition 5.15), CS0SCAN0 (SFR Definition 8.5), and CS0SCAN1 (SFR Definition 8.6).
- Replaced all instances of V_{BAT} with V_{DD}.
- Added a note to “11.1. Accessing XRAM” , “15.5. Sleep Mode” , and “18. Reset Sources” regarding an issue with the first address of XRAM.
- Added a note to “15.5. Sleep Mode” and “19. Clocking Sources” regarding using the internal low power