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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I <sup>2</sup> C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/c8051f986-c-gu">https://www.e-xfl.com/product-detail/silicon-labs/c8051f986-c-gu</a>

# C8051F99x-C8051F98x

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22.3.SMBus Operation .....	237
22.3.1.Transmitter vs. Receiver .....	237
22.3.2.Arbitration.....	238
22.3.3.Clock Low Extension.....	238
22.3.4.SCL Low Timeout.....	238
22.3.5.SCL High (SMBus Free) Timeout .....	238
22.4.Using the SMBus.....	239
22.4.1.SMBus Configuration Register.....	240
22.4.2.SMB0CN Control Register .....	243
22.4.3.Hardware Slave Address Recognition .....	246
22.4.4.Data Register .....	248
22.5.SMBus Transfer Modes.....	249
22.5.1.Write Sequence (Master) .....	249
22.5.2.Read Sequence (Master) .....	250
22.5.3.Write Sequence (Slave) .....	251
22.5.4.Read Sequence (Slave).....	252
22.6.SMBus Status Decoding.....	252
<b>23. UART0.....</b>	<b>257</b>
23.1.Enhanced Baud Rate Generation.....	258
23.2.Operational Modes .....	259
23.2.1.8-Bit UART .....	259
23.2.2.9-Bit UART .....	260
23.3.Multiprocessor Communications .....	260
<b>24. Enhanced Serial Peripheral Interface (SPI0).....</b>	<b>265</b>
24.1.Signal Descriptions.....	266
24.1.1.Master Out, Slave In (MOSI).....	266
24.1.2.Master In, Slave Out (MISO).....	266
24.1.3.Serial Clock (SCK) .....	266
24.1.4.Slave Select (NSS) .....	266
24.2.SPI0 Master Mode Operation .....	266
24.3.SPI0 Slave Mode Operation .....	268
24.4.SPI0 Interrupt Sources .....	269
24.5.Serial Clock Phase and Polarity .....	269
24.6.SPI Special Function Registers .....	271
<b>25. Timers.....</b>	<b>278</b>
25.1.Timer 0 and Timer 1 .....	280
25.1.1.Mode 0: 13-bit Counter/Timer .....	280
25.1.2.Mode 1: 16-bit Counter/Timer .....	281
25.1.3.Mode 2: 8-bit Counter/Timer with Auto-Reload.....	282
25.1.4.Mode 3: Two 8-bit Counter/Timers (Timer 0 Only).....	283
25.2.Timer 2 .....	288
25.2.1.16-bit Timer with Auto-Reload.....	288
25.2.2.8-bit Timers with Auto-Reload.....	289
25.2.3.Comparator 0/SmaRTClock Capture Mode .....	290
25.3.Timer 3 .....	294

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Figure 5.10. Voltage Reference Functional Block Diagram.....	88
Figure 7.1. Comparator 0 Functional Block Diagram .....	93
Figure 7.2. Comparator Hysteresis Plot .....	95
Figure 7.3. CP0 Multiplexer Block Diagram.....	98
Figure 8.1. CS0 Block Diagram .....	100
Figure 8.2. Auto-Scan Example.....	103
Figure 8.3. CS0 Multiplexer Block Diagram.....	117
Figure 9.1. CIP-51 Block Diagram.....	119
Figure 10.1. C8051F99x-C8051F98x Memory Map .....	128
Figure 10.2. Flash Program Memory Map.....	129
Figure 14.1. Flash Program Memory Map (8 kB and smaller devices) .....	152
Figure 15.1. C8051F99x-C8051F98x Power Distribution.....	163
Figure 16.1. CRC0 Block Diagram .....	172
Figure 16.2. Bit Reverse Register .....	179
Figure 18.1. Reset Sources.....	181
Figure 18.2. Power-Fail Reset Timing Diagram .....	182
Figure 19.1. Clocking Sources Block Diagram .....	188
Figure 19.2. 25 MHz External Crystal Example.....	190
Figure 20.1. SmaRTClock Block Diagram.....	197
Figure 20.2. Interpreting Oscillation Robustness (Duty Cycle) Test Results.....	206
Figure 21.1. Port I/O Functional Block Diagram .....	215
Figure 21.2. Port I/O Cell Block Diagram .....	216
Figure 21.3. Peripheral Availability on Port I/O Pins.....	219
Figure 21.4. Crossbar Priority Decoder in Example Configuration (No Pins Skipped). 220	
Figure 21.5. Crossbar Priority Decoder in Example Configuration (4 Pins Skipped) .....	220
Figure 22.1. SMBus Block Diagram .....	235
Figure 22.2. Typical SMBus Configuration .....	236
Figure 22.3. SMBus Transaction.....	237
Figure 22.4. Typical SMBus SCL Generation.....	240
Figure 22.5. Typical Master Write Sequence .....	249
Figure 22.6. Typical Master Read Sequence .....	250
Figure 22.7. Typical Slave Write Sequence .....	251
Figure 22.8. Typical Slave Read Sequence .....	252
Figure 23.1. UART0 Block Diagram .....	257
Figure 23.2. UART0 Baud Rate Logic.....	258
Figure 23.3. UART Interconnect Diagram .....	259
Figure 23.4. 8-Bit UART Timing Diagram.....	259
Figure 23.5. 9-Bit UART Timing Diagram.....	260
Figure 23.6. UART Multi-Processor Mode Interconnect Diagram .....	261
Figure 24.1. SPI Block Diagram .....	265
Figure 24.2. Multiple-Master Mode Connection Diagram .....	267
Figure 24.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram 267	

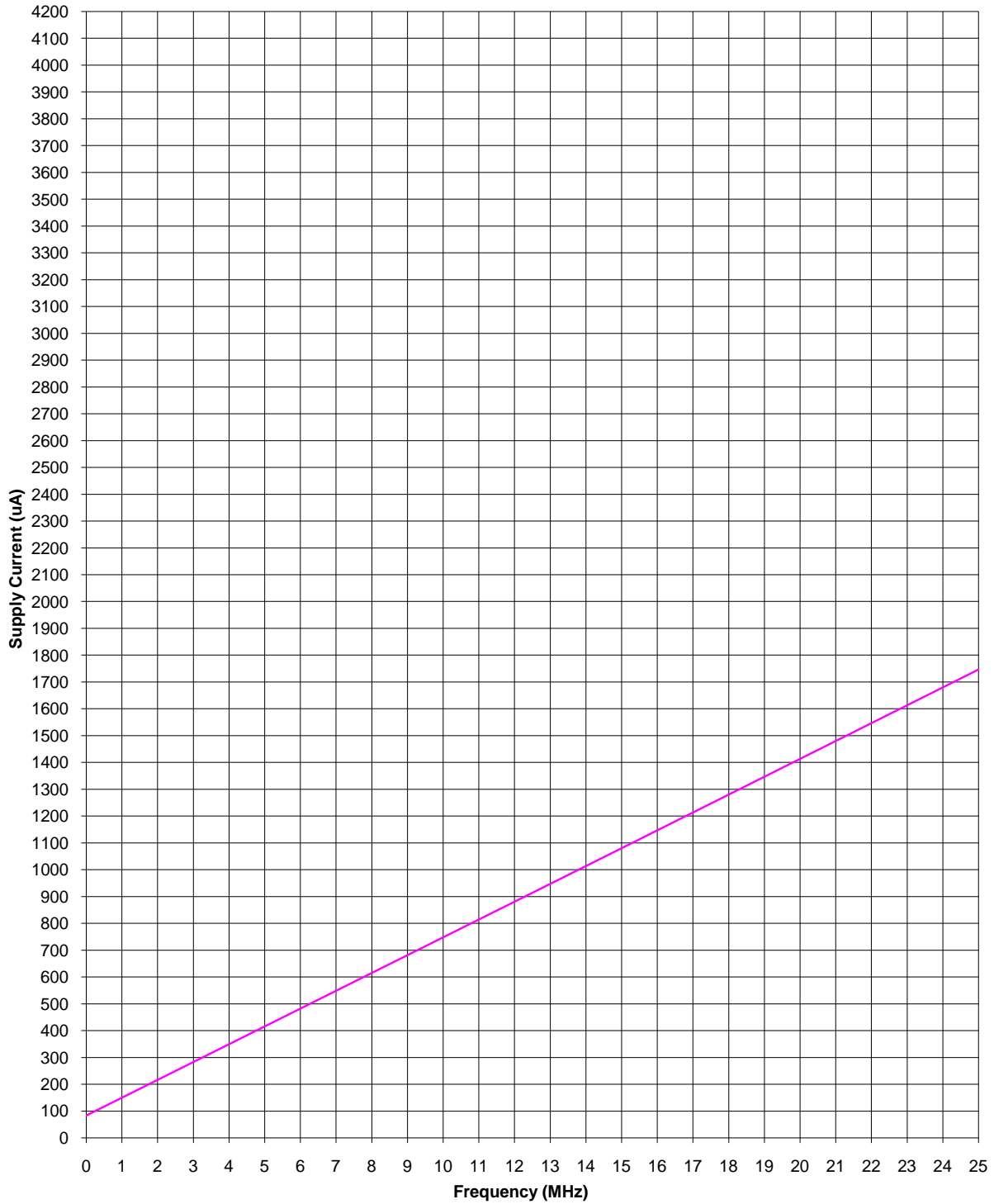
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# C8051F99x-C8051F98x

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SFR Definition 13.2. IP: Interrupt Priority	143
SFR Definition 13.3. EIE1: Extended Interrupt Enable 1	144
SFR Definition 13.4. EIP1: Extended Interrupt Priority 1	145
SFR Definition 13.5. EIE2: Extended Interrupt Enable 2	146
SFR Definition 13.6. EIP2: Extended Interrupt Priority 2	147
SFR Definition 13.7. IT01CF: INT0/INT1 Configuration	149
SFR Definition 14.1. DEVICEID: Device Identification	154
SFR Definition 14.2. REVID: Revision Identification	155
SFR Definition 14.3. PSCTL: Program Store R/W Control	159
SFR Definition 14.4. FLKEY: Flash Lock and Key	160
SFR Definition 14.5. FLSCL: Flash Scale	161
SFR Definition 14.6. FLWR: Flash Write Only	161
SFR Definition 15.1. PMU0CF: Power Management Unit Configuration <sup>1,2,3</sup>	168
SFR Definition 15.2. PMU0FL: Power Management Unit Flag <sup>1,2</sup>	169
SFR Definition 15.3. PMU0MD: Power Management Unit Mode	170
SFR Definition 15.4. PCON: Power Management Control Register	171
SFR Definition 16.1. CRC0CN: CRC0 Control	175
SFR Definition 16.2. CRC0IN: CRC0 Data Input	176
SFR Definition 16.3. CRC0DAT: CRC0 Data Output	176
SFR Definition 16.4. CRC0AUTO: CRC0 Automatic Control	177
SFR Definition 16.5. CRC0CNT: CRC0 Automatic Flash Sector Count	178
SFR Definition 16.6. CRC0FLIP: CRC0 Bit Flip	179
SFR Definition 17.1. REG0CN: Voltage Regulator Control	180
SFR Definition 18.1. VDM0CN: VDD Supply Monitor Control	184
SFR Definition 18.2. RSTSRC: Reset Source	187
SFR Definition 19.1. CLKSEL: Clock Select	193
SFR Definition 19.2. OSCICN: Internal Oscillator Control	194
SFR Definition 19.3. OSCICL: Internal Oscillator Calibration	195
SFR Definition 19.4. OSCXCN: External Oscillator Control	196
SFR Definition 20.1. RTC0KEY: SmARTClock Lock and Key	201
SFR Definition 20.2. RTC0ADR: SmARTClock Address	202
SFR Definition 20.3. RTC0DAT: SmARTClock Data	202
Internal Register Definition 20.4. RTC0CN: SmARTClock Control	211
Internal Register Definition 20.5. RTC0XCN: SmARTClock Oscillator Control	212
Internal Register Definition 20.6. RTC0XCF: SmARTClock Oscillator Configuration	213
Internal Register Definition 20.7. CAPTUREn: SmARTClock Timer Capture	214
Internal Register Definition 20.8. ALARMn: SmARTClock Alarm Programmed Value	214
SFR Definition 21.1. XBR0: Port I/O Crossbar Register 0	222
SFR Definition 21.2. XBR1: Port I/O Crossbar Register 1	223
SFR Definition 21.3. XBR2: Port I/O Crossbar Register 2	224
SFR Definition 21.4. P0MASK: Port0 Mask Register	225
SFR Definition 21.5. P0MAT: Port0 Match Register	225
SFR Definition 21.6. P1MASK: Port1 Mask Register	226
SFR Definition 21.7. P1MAT: Port1 Match Register	226
SFR Definition 21.8. P0: Port0	228

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**Figure 4.2. Idle Mode Current (External CMOS Clock)**

# C8051F99x-C8051F98x

**Table 4.5. Power Management Electrical Specifications**

$V_{DD} = 1.8$  to  $3.6$  V,  $-40$  to  $+85$  °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Idle Mode Wake-up Time		2	—	3	SYCLKs
Suspend Mode Wake-up Time	CLKDIV = 0x00 Low Power or Precision Osc.	—	400	—	ns
Sleep Mode Wake-up Time		—	2	—	μs

**Table 4.6. Flash Electrical Characteristics**

$V_{DD} = 1.8$  to  $3.6$  V,  $-40$  to  $+85$  °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	C8051F980/1/6/7, C8051F990/1/6/7	8192	—	—	bytes
	C8051F982/3/8/9	4096	—	—	bytes
	C8051F985	2048	—	—	bytes
Endurance		20 k	100k	—	Erase/Write Cycles
Erase Cycle Time		28	32	36	ms
Write Cycle Time		57	64	71	μs

**Table 4.7. Internal Precision Oscillator Electrical Characteristics**

$V_{DD} = 1.8$  to  $3.6$  V;  $T_A = -40$  to  $+85$  °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	$-40$ to $+85$ °C, $V_{DD} = 1.8$ – $3.6$ V	24	24.5	25	MHz
Oscillator Supply Current (from $V_{DD}$ )	25 °C; includes bias current of 90–100 μA	—	300*	—	μA

\*Note: Does not include clock divider or clock tree supply current.

**Table 4.8. Internal Low-Power Oscillator Electrical Characteristics**

$V_{DD} = 1.8$  to  $3.6$  V;  $T_A = -40$  to  $+85$  °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	$-40$ to $+85$ °C, $V_{DD} = 1.8$ – $3.6$ V	18	20	22	MHz
Oscillator Supply Current (from $V_{DD}$ )	25 °C No separate bias current required	—	100*	—	μA

\*Note: Does not include clock divider or clock tree supply current.

**Table 4.12. Voltage Reference Electrical Characteristics**

$V_{DD}$  = 1.8 to 3.6 V, -40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
<b>Internal High-Speed Reference (REFSL[1:0] = 11)</b>					
Output Voltage	-40 to +85 °C, $V_{DD}$ = 1.8–3.6 V	1.62	1.65	1.68	V
VREF Turn-on Time		—	—	1.5	μs
Supply Current	Normal Power Mode Low Power Mode	— —	260 140	— —	μA
<b>External Reference (REFSL[1:0] = 00, REFOE = 0)</b>					
Input Voltage Range		0	—	$V_{DD}$	V
Input Current	Sample Rate = 300 ksps; VREF = 3.0 V	—	5.25	—	μA

# C8051F99x-C8051F98x

**Table 4.13. IREF0 Electrical Characteristics**

$V_{DD}$  = 1.8 to 3.6 V, -40 to +85 °C, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
<b>Static Performance</b>					
Resolution		6			bits
Output Compliance Range	Low Power Mode, Source	0	—	$V_{DD} - 0.4$	V
	High Current Mode, Source	0	—	$V_{DD} - 0.8$	
	Low Power Mode, Sink	0.3	—	$V_{DD}$	
	High Current Mode, Sink	0.8	—	$V_{DD}$	
Integral Nonlinearity		—	$<\pm 0.2$	$\pm 1.0$	LSB
Differential Nonlinearity		—	$<\pm 0.2$	$\pm 1.0$	LSB
Offset Error		—	$<\pm 0.1$	$\pm 0.5$	LSB
Full Scale Error	Low Power Mode, Source	—	—	$\pm 5$	%
	High Current Mode, Source	—	—	$\pm 6$	%
	Low Power Mode, Sink	—	—	$\pm 8$	%
	High Current Mode, Sink	—	—	$\pm 8$	%
Absolute Current Error	Low Power Mode Sourcing 20 $\mu$ A	—	$<\pm 1$	$\pm 3$	%
<b>Dynamic Performance</b>					
Output Settling Time to 1/2 LSB		—	300	—	ns
Startup Time		—	1	—	$\mu$ s
<b>Power Consumption</b>					
Net Power Supply Current ( $V_{DD}$ supplied to IREF0 minus any output source current)	Low Power Mode, Source				
	IREF0DAT = 000001	—	10	—	$\mu$ A
	IREF0DAT = 111111	—	10	—	$\mu$ A
	High Current Mode, Source				
	IREF0DAT = 000001	—	10	—	$\mu$ A
	IREF0DAT = 111111	—	10	—	$\mu$ A
	Low Power Mode, Sink				
	IREF0DAT = 000001	—	1	—	$\mu$ A
	IREF0DAT = 111111	—	11	—	$\mu$ A
	High Current Mode, Sink				
IREF0DAT = 000001	—	12	—	$\mu$ A	
IREF0DAT = 111111	—	81	—	$\mu$ A	
<b>Note:</b> Refer to “PWM Enhanced Mode” on page 91 for information on how to improve IREF0 resolution.					



# C8051F99x-C8051F98x

## 7. Comparator

C8051F99x-C8051F98x devices include an on-chip programmable voltage comparator: Comparator 0 (CPT0) shown in Figure 7.1.

The Comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a digital synchronous “latched” output (CP0), or a digital asynchronous “raw” output (CP0A). The asynchronous CP0A signal is available even when the system clock is not active. This allows the Comparator to operate and generate an output when the device is in some low power modes.

### 7.1. Comparator Inputs

Each Comparator performs an analog comparison of the voltage levels at its positive (CP0+) and negative (CP0-) input. The analog input multiplexers are completely under software control and configured using SFR registers. See Section “7.6. Comparator0 Analog Multiplexer” on page 98 for details on how to select and configure Comparator inputs.

**Important Note About Comparator Inputs:** The Port pins selected as Comparator inputs should be configured as analog inputs and skipped by the Crossbar. See the Port I/O chapter for more details on how to configure Port I/O pins as Analog Inputs. The Comparator may also be used to compare the logic level of digital signals, however, Port I/O pins configured as digital inputs must be driven to a valid logic state (HIGH or LOW) to avoid increased power consumption.

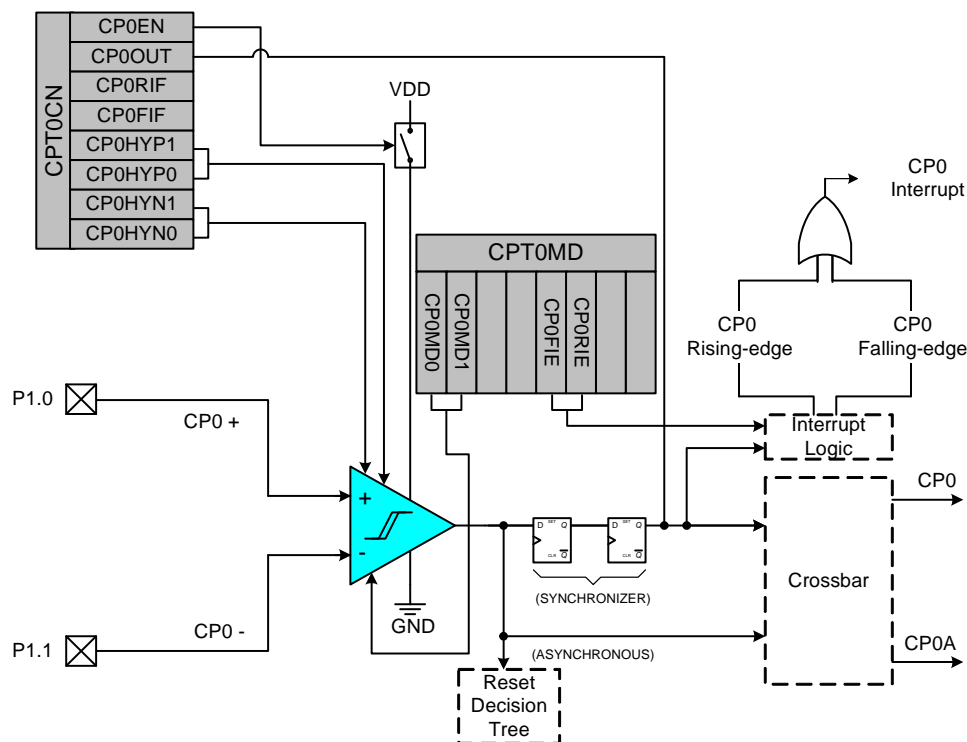


Figure 7.1. Comparator 0 Functional Block Diagram

# C8051F99x-C8051F98x

## 8.14. Capacitive Sense Multiplexer

The input multiplexer can be controlled through two methods. The CS0MX register can be written to through firmware, or the register can be configured automatically using the modules auto-scan functionality (see “8.8. Automatic Scanning (Method 1—CS0SMEN = 0)” ).

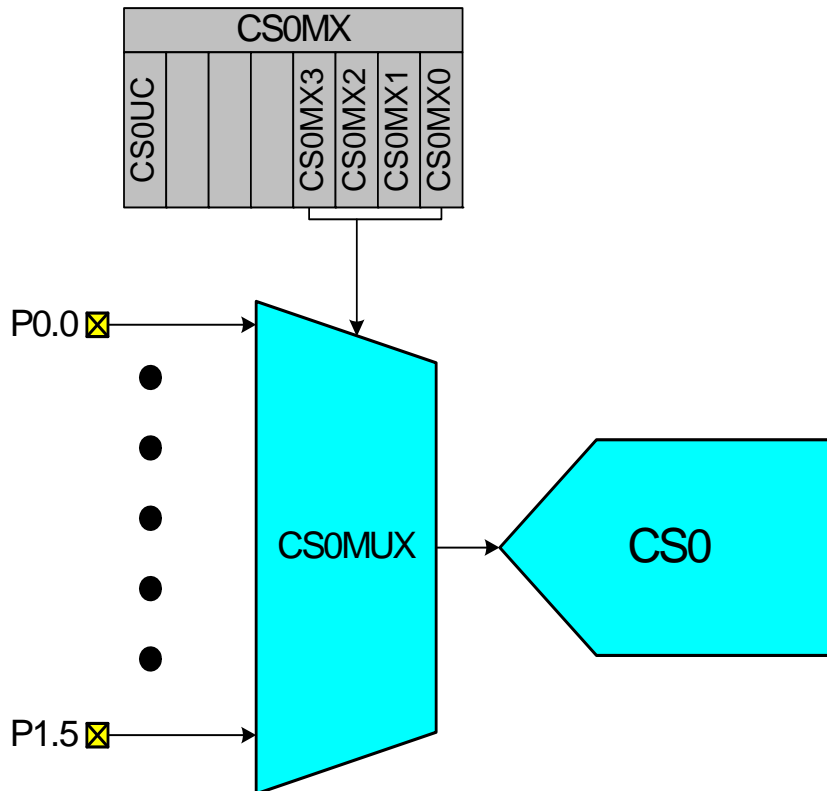


Figure 8.3. CS0 Multiplexer Block Diagram

## Notes on Registers, Operands and Addressing Modes:

**Rn**—Register R0–R7 of the currently selected register bank.

**@Ri**—Data RAM location addressed indirectly through R0 or R1.

**rel**—8-bit, signed (twos complement) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps.

**direct**—8-bit internal data location's address. This could be a direct-access Data RAM location (0x00–0x7F) or an SFR (0x80–0xFF).

**#data**—8-bit constant

**#data16**—16-bit constant

**bit**—Direct-accessed bit in Data RAM or SFR

**addr11**—11-bit destination address used by ACALL and AJMP. The destination must be within the same 2 kB page of program memory as the first byte of the following instruction.

**addr16**—16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8 kB program memory space.

There is one unused opcode (0xA5) that performs the same function as NOP.  
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# C8051F99x-C8051F98x

## SFR Definition 9.6. PSW: Program Status Word

Bit	7	6	5	4	3	2	1	0
Name	CY	AC	F0	RS[1:0]		OV	F1	PARITY
Type	R/W	R/W	R/W	R/W		R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0xD0; Bit-Addressable

Bit	Name	Function
7	CY	<b>Carry Flag.</b> This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to logic 0 by all other arithmetic operations.
6	AC	<b>Auxiliary Carry Flag.</b> This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to logic 0 by all other arithmetic operations.
5	F0	<b>User Flag 0.</b> This is a bit-addressable, general purpose flag for use under software control.
4:3	RS[1:0]	<b>Register Bank Select.</b> These bits select which register bank is used during register accesses. 00: Bank 0, Addresses 0x00-0x07 01: Bank 1, Addresses 0x08-0x0F 10: Bank 2, Addresses 0x10-0x17 11: Bank 3, Addresses 0x18-0x1F
2	OV	<b>Overflow Flag.</b> This bit is set to 1 under the following circumstances: <ul style="list-style-type: none"> <li>• An ADD, ADDC, or SUBB instruction causes a sign-change overflow.</li> <li>• A MUL instruction results in an overflow (result is greater than 255).</li> <li>• A DIV instruction causes a divide-by-zero condition.</li> </ul> The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.
1	F1	<b>User Flag 1.</b> This is a bit-addressable, general purpose flag for use under software control.
0	PARITY	<b>Parity Flag.</b> This bit is set to logic 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

# C8051F99x-C8051F98x

## SFR Definition 12.1. SFR Page: SFR Page

Bit	7	6	5	4	3	2	1	0
Name	SFRPAGE[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0xA7

Bit	Name	Function
7:0	SFRPAGE[7:0]	<b>SFR Page.</b> Specifies the SFR Page used when reading, writing, or modifying special function registers.

**Table 12.3. Special Function Registers**

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page
ACC	0xE0	All	Accumulator	126
ADC0AC	0xBA	0x0	ADC0 Accumulator Configuration	76
ADC0CF	0x97	0x0	ADC0 Configuration	75
ADC0CN	0xE8	0x0	ADC0 Control	74
ADC0GTH	0xC4	0x0	ADC0 Greater-Than Compare High	80
ADC0GTL	0xC3	0x0	ADC0 Greater-Than Compare Low	80
ADC0H	0xBE	0x0	ADC0 High	79
ADC0L	0xBD	0x0	ADC0 Low	79
ADC0LTH	0xC6	0x0	ADC0 Less-Than Compare Word High	81
ADC0LTL	0xC5	0x0	ADC0 Less-Than Compare Word Low	81
ADC0MX	0x96	0x0	AMUX0 Channel Select	84
ADC0PWR	0xBB	All	ADC0 Burst Mode Power-Up Time	77
ADC0TK	0xBC	All	ADC0 Tracking Control	78
B	0xF0	All	B Register	126
CKCON	0x8E	0x0	Clock Control	279
CLKSEL	0xA9	All	Clock Select	193
CPT0CN	0x9B	0x0	Comparator0 Control	96
CPT0MD	0x9D	0x0	Comparator0 Mode Selection	97
CPT0MX	0x9F	0x0	Comparator0 Mux Selection	99
CRC0AUTO	0x9E	All	CRC0 Automatic Control	177
CRC0CN	0x84	All	CRC0 Control	175
CRC0CNT	0x9A	All	CRC0 Automatic Flash Sector Count	178
CRC0DAT	0x86	All	CRC0 Data	176
CRC0FLIP	0x9C	All	CRC0 Flip	179
CRC0IN	0x85	All	CRC0 Input	176
CS0CF	0xAA	0x0	CS0 Configuration	108
CS0CN	0xB0	0x0	CS0 Control	107

## 15.1. Normal Mode

The MCU is fully functional in normal mode. Figure 15.1 shows the on-chip power distribution to various peripherals. There are two supply voltages powering various sections of the chip:  $V_{DD}$  and the 1.8 V internal core supply. All analog peripherals are directly powered from the  $V_{DD}$  pin. All digital peripherals and the CIP-51 core are powered from the 1.8 V internal core supply. RAM, PMU0 and the SmarTClock are always powered directly from the  $V_{DD}$  pin in sleep mode and powered from the core supply in all other power modes.

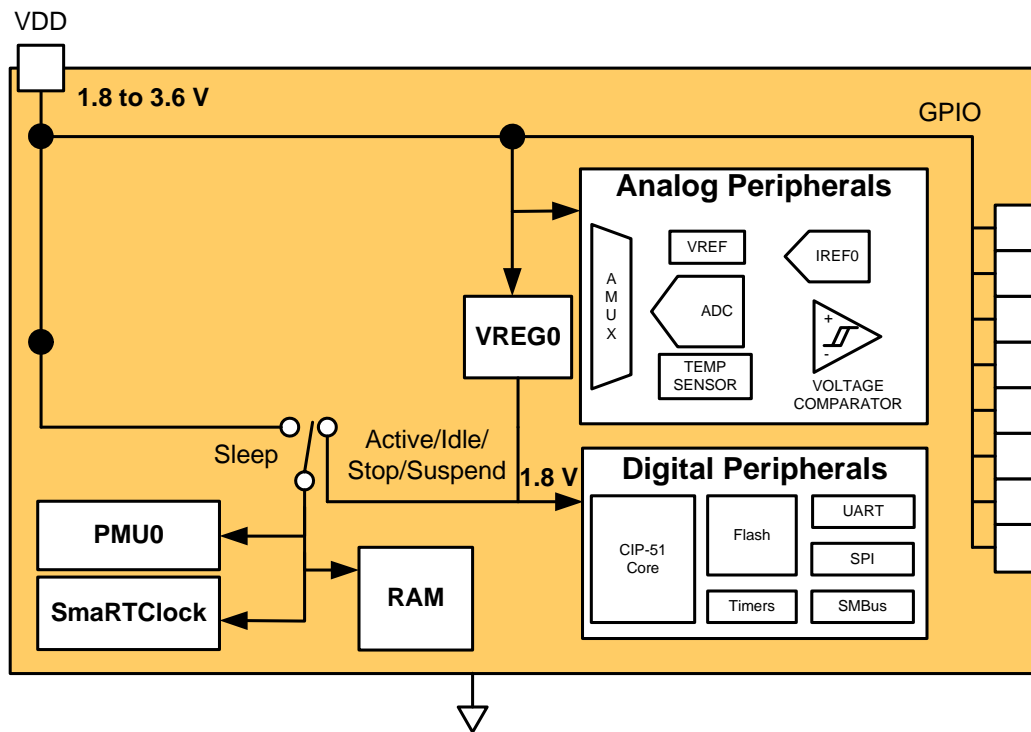


Figure 15.1. C8051F99x-C8051F98x Power Distribution

# C8051F99x-C8051F98x

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## 16.2. Preparing for a CRC Calculation

To prepare CRC0 for a CRC calculation, software should set the initial value of the result. The polynomial used for the CRC computation is 0x1021. The CRC0 result may be initialized to one of two values: 0x0000 or 0xFFFF. The following steps can be used to initialize CRC0.

1. Select the initial result value (Set CRC0VAL to 0 for 0x0000 or 1 for 0xFFFF).
2. Set the result to its initial value (Write 1 to CRC0INIT).

## 16.3. Performing a CRC Calculation

Once CRC0 is initialized, the input data stream is sequentially written to CRC0IN, one byte at a time. The CRC0 result is automatically updated after each byte is written. The CRC engine may also be configured to automatically perform a CRC on one or more 256 byte blocks. The following steps can be used to automatically perform a CRC on Flash memory.

1. Prepare CRC0 for a CRC calculation as shown above.
2. Write the index of the starting page to CRC0AUTO.
3. Set the AUTOEN bit in CRC0AUTO.
4. Write the number of 256 byte blocks to perform in the CRC calculation to CRC0CNT.
5. Write any value to CRC0CN (or OR its contents with 0x00) to initiate the CRC calculation. The CPU will not execute any additional code until the CRC operation completes. **See the note in SFR Definition 16.1. CRC0CN: CRC0 Control for more information on how to properly initiate a CRC calculation.**
6. Clear the AUTOEN bit in CRC0AUTO.
7. Read the CRC result using the procedure below.

## 16.4. Accessing the CRC0 Result

The internal CRC0 result is 16 bits. The CRC0PNT bits select the byte that is targeted by read and write operations on CRC0DAT and increment after each read or write. The calculation result will remain in the internal CR0 result register until it is set, overwritten, or additional data is written to CRC0IN.

# C8051F99x-C8051F98x

## 18. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled

All SFRs are reset to the predefined values noted in the SFR descriptions. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. Since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pullups are enabled during and after the reset. For power-on resets, the  $\overline{\text{RST}}$  pin is high-impedance with the weak pull-up off until the device exits the reset state. For  $V_{\text{DD}}$  Monitor resets, the  $\overline{\text{RST}}$  pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. Refer to Section “19. Clocking Sources” on page 188 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source (Section “26.4. Watchdog Timer Mode” on page 311 details the use of the Watchdog Timer). Program execution begins at location 0x0000.

**Important Note:** On device reset or upon waking up from Sleep mode, address 0x0000 of external memory may be overwritten by an indeterminate value. The indeterminate value is 0x00 in most situations. A dummy variable should be placed at address 0x0000 in external memory to ensure that the application firmware does not store any data that needs to be retained during sleep or reset at this memory location.

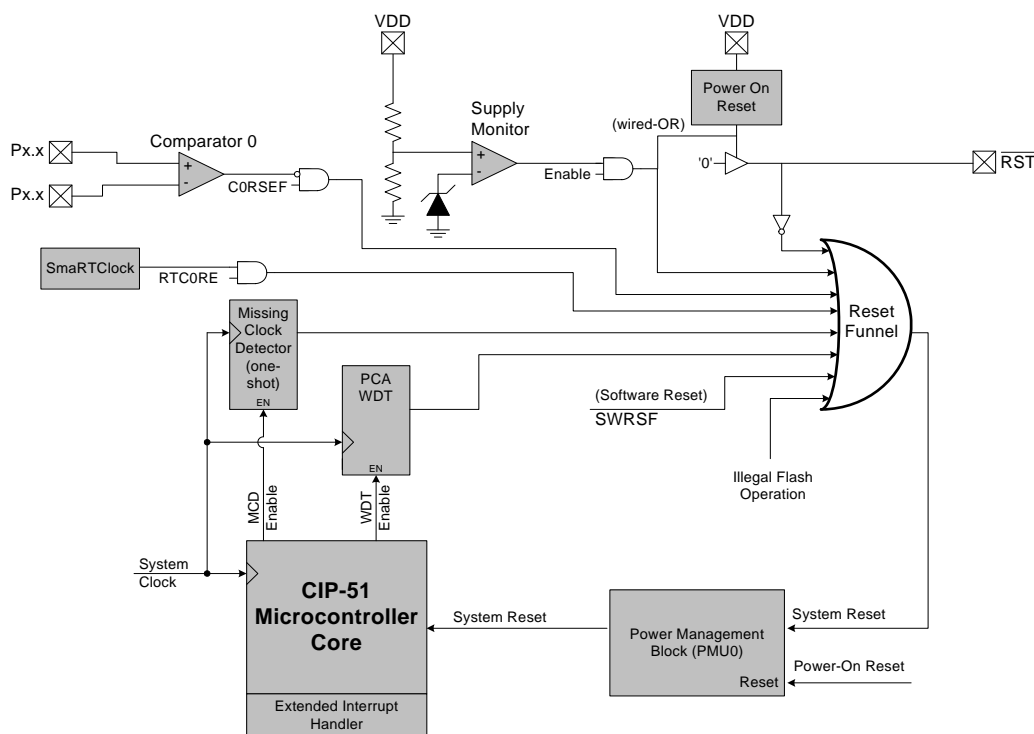


Figure 18.1. Reset Sources



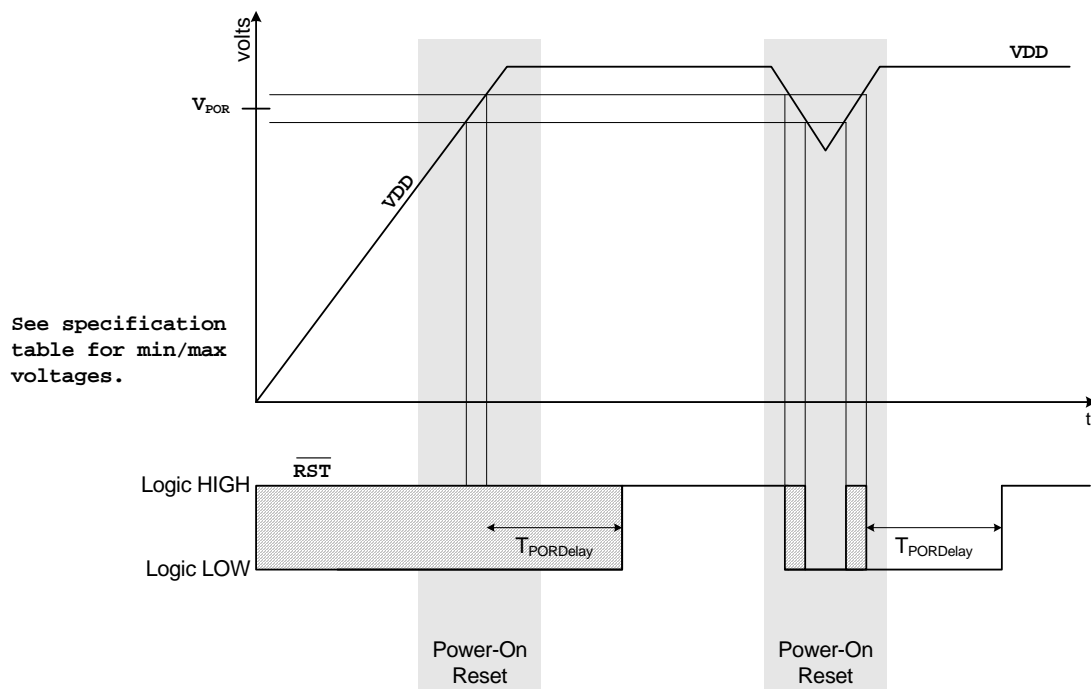
## 18.1. Power-On Reset

During power-up, the device is held in a reset state and the  $\overline{\text{RST}}$  pin voltage tracks  $V_{\text{DD}}$  (through a weak pull-up) until the device is released from reset. After  $V_{\text{DD}}$  settles above  $V_{\text{POR}}$ , a delay occurs before the device is released from reset; the delay decreases as the  $V_{\text{DD}}$  ramp time increases ( $V_{\text{DD}}$  ramp time is defined as how fast  $V_{\text{DD}}$  ramps from 0 V to  $V_{\text{POR}}$ ). Figure 18.2 plots the power-on and  $V_{\text{DD}}$  monitor reset timing. For valid ramp times (less than 3 ms), the power-on reset delay ( $T_{\text{PORDelay}}$ ) is typically 7 ms ( $V_{\text{DD}} = 1.8 \text{ V}$ ) or 15 ms ( $V_{\text{DD}} = 3.6 \text{ V}$ ).

**Note:** The maximum  $V_{\text{DD}}$  ramp time is 3 ms; slower ramp times may cause the device to be released from reset before  $V_{\text{DD}}$  reaches the  $V_{\text{POR}}$  level.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset.

The POR supply monitor can be disabled to save power by writing 1 to the MONDIS (PMU0MD.5) bit. When the POR supply monitor is disabled, all reset sources will trigger a full POR and will re-enable the POR supply monitor.



**Figure 18.2. Power-Fail Reset Timing Diagram**

## Internal Register Definition 20.5. RTC0XCN: SmaRTClock Oscillator Control

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	AGCEN	XMODE	BIASX2	CLKVLD	LFOEN			
<b>Type</b>	R/W	R/W	R/W	R	R	R	R	R
<b>Reset</b>	0	0	0	0	0	0	0	0

SmaRTClock Address = 0x05

Bit	Name	Function
7	AGCEN	<b>SmaRTClock Oscillator Automatic Gain Control (AGC) Enable.</b> 0: AGC disabled. 1: AGC enabled.
6	XMODE	<b>SmaRTClock Oscillator Mode.</b> Selects Crystal or Self Oscillate Mode. 0: Self-Oscillate Mode selected. 1: Crystal Mode selected.
5	BIASX2	<b>SmaRTClock Oscillator Bias Double Enable.</b> <b>Enables/disables the Bias Double feature.</b> 0: Bias Double disabled. 1: Bias Double enabled.
4	CLKVLD	<b>SmaRTClock Oscillator Crystal Valid Indicator.</b> Indicates if oscillation amplitude is sufficient for maintaining oscillation. 0: Oscillation has not started or oscillation amplitude is too low to maintain oscillation. 1: Sufficient oscillation amplitude detected.
3	LFOEN	<b>Low Frequency Oscillator Enable and Select.</b> Overrides XMODE and selects the internal low frequency oscillator (LFO) as the SmaRTClock oscillator source. 0: XMODE determines SmaRTClock oscillator source. 1: LFO enabled and selected as SmaRTClock oscillator source.
2:0	Unused	Read = 000b; Write = Don't Care.

## 22.1. Supporting Documents

It is assumed the reader is familiar with or has access to the following supporting documents:

- The I<sup>2</sup>C-Bus and How to Use It (including specifications), Philips Semiconductor.
- The I<sup>2</sup>C-Bus Specification—Version 2.0, Philips Semiconductor.
- System Management Bus Specification—Version 1.1, SBS Implementers Forum.

## 22.2. SMBus Configuration

Figure 22.2 shows a typical SMBus configuration. The SMBus specification allows any recessive voltage between 3.0 V and 5.0 V; different devices on the bus may operate at different voltage levels.

**Note:** The port pins on C8051F99x-C8051F98x devices are not 5 V tolerant, therefore, the device may only be used in SMBus networks where the supply voltage does not exceed  $V_{DD}$ .

The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pullup resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus not exceed 300 ns and 1000 ns, respectively.

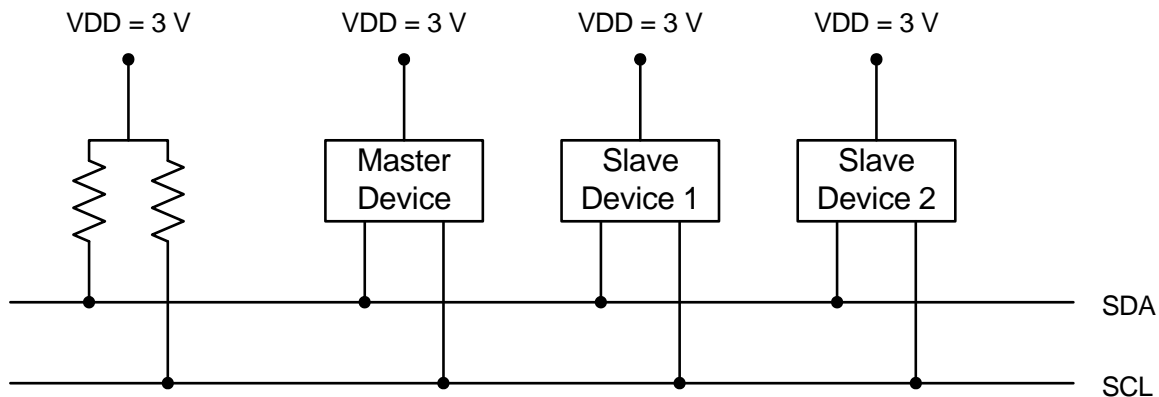


Figure 22.2. Typical SMBus Configuration

## SFR Definition 22.1. SMB0CF: SMBus Clock/Configuration

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	ENSMB	INH	BUSY	EXTHOLD	SMBTOE	SMBFTE	SMBCS[1:0]	
<b>Type</b>	R/W	R/W	R	R/W	R/W	R/W	R/W	
<b>Reset</b>	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC1

Bit	Name	Function
7	ENSMB	<p><b>SMBus Enable.</b></p> <p>This bit enables the SMBus interface when set to 1. When enabled, the interface constantly monitors the SDA and SCL pins.</p>
6	INH	<p><b>SMBus Slave Inhibit.</b></p> <p>When this bit is set to logic 1, the SMBus does not generate an interrupt when slave events occur. This effectively removes the SMBus slave from the bus. Master Mode interrupts are not affected.</p>
5	BUSY	<p><b>SMBus Busy Indicator.</b></p> <p>This bit is set to logic 1 by hardware when a transfer is in progress. It is cleared to logic 0 when a STOP or free-timeout is sensed.</p>
4	EXTHOLD	<p><b>SMBus Setup and Hold Time Extension Enable.</b></p> <p>This bit controls the SDA setup and hold times according to Table 22.2.                      0: SDA Extended Setup and Hold Times disabled.                      1: SDA Extended Setup and Hold Times enabled.</p>
3	SMBTOE	<p><b>SMBus SCL Timeout Detection Enable.</b></p> <p>This bit enables SCL low timeout detection. If set to logic 1, the SMBus forces Timer 3 to reload while SCL is high and allows Timer 3 to count when SCL goes low. If Timer 3 is configured to Split Mode, only the High Byte of the timer is held in reload while SCL is high. Timer 3 should be programmed to generate interrupts at 25 ms, and the Timer 3 interrupt service routine should reset SMBus communication.</p>
2	SMBFTE	<p><b>SMBus Free Timeout Detection Enable.</b></p> <p>When this bit is set to logic 1, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods.</p>
1:0	SMBCS[1:0]	<p><b>SMBus Clock Source Selection.</b></p> <p>These two bits select the SMBus clock source, which is used to generate the SMBus bit rate. The selected device should be configured according to Equation 22.1.</p> <p>00: Timer 0 Overflow                      01: Timer 1 Overflow                      10: Timer 2 High Byte Overflow                      11: Timer 2 Low Byte Overflow</p>

# C8051F99x-C8051F98x

## 23.2. Operational Modes

UART0 provides standard asynchronous, full duplex communication. The UART mode (8-bit or 9-bit) is selected by the S0MODE bit (SCON0.7). Typical UART connection options are shown below.

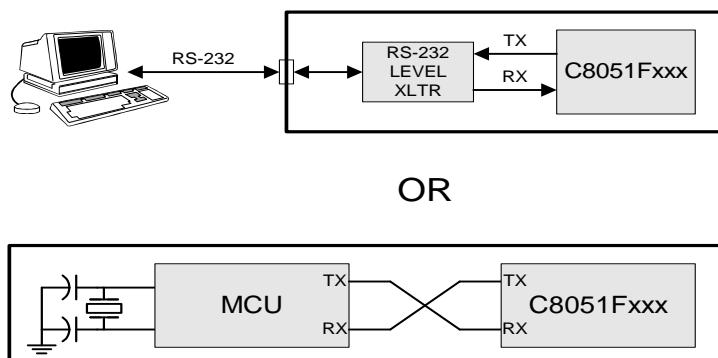


Figure 23.3. UART Interconnect Diagram

### 23.2.1. 8-Bit UART

8-Bit UART mode uses a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when software writes a data byte to the SBUF0 register. The T10 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if MCE0 is logic 1, the stop bit must be logic 1. In the event of a receive data overrun, the first received 8 bits are latched into the SBUF0 receive register and the following overrun data bits are lost.

If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either T10 or RI0 is set.

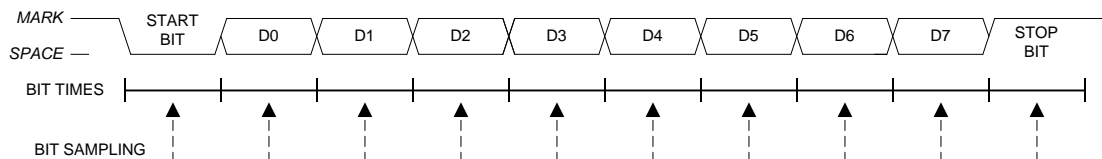


Figure 23.4. 8-Bit UART Timing Diagram