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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I <sup>2</sup> C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/c8051f988-c-gm">https://www.e-xfl.com/product-detail/silicon-labs/c8051f988-c-gm</a>

## 1.2. Port Input/Output

Digital and analog resources are available through 16 or 17 I/O pins. Port pins are organized as three byte-wide ports. Port pins P0.0–P1.7 can be defined as digital or analog I/O. Digital I/O pins can be assigned to one of the internal digital resources or used as general purpose I/O (GPIO). Analog I/O pins are used by the internal analog resources. P2.7 can be used as GPIO and is shared with the C2 Interface Data signal (C2D). See Section “27. C2 Interface” on page 319 for more details.

The designer has complete control over which digital and analog functions are assigned to individual Port pins, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. See Section “21.3. Priority Crossbar Decoder” on page 219 for more information on the Crossbar.

All Port I/Os can tolerate voltages up to the supply rail when used as digital inputs or open-drain outputs. For Port I/Os configured as push-pull outputs, current is sourced from the VDD supply. Port I/Os used for analog functions can operate up to the VDD supply voltage. See Section “21.1. Port I/O Modes of Operation” on page 216 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications.

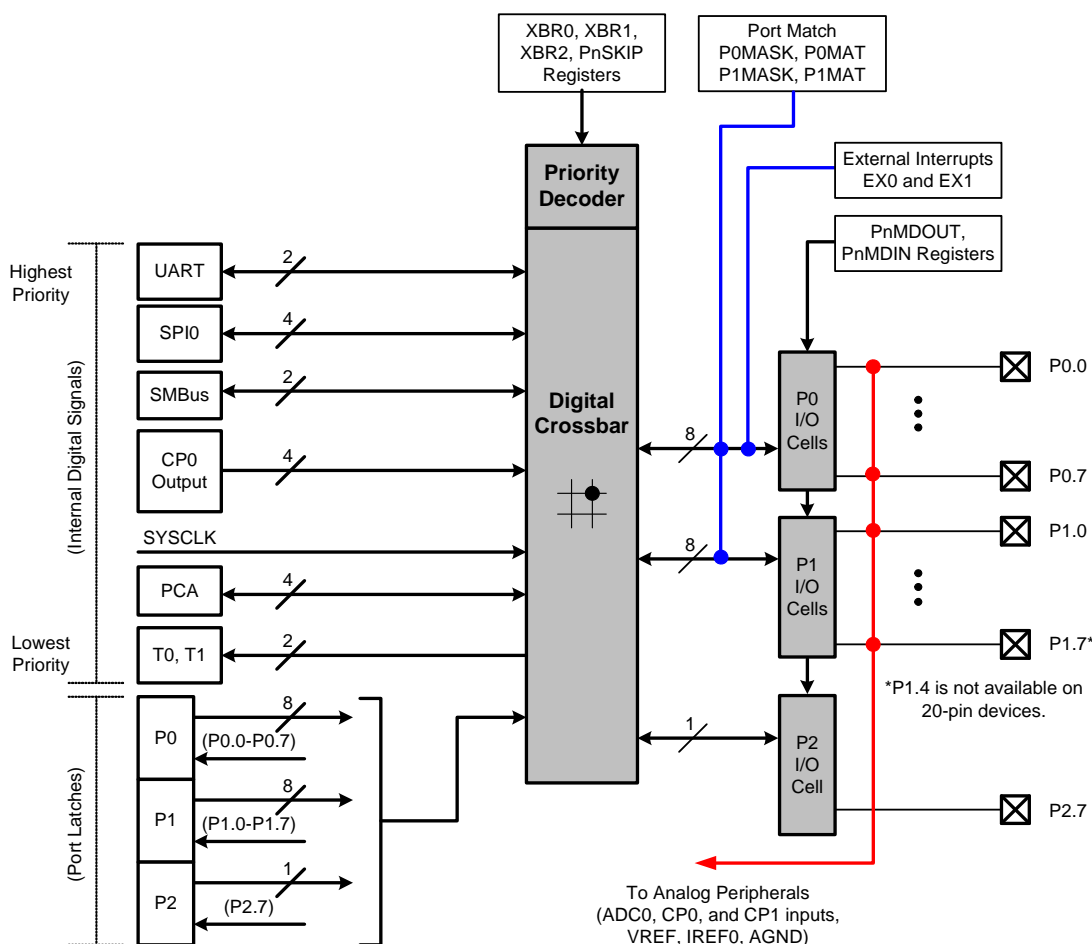


Figure 1.14. Port I/O Functional Block Diagram

**Table 4.16. Capacitive Sense Electrical Characteristics**

$V_{DD} = 1.8$  to  $3.6$  V;  $T_A = -40$  to  $+85$  °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Single Conversion Time <sup>1</sup>	12-bit Mode	20	25	40	μs
	13-bit Mode (default)	21	27	42.5	
	14-bit Mode	23	29	45	
	16-bit Mode	26	33	50	
Number of Channels	24-pin Packages	17			Channels
	20-pin Packages	16			
Capacitance per Code	Default Configuration	—	1	—	fF
Maximum External Capacitive Load	CS0CG = 111b (Default)	—	45	—	pF
	CS0CG = 000b	—	500	—	pF
Maximum External Series Impedance	CS0CG = 111b (Default)	—	50	—	kΩ
Power Supply Current	CS module bias current, 25 °C	—	50	60	μA
	CS module alone, maximum code output, 25 °C	—	90	125	μA
	Wake-on-CS threshold (suspend mode with regulator and CS module on) <sup>3</sup>	—	130	180	μA
<b>Notes:</b>					
1. Conversion time is specified with the default configuration.					
2. RMS Noise is equivalent to one standard deviation. Peak-to-peak noise encompasses ±3.3 standard deviations. The RMS noise value is specified with the default configuration.					
3. Includes only current from regulator, CS module, and MCU in suspend mode.					

## SFR Definition 5.6. ADC0H: ADC0 Data Word High Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0[15:8]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xBE

Bit	Name	Description	Read	Write
7:0	ADC0[15:8]	<b>ADC0 Data Word High Byte.</b>	Most Significant Byte of the 16-bit ADC0 Accumulator formatted according to the settings in AD0SJST[2:0].	Set the most significant byte of the 16-bit ADC0 Accumulator to the value written.
<b>Note:</b> If Accumulator shifting is enabled, the most significant bits of the value read will be zeros. This register should not be written when the SYNC bit is set to 1.				

## SFR Definition 5.7. ADC0L: ADC0 Data Word Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xBD;

Bit	Name	Description	Read	Write
7:0	ADC0[7:0]	<b>ADC0 Data Word Low Byte.</b>	Least Significant Byte of the 16-bit ADC0 Accumulator formatted according to the settings in AD0SJST[2:0].	Set the least significant byte of the 16-bit ADC0 Accumulator to the value written.
<b>Note:</b> If Accumulator shifting is enabled, the most significant bits of the value read will be the least significant bits of the accumulator high byte. This register should not be written when the SYNC bit is set to 1.				

## 8.11. CS0 Conversion Accumulator

CS0 can be configured to accumulate multiple conversions on an input channel. The number of samples to be accumulated is configured using the CS0ACU2:0 bits (CS0CF2:0). The accumulator can accumulate 1, 4, 8, 16, 32, or 64 samples. After the defined number of samples have been accumulated, the result is divided by either 1, 4, 8, 16, 32, or 64 (depending on the CS0ACU[2:0] setting) and copied to the CS0DH:CS0DL SFRs.

**Table 8.1. Operation with Auto-scan and Accumulate**

Auto-Scan Enabled	Accumulator Enabled	CS0 Conversion Complete Interrupt Behavior	CS0 Greater Than Interrupt Behavior	CS0MX Behavior
N	N	CS0INT Interrupt serviced after 1 conversion completes	Interrupt serviced after 1 conversion completes if value in CS0DH:CS0DL is greater than CS0THH:CS0THL	CS0MX unchanged.
N	Y	CS0INT Interrupt serviced after <i>M</i> conversions complete	Interrupt serviced after <i>M</i> conversions complete if value in CS0DH:CS0DL (post accumulate and divide) is greater than CS0THH:CS0THL	CS0MX unchanged.
Y	N	CS0INT Interrupt serviced after 1 conversion completes	Interrupt serviced after conversion completes if value in CS0DH:CS0DL is greater than CS0THH:CS0THL; Auto-Scan stopped	If greater-than comparator detects conversion value is greater than CS0THH:CS0THL, CS0MX is left unchanged; otherwise, CS0MX updates to the next channel (CS0MX + 1) and wraps back to CS0SS after passing CS0SE.
Y	Y	CS0INT Interrupt serviced after <i>M</i> conversions complete	Interrupt serviced after <i>M</i> conversions complete if value in CS0DH:CS0DL (post accumulate and divide) is greater than CS0THH:CS0THL; Auto-Scan stopped	If greater-than comparator detects conversion value is greater than CS0THH:CS0THL, CS0MX is left unchanged; otherwise, CS0MX updates to the next channel (CS0MX + 1) and wraps back to CS0SS after passing CS0SE.
<b>Note:</b> M = Accumulator setting (1x, 4x, 8x, 16x, 32x, 64x).				

## SFR Definition 8.3. CS0DH: Capacitive Sense Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	CS0DH[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xEE

Bit	Name	Description
7:0	CS0DH	<b>CS0 Data High Byte.</b> Stores the high byte of the last completed 16-bit Capacitive Sense conversion.

## SFR Definition 8.4. CS0DL: Capacitive Sense Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	CS0DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xED

Bit	Name	Description
7:0	CS0DL	<b>CS0 Data Low Byte.</b> Stores the low byte of the last completed 16-bit Capacitive Sense conversion.

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

## 9.2. Programming and Debugging Support

In-system programming of the Flash program memory and communication with on-chip debug support logic is accomplished via the Silicon Labs 2-Wire Development Interface (C2).

The on-chip debug support logic facilitates full speed in-circuit debugging, allowing the setting of hardware breakpoints, starting, stopping and single stepping through program execution (including interrupt service routines), examination of the program's call stack, and reading/writing the contents of registers and memory. This method of on-chip debugging is completely non-intrusive, requiring no RAM, Stack, timers, or other on-chip resources. C2 details can be found in Section "27. C2 Interface" on page 319.

The CIP-51 is supported by development tools from Silicon Labs and third party vendors. Silicon Labs provides an integrated development environment (IDE) including editor, debugger and programmer. The IDE's debugger and programmer interface to the CIP-51 via the C2 interface to provide fast and efficient in-system device programming and debugging. Third party macro assemblers and C compilers are also available.

## 9.3. Instruction Set

The instruction set of the CIP-51 System Controller is fully compatible with the standard MCS-51™ instruction set. Standard 8051 development tools can be used to develop software for the CIP-51. All CIP-51 instructions are the binary and functional equivalent of their MCS-51™ counterparts, including opcodes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051.

### 9.3.1. Instruction and CPU Timing

In many 8051 implementations, a distinction is made between machine cycles and clock cycles, with machine cycles varying from 2 to 12 clock cycles in length. However, the CIP-51 implementation is based solely on clock cycle timing. All instruction timings are specified in terms of clock cycles.

Due to the pipelined architecture of the CIP-51, most instructions execute in the same number of clock cycles as there are program bytes in the instruction. Conditional branch instructions take one less clock cycle to complete when the branch is not taken as opposed to when the branch is taken. Table 9.1 is the CIP-51 Instruction Set Summary, which includes the mnemonic, number of bytes, and number of clock cycles for each instruction.

# C8051F99x-C8051F98x

**Table 12.3. Special Function Registers (Continued)**

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page
P1SKIP	0xD5	0x0	Port 1 Skip	231
P2	0xA0	All	Port 2 Latch	233
P2DRV	0x9D	0xF	Port 2 Drive Strength	234
P2MDOUT	0xA6	0x0	Port 2 Output Mode Configuration	234
PCA0CN	0xD8	0x0	PCA0 Control	313
PCA0CPH0	0xFC	0x0	PCA0 Capture 0 High	318
PCA0CPH1	0xEA	0x0	PCA0 Capture 1 High	318
PCA0CPH2	0xEC	0x0	PCA0 Capture 2 High	318
PCA0CPL0	0xFB	0x0	PCA0 Capture 0 Low	318
PCA0CPL1	0xE9	0x0	PCA0 Capture 1 Low	318
PCA0CPL2	0xEB	0x0	PCA0 Capture 2 Low	318
PCA0CPM0	0xDA	0x0	PCA0 Module 0 Mode Register	316
PCA0CPM1	0xDB	0x0	PCA0 Module 1 Mode Register	316
PCA0CPM2	0xDC	0x0	PCA0 Module 2 Mode Register	316
PCA0H	0xFA	0x0	PCA0 Counter High	317
PCA0L	0xF9	0x0	PCA0 Counter Low	317
PCA0MD	0xD9	0x0	PCA0 Mode	314
PCA0PWM	0xDF	0x0	PCA0 PWM Configuration	315
PCON	0x87	All	Power Control	171
PMU0CF	0xB5	0x0	PMU0 Configuration	168
PMU0FL	0xCE	0x0	PMU0 Flag Register	169
PMU0MD	0xB5	0xF	PMU0 Mode	170
PSCTL	0x8F	All	Program Store R/W Control	159
PSW	0xD0	All	Program Status Word	127
REF0CN	0xD1	0x0	Voltage Reference Control	90
REG0CN	0xC9	0x0	Voltage Regulator (REG0) Control	180
REVID	0xE2	0xF	Revision ID	155
RSTSRC	0xEF	0x0	Reset Source Configuration/Status	187
RTC0ADR	0xAC	0x0	RTC0 Address	202
RTC0DAT	0xAD	0x0	RTC0 Data	202
RTC0KEY	0xAE	0x0	RTC0 Key	201
SBUF0	0x99	0x0	UART0 Data Buffer	263
SCON0	0x98	0x0	UART0 Control	262
SFRPAGE	0xA7	All	SFR Page	134
SMB0ADM	0xF5	0x0	SMBus Slave Address Mask	247
SMB0ADR	0xF4	0x0	SMBus Slave Address	247
SMB0CF	0xC1	0x0	SMBus0 Configuration	242
SMB0CN	0xC0	0x0	SMBus0 Control	244
SMB0DAT	0xC2	0x0	SMBus0 Data	248
SP	0x81	All	Stack Pointer	126
SPI0CFG	0xA1	0x0	SPI0 Configuration	272
SPI0CKR	0xA2	0x0	SPI0 Clock Rate Control	274
SPI0CN	0xF8	0x0	SPI0 Control	273
SPI0DAT	0xA3	0x0	SPI0 Data	274

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## SFR Definition 14.2. REVID: Revision Identification

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Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xE2

Bit	Name	Function
7:0	REVID[7:0]	<b>Revision Identification.</b> These bits contain a value that can be decoded to determine the silicon revision. For example, 0x00 for Rev A, 0x01 for Rev B, 0x02 for Rev C, etc.

# C8051F99x-C8051F98x

## SFR Definition 15.1. PMU0CF: Power Management Unit Configuration<sup>1,2,3</sup>

Bit	7	6	5	4	3	2	1	0
Name	SLEEP	SUSPEND	CLEAR	RSTWK	RTCFWK	RTCAWK	PMATWK	CPT0WK
Type	W	W	W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	Varies	Varies	Varies	Varies	Varies

SFR Page = 0x0; SFR Address = 0xB5

Bit	Name	Description	Write	Read
7	SLEEP	<b>Sleep Mode Select</b>	Writing 1 places the device in Sleep Mode.	N/A
6	SUSPEND	<b>Suspend Mode Select</b>	Writing 1 places the device in Suspend Mode.	N/A
5	CLEAR	<b>Wake-up Flag Clear</b>	Writing 1 clears all wake-up flags.	N/A
4	RSTWK	<b>Reset Pin Wake-up Flag</b>	N/A	Set to 1 if a glitch has been detected on $\overline{RST}$ .
3	RTCFWK	<b>SmaRTClock Oscillator Fail Wake-up Source Enable and Flag</b>	0: Disable wake-up on SmaRTClock Osc. Fail. 1: Enable wake-up on SmaRTClock Osc. Fail.	Set to 1 if the SmaRTClock Oscillator has failed.
2	RTCAWK	<b>SmaRTClock Alarm Wake-up Source Enable and Flag</b>	0: Disable wake-up on SmaRTClock Alarm. 1: Enable wake-up on SmaRTClock Alarm.	Set to 1 if a SmaRTClock Alarm has occurred.
1	PMATWK	<b>Port Match Wake-up Source Enable and Flag</b>	0: Disable wake-up on Port Match Event. 1: Enable wake-up on Port Match Event.	Set to 1 if a Port Match Event has occurred.
0	CPT0WK	<b>Comparator0 Wake-up Source Enable and Flag</b>	0: Disable wake-up on Comparator0 rising edge. 1: Enable wake-up on Comparator0 rising edge.	Set to 1 if Comparator0 rising edge caused the last wake-up.

### Notes:

1. Read-modify-write operations (ORL, ANL, etc.) should not be used on this register. Wake-up sources must be re-enabled each time the SLEEP or SUSPEND bits are written to 1.
2. The Low Power Internal Oscillator cannot be disabled and the MCU cannot be placed in Suspend or Sleep Mode if any wake-up flags are set to 1. Software should clear all wake-up sources after each reset and after each wake-up from Suspend or Sleep Modes.
3. PMU0 requires two system clocks to update the wake-up source flags after waking from Suspend mode. The wake-up source flags will read '0' during the first two system clocks following the wake from Suspend mode.

## SFR Definition 15.4. PCON: Power Management Control Register

Bit	7	6	5	4	3	2	1	0
Name	GF[5:0]						STOP	IDLE
Type	R/W						W	W
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0x87

Bit	Name	Description	Write	Read
7:2	GF[5:0]	<b>General Purpose Flags</b>	Sets the logic value.	Returns the logic value.
1	STOP	<b>Stop Mode Select</b>	Writing 1 places the device in Stop Mode.	N/A
0	IDLE	<b>Idle Mode Select</b>	Writing 1 places the device in Idle Mode.	N/A

## 15.8. Power Management Specifications

See Table 4.5 on page 58 for detailed Power Management Specifications.

## 16. Cyclic Redundancy Check Unit (CRC0)

C8051F99x-C8051F98x devices include a cyclic redundancy check unit (CRC0) that can perform a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data written to the CRC0IN register. CRC0 posts the 16-bit result to an internal register. The internal result register may be accessed indirectly using the CRC0PNT bits and CRC0DAT register, as shown in Figure 16.1. CRC0 also has a bit reverse register for quick data manipulation.

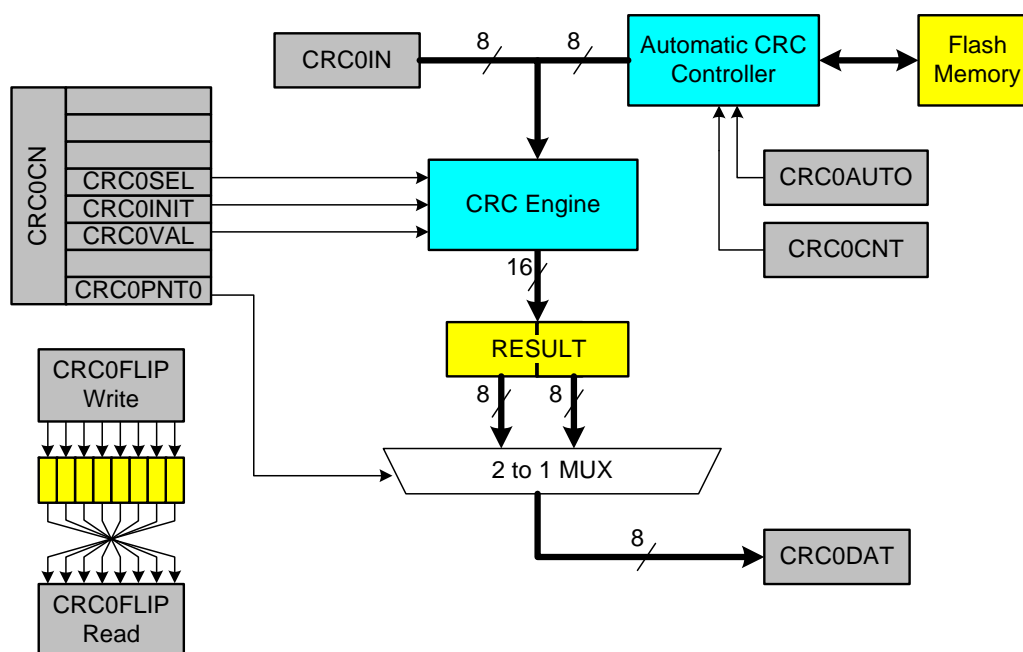


Figure 16.1. CRC0 Block Diagram

### 16.1. CRC Algorithm

The C8051F99x-C8051F98x CRC unit generates a CRC result equivalent to the following algorithm:

1. XOR the input with the most-significant bits of the current CRC result. If this is the first iteration of the CRC unit, the current CRC result will be the set initial value (0x0000 or 0xFFFF).
- 2a. If the MSB of the CRC result is set, shift the CRC result and XOR the result with the selected polynomial.
- 2b. If the MSB of the CRC result is not set, shift the CRC result.

Repeat Steps 2a/2b for the number of input bits (8). The algorithm is also described in the following example.

## 19.4. Special Function Registers for Selecting and Configuring the System Clock

The clocking sources on C8051F99x-C8051F98x devices are enabled and configured using the OSCICN, OSCICL, OSCXCN and the SmaRTClock internal registers. See Section “20. SmaRTClock (Real Time Clock)” on page 197 for SmaRTClock register descriptions. The system clock source for the MCU can be selected using the CLKSEL register. To minimize active mode current, the oneshot timer which sets Flash read time should be bypassed when the system clock is greater than 10 MHz. See the FLSCL register description for details.

The clock selected as the system clock can be divided by 1, 2, 4, 8, 16, 32, 64, or 128. When switching between two clock divide values, the transition may take up to 128 cycles of the undivided clock source. The CLKRDY flag can be polled to determine when the new clock divide value has been applied. The clock divider must be set to "divide by 1" when entering Suspend or Sleep Mode.

The system clock source may also be switched on-the-fly. The switchover takes effect after one clock period of the slower oscillator.

### SFR Definition 19.1. CLKSEL: Clock Select

Bit	7	6	5	4	3	2	1	0
Name	CLKRDY	CLKDIV[2:0]				CLKSEL[2:0]		
Type	R	R/W			R/W	R/W		
Reset	1	0	0	0	0	0	1	0

SFR Page = All; SFR Address = 0xA9

Bit	Name	Function
7	CLKRDY	<b>System Clock Divider Clock Ready Flag.</b> 0: The selected clock divide setting has not been applied to the system clock. 1: The selected clock divide setting has been applied to the system clock.
6:4	CLKDIV[2:0]	<b>System Clock Divider Bits.</b> Selects the clock division to be applied to the undivided system clock source. 000: System clock is divided by 1. 001: System clock is divided by 2. 010: System clock is divided by 4. 011: System clock is divided by 8. 100: System clock is divided by 16. 101: System clock is divided by 32. 110: System clock is divided by 64. 111: System clock is divided by 128.
3	Unused	Read = 0b. Must Write 0b.
2:0	CLKSEL[2:0]	<b>System Clock Select.</b> Selects the oscillator to be used as the undivided system clock source. 000: Precision Internal Oscillator. 001: External Oscillator. 010: Low Power Oscillator divided by 8. 011: SmaRTClock Oscillator. 100: Low Power Oscillator. All other values reserved.

## 20.1.2. Using RTC0ADR and RTC0DAT to Access SmaRTClock Internal Registers

The SmaRTClock internal registers can be read and written using RTC0ADR and RTC0DAT. The RTC0ADR register selects the SmaRTClock internal register that will be targeted by subsequent reads or writes. Recommended instruction timing is provided in this section. If the recommended instruction timing is not followed, then BUSY (RTC0ADR.7) should be checked prior to each read or write operation to make sure the SmaRTClock Interface is not busy performing the previous read or write operation. A SmaRTClock Write operation is initiated by writing to the RTC0DAT register. Below is an example of writing to a SmaRTClock internal register.

1. Poll BUSY (RTC0ADR.7) until it returns 0 or follow recommended instruction timing.
2. Write 0x05 to RTC0ADR. This selects the internal RTC0CN register at SmaRTClock Address 0x05.
3. Write 0x00 to RTC0DAT. This operation writes 0x00 to the internal RTC0CN register.

A SmaRTClock Read operation is initiated by setting the SmaRTClock Interface Busy bit. This transfers the contents of the internal register selected by RTC0ADR to RTC0DAT. The transferred data will remain in RTC0DAT until the next read or write operation. Below is an example of reading a SmaRTClock internal register.

1. Poll BUSY (RTC0ADR.7) until it returns 0 or follow recommended instruction timing.
2. Write 0x05 to RTC0ADR. This selects the internal RTC0CN register at SmaRTClock Address 0x05.
3. Write 1 to BUSY. This initiates the transfer of data from RTC0CN to RTC0DAT.
4. Poll BUSY (RTC0ADR.7) until it returns 0 or follow recommended instruction timing.
5. Read data from RTC0DAT. This data is a copy of the RTC0CN register.

**Note:** The RTC0ADR and RTC0DAT registers will retain their state upon a device reset.

## 20.1.3. RTC0ADR Short Strobe Feature

Reads and writes to indirect SmaRTClock registers normally take 7 system clock cycles. To minimize the indirect register access time, the Short Strobe feature decreases the read and write access time to 6 system clocks. The Short Strobe feature is automatically enabled on reset and can be manually enabled/disabled using the SHORT (RTC0ADR.4) control bit.

Recommended Instruction Timing for a single register read with short strobe enabled:

```
mov RTC0ADR, #095h
nop
nop
nop
nop
mov A, RTC0DAT
```

Recommended Instruction Timing for a single register write with short strobe enabled:

```
mov RTC0ADR, #095h
mov RTC0DAT, #000h
nop
```

## 20.1.4. SmaRTClock Interface Autoread Feature

When Autoread is enabled, each read from RTC0DAT initiates the next indirect read operation on the SmaRTClock internal register selected by RTC0ADR. Software should set the BUSY bit once at the beginning of each series of consecutive reads. Software should follow recommended instruction timing or check if the SmaRTClock Interface is busy prior to reading RTC0DAT. Autoread is enabled by setting AUTORD (RTC0ADR.6) to logic 1.

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## 20.2. SmarTClock Clocking Sources

The SmarTClock peripheral is clocked from its own timebase, independent of the system clock. The SmarTClock timebase can be derived from an external CMOS clock, the internal LFO, or the SmarT-Clock oscillator circuit, which has two modes of operation: Crystal Mode, and Self-Oscillate Mode. The oscillation frequency is 32.768 kHz in Crystal Mode and can be programmed in the range of 10 kHz to 40 kHz in Self-Oscillate Mode. The internal LFO frequency is 16.4 kHz  $\pm$ 20%. The frequency of the SmarTClock oscillator can be measured with respect to another oscillator using an on-chip timer. See Section “25. Timers” on page 278 for more information on how this can be accomplished.

**Note:** The SmarTClock timebase can be selected as the system clock and routed to a port pin. See Section “19. Clocking Sources” on page 188 for information on selecting the system clock source and Section “21. Port Input/Output” on page 215 for information on how to route the system clock to a port pin. The SmarTClock timebase can also be routed to a port pin while the device is in its ultra low power sleep mode. See the PMU0MD register description for details.

### 20.2.1. Using the SmarTClock Oscillator with a Crystal or External CMOS Clock

When using Crystal Mode, a 32.768 kHz crystal should be connected between XTAL3 and XTAL4. No other external components are required. The following steps show how to start the SmarTClock crystal oscillator in software:

1. Configure the XTAL3 and XTAL4 pins for Analog I/O.
2. Set SmarTClock to Crystal Mode (XMODE = 1).
3. Disable Automatic Gain Control (AGCEN) and enable Bias Doubling (BIASX2) for fast crystal startup.
4. Set the desired loading capacitance (RTC0XCF).
5. Enable power to the SmarTClock oscillator circuit (RTC0EN = 1).
6. Wait 20 ms.
7. Poll the SmarTClock Clock Valid Bit (CLKVLD) until the crystal oscillator stabilizes.
8. Poll the SmarTClock Load Capacitance Ready Bit (LOADRDY) until the load capacitance reaches its programmed value.
9. Enable Automatic Gain Control (AGCEN) and disable Bias Doubling (BIASX2) for maximum power savings.
10. Enable the SmarTClock missing clock detector.
11. Wait 2 ms.
12. Clear the PMU0CF wake-up source flags.

In Crystal Mode, the SmarTClock oscillator may be driven by an external CMOS clock. The CMOS clock should be applied to XTAL3. XTAL4 should be left floating. In this mode, the external CMOS clock is ac coupled into the SmarTClock and should have a minimum voltage swing of 400 mV. The CMOS clock signal voltage should not exceed VDD or drop below GND. Bias levels closer to VDD will result in lower I/O power consumption because the XTAL3 pin has a built-in weak pull-up. The SmarTClock oscillator should be configured to its lowest bias setting with AGC disabled. The CLKVLD bit is indeterminate when using a CMOS clock, however, the OSCFAIL bit may be checked 2 ms after SmarTClock oscillator is powered on to ensure that there is a valid clock on XTAL3.

## SFR Definition 21.6. P1MASK: Port1 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P1MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0xBF

Bit	Name	Function
7:0	P1MASK[7:0]	<b>Port 1 Mask Value.</b> Selects P1 pins to be compared to the corresponding bits in P1MAT. 0: P1.n pin logic value is ignored and cannot cause a Port Mismatch event. 1: P1.n pin logic value is compared to P1MAT.n.

## SFR Definition 21.7. P1MAT: Port1 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P1MAT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = 0x0; SFR Address = 0xCF

Bit	Name	Function
7:0	P1MAT[7:0]	<b>Port 1 Match Value.</b> Match comparison value used on Port 1 for bits in P1MASK which are set to 1. 0: P1.n pin logic value is compared with logic LOW. 1: P1.n pin logic value is compared with logic HIGH.

# C8051F99x-C8051F98x

## SFR Definition 21.10. P0MDIN: Port0 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page= 0x0; SFR Address = 0xF1

Bit	Name	Function
7:0	P0MDIN[7:0]	<b>Analog Configuration Bits for P0.7–P0.0 (respectively).</b> Port pins configured for analog mode have their weak pullup, and digital receiver disabled. The digital driver is not explicitly disabled. 0: Corresponding P0.n pin is configured for analog mode. 1: Corresponding P0.n pin is not configured for analog mode.

## SFR Definition 21.11. P0MDOUT: Port0 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xA4

Bit	Name	Function
7:0	P0MDOUT[7:0]	<b>Output Configuration Bits for P0.7–P0.0 (respectively).</b> These bits control the digital driver even when the corresponding bit in register P0MDIN is logic 0. 0: Corresponding P0.n Output is open-drain. 1: Corresponding P0.n Output is push-pull.

**Table 23.1. Timer Settings for Standard Baud Rates  
Using The Internal 24.5 MHz Oscillator**

Frequency: 24.5 MHz							
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select) <sup>1</sup>	T1M <sup>1</sup>	Timer 1 Reload Value (hex)
SYSCLK from Internal Osc.	230400	–0.32%	106	SYSCLK	XX <sup>2</sup>	1	0xCB
	115200	–0.32%	212	SYSCLK	XX	1	0x96
	57600	0.15%	426	SYSCLK	XX	1	0x2B
	28800	–0.32%	848	SYSCLK/4	01	0	0x96
	14400	0.15%	1704	SYSCLK/12	00	0	0xB9
	9600	–0.32%	2544	SYSCLK/12	00	0	0x96
	2400	–0.32%	10176	SYSCLK/48	10	0	0x96
	1200	0.15%	20448	SYSCLK/48	10	0	0x2B
<b>Notes:</b> <ol style="list-style-type: none"> <li>1. SCA1–SCA0 and T1M bit definitions can be found in Section 25.1.</li> <li>2. X = Don't care.</li> </ol>							

**Table 23.2. Timer Settings for Standard Baud Rates  
Using an External 22.1184 MHz Oscillator**

Frequency: 22.1184 MHz							
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select) <sup>1</sup>	T1M <sup>1</sup>	Timer 1 Reload Value (hex)
SYSCLK from External Osc.	230400	0.00%	96	SYSCLK	XX <sup>2</sup>	1	0xD0
	115200	0.00%	192	SYSCLK	XX	1	0xA0
	57600	0.00%	384	SYSCLK	XX	1	0x40
	28800	0.00%	768	SYSCLK / 12	00	0	0xE0
	14400	0.00%	1536	SYSCLK / 12	00	0	0xC0
	9600	0.00%	2304	SYSCLK / 12	00	0	0xA0
	2400	0.00%	9216	SYSCLK / 48	10	0	0xA0
	1200	0.00%	18432	SYSCLK / 48	10	0	0x40
SYSCLK from Internal Osc.	230400	0.00%	96	EXTCLK / 8	11	0	0xFA
	115200	0.00%	192	EXTCLK / 8	11	0	0xF4
	57600	0.00%	384	EXTCLK / 8	11	0	0xE8
	28800	0.00%	768	EXTCLK / 8	11	0	0xD0
	14400	0.00%	1536	EXTCLK / 8	11	0	0xA0
	9600	0.00%	2304	EXTCLK / 8	11	0	0x70
<b>Notes:</b> <ol style="list-style-type: none"> <li>1. SCA1–SCA0 and T1M bit definitions can be found in Section 25.1.</li> <li>2. X = Don't care.</li> </ol>							

## 25.2.3. Comparator 0/SmaRTClock Capture Mode

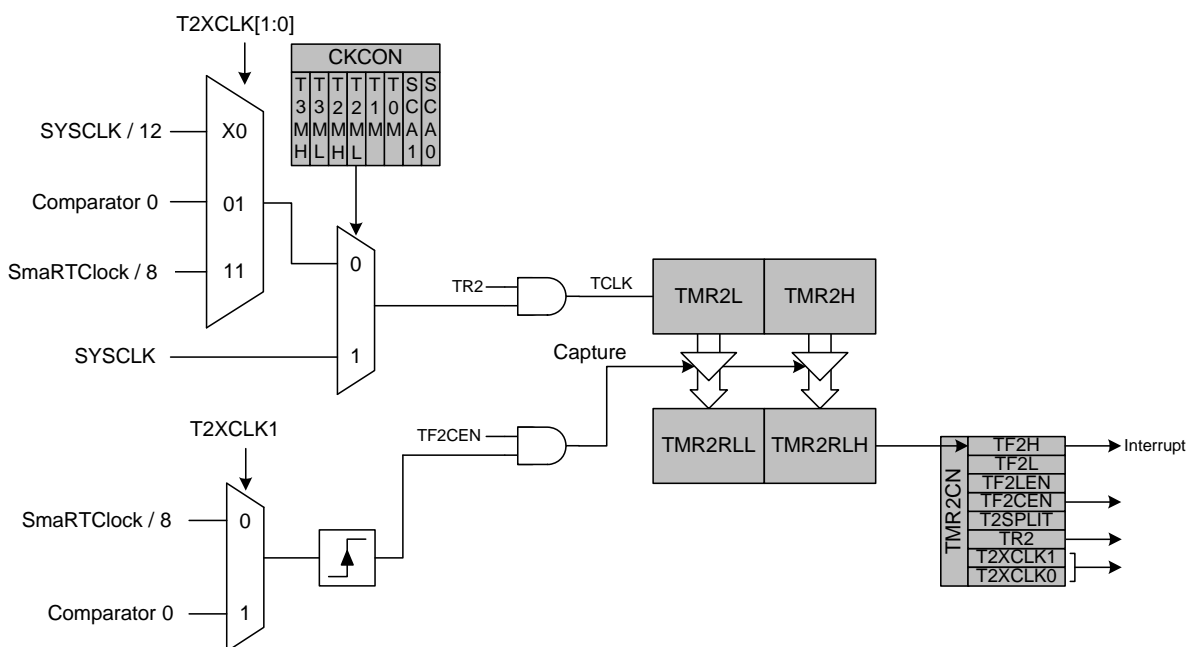
The Capture Mode in Timer 2 allows either Comparator 0 or the SmaRTClock period to be measured against the system clock or the system clock divided by 12. Comparator 0 and the SmaRTClock period can also be compared against each other. Timer 2 Capture Mode is enabled by setting TF2CEN to 1. Timer 2 should be in 16-bit auto-reload mode when using Capture Mode.

When Capture Mode is enabled, a capture event will be generated either every Comparator 0 rising edge or every 8 SmaRTClock clock cycles, depending on the T2XCLK1 setting. When the capture event occurs, the contents of Timer 2 (TMR2H:TMR2L) are loaded into the Timer 2 reload registers (TMR2RLH:TMR2RLL) and the TF2H flag is set (triggering an interrupt if Timer 2 interrupts are enabled). By recording the difference between two successive timer capture values, the Comparator 0 or SmaRT-Clock period can be determined with respect to the Timer 2 clock. The Timer 2 clock should be much faster than the capture clock to achieve an accurate reading.

For example, if T2ML = 1b, T2XCLK1 = 0b, and TF2CEN = 1b, Timer 2 will clock every SYSCLK and capture every SmaRTClock clock divided by 8. If the SYSCLK is 24.5 MHz and the difference between two successive captures is 5984, then the SmaRTClock clock is as follows:

$$24.5 \text{ MHz} / (5984 / 8) = 0.032754 \text{ MHz or } 32.754 \text{ kHz.}$$

This mode allows software to determine the exact SmaRTClock frequency in self-oscillate mode and the time between consecutive Comparator 0 rising edges, which is useful for detecting changes in the capacitance of a Touch Sense Switch.



**Figure 25.6. Timer 2 Capture Mode Block Diagram**

**SFR Definition 25.8. TMR2CN: Timer 2 Control**

Bit	7	6	5	4	3	2	1	0
Name	TF2H	TF2L	TF2LEN	TF2CEN	T2SPLIT	TR2	T2XCLK[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC8; Bit-Addressable

Bit	Name	Function
7	TF2H	<b>Timer 2 High Byte Overflow Flag.</b> Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF2L	<b>Timer 2 Low Byte Overflow Flag.</b> Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. TF2L will be set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.
5	TF2LEN	<b>Timer 2 Low Byte Interrupt Enable.</b> When set to 1, this bit enables Timer 2 Low Byte interrupts. If Timer 2 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 2 overflows.
4	TF2CEN	<b>Timer 2 Capture Enable.</b> When set to 1, this bit enables Timer 2 Capture Mode.
3	T2SPLIT	<b>Timer 2 Split Mode Enable.</b> When set to 1, Timer 2 operates as two 8-bit timers with auto-reload. Otherwise, Timer 2 operates in 16-bit auto-reload mode.
2	TR2	<b>Timer 2 Run Control.</b> Timer 2 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in split mode.
1:0	T2XCLK[1:0]	<b>Timer 2 External Clock Select.</b> This bit selects the “external” and “capture trigger” clock sources for Timer 2. If Timer 2 is in 8-bit mode, this bit selects the “external” clock source for both timer bytes. Timer 2 Clock Select bits (T2MH and T2ML in register CKCON) may still be used to select between the “external” clock and the system clock for either timer. Note: External clock sources are synchronized with the system clock. 00: External Clock is SYSCLK/12. Capture trigger is SmarTClock/8. 01: External Clock is Comparator 0. Capture trigger is SmarTClock/8. 10: External Clock is SYSCLK/12. Capture trigger is Comparator 0. 11: External Clock is SmarTClock/8. Capture trigger is Comparator 0.

## SFR Definition 25.11. TMR2L: Timer 2 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xCC

Bit	Name	Function
7:0	TMR2L[7:0]	<b>Timer 2 Low Byte.</b> In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

## SFR Definition 25.12. TMR2H Timer 2 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xCD

Bit	Name	Function
7:0	TMR2H[7:0]	<b>Timer 2 High Byte.</b> In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8-bit mode, TMR2H contains the 8-bit high byte timer value.