E·XFL



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f988-c-gur

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 3.6. QSOP-24 Package Marking Diagram







Table 3.7. PCB Land Pattern

Dimension	MIN	MAX	
С	5.20 5.30		
E	0.635 BSC		
Х	0.30	0.40	
Y	1.50	1.60	

Notes:

General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be $60 \ \mu m$ minimum, all the way around the pad.

Stencil Design

- **1.** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 2. The stencil thickness should be 0.125 mm (5 mils).

3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

- 1. A No-Clean, Type-3 solder paste is recommended.
- 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



Table 4.2. Global Electrical Characteristics (Continued)

-40 to +85 °C, 25 MHz system clock unless otherwise specified. See "AN358: Optimizing Low Power Operation of the 'F9xx" for details on how to achieve the supply current specifications listed in this table.

Parameter	Conditions	Min	Тур	Max	Units
Digital Supply Current—CP	U Inactive (Idle Mode, not fetching instru	ictions	from Fl	ash)	
I _{DD} ^{4, 6}	V _{DD} = 1.8–3.6 V, F = 24.5 MHz (includes precision oscillator current)		1.8	3.0	mA
	V _{DD} = 1.8–3.6 V, F = 20 MHz (includes low power oscillator current)		1.4	_	mA
	V_{DD} = 1.8 V, F = 1 MHz V_{DD} = 3.6 V, F = 1 MHz (includes external oscillator/GPIO current)		145 180	_	μΑ μΑ
	V _{DD} = 1.8–3.6 V, F = 32.768 kHz (includes SmaRTClock oscillator current)		82	_	μA
I _{DD} Frequency Sensitivity ^{1,6}	V _{DD} = 1.8–3.6 V, T = 25 °C	—	67	—	µA/MHz
Digital Supply Current—Su	spend and Sleep Mode				
Digital Supply Current (Suspend Mode)	V _{DD} = 1.8–3.6 V		77		μA
Digital Supply Current (Sleep Mode, SmaRTClock running, 32.768 kHz crystal)	1.8 V, T = 25 °C 3.0 V, T = 25 °C 3.6 V, T = 25 °C 1.8 V, T = 85 °C 3.0 V, T = 85 °C 3.6 V, T = 85 °C		0.60 0.70 0.80 0.80 0.90 1.00		μA
	(includes SmaRTClock oscillator and V _{DD} Supply Monitor)				
Digital Supply Current (Sleep Mode, SmaRTClock running, internal LFO)	1.8 V, T = 25 °C 3.0 V, T = 25 °C 3.6 V, T = 25 °C 1.8 V, T = 85 °C 3.0 V, T = 85 °C 3.6 V, T = 85 °C 3.6 V, T = 85 °C (includes SmaRTClock oscillator and V_{DD} Supply Monitor)		0.30 0.40 0.50 0.50 0.70 0.80		μA
Digital Supply Current (Sleep Mode)	1.8 V, T = 25 °C 3.0 V, T = 25 °C 3.6 V, T = 25 °C 1.8 V, T = 85 °C 3.0 V, T = 85 °C 3.6 V, T = 85 °C (includes V _{DD} supply monitor)		0.05 0.07 0.08 0.20 0.24 0.28		μA
Digital Supply Current (Sleep Mode, VDD Supply Monitor Disabled)	1.8 V, T = 25 °C 3.0 V, T = 25 °C 3.6 V, T = 25 °C 1.8 V, T = 85 °C 3.0 V, T = 85 °C 3.6 V, T = 85 °C		0.005 0.01 0.02 0.15 0.19 0.23		μΑ





Figure 4.2. Idle Mode Current (External CMOS Clock)



5.2.3. Burst Mode

Burst Mode is a power saving feature that allows ADC0 to remain in a low power state between conversions. When Burst Mode is enabled, ADC0 wakes from a low power state, accumulates 1, 4, 8, 16, 32, or 64 using an internal Burst Mode clock (approximately 20 MHz), then re-enters a low power state. Since the Burst Mode clock is independent of the system clock, ADC0 can perform multiple conversions then enter a low power state within a single system clock cycle, even if the system clock is slow (e.g. 32.768 kHz), or suspended.

Burst Mode is enabled by setting BURSTEN to logic 1. When in Burst Mode, AD0EN controls the ADC0 idle power state (i.e. the state ADC0 enters when not tracking or performing conversions). If AD0EN is set to logic 0, ADC0 is powered down after each burst. If AD0EN is set to logic 1, ADC0 remains enabled after each burst. On each convert start signal, ADC0 is awakened from its Idle Power State. If AD0C0 is powered down, it will automatically power up and wait the programmable Power-Up Time controlled by the AD0PWR bits. Otherwise, ADC0 will start tracking and converting immediately. Figure 5.3 shows an example of Burst Mode Operation with a slow system clock and a repeat count of 4.

When Burst Mode is enabled, a single convert start will initiate a number of conversions equal to the repeat count. When Burst Mode is disabled, a convert start is required to initiate each conversion. In both modes, the ADC0 End of Conversion Interrupt Flag (AD0INT) will be set after "repeat count" conversions have been accumulated. Similarly, the Window Comparator will not compare the result to the greater-than and less-than registers until "repeat count" conversions have been accumulated.

In Burst Mode, tracking is determined by the settings in AD0PWR and AD0TK. The default settings for these registers will work in most applications without modification; however, settling time requirements may need adjustment in some applications. Refer to "5.2.4. Settling Time Requirements" on page 71 for more details.

Notes:

- Setting AD0TM to 1 will insert an additional 3 SAR clocks of tracking before each conversion, regardless of the settings of AD0PWR and AD0TK.
- When using Burst Mode, care must be taken to issue a convert start signal no faster than once every four SYSCLK periods. This includes external convert start signals.



T = Tracking set by AD0TK T3 = Tracking set by AD0TM (3 SAR clocks) C = Converting

Figure 5.3. Burst Mode Tracking Example with Repeat Count Set to 4



5.2.5. Gain Setting

The ADC has gain settings of 1x and 0.5x. In 1x mode, the full scale reading of the ADC is determined directly by V_{REF}. In 0.5x mode, the full-scale reading of the ADC occurs when the input voltage is V_{REF} x 2. The 0.5x gain setting can be useful to obtain a higher input Voltage range when using a small V_{REF} voltage, or to measure input voltages that are between V_{REF} and V_{DD}. Gain settings for the ADC are controlled by the AMP0GN bit in register ADC0CF.

5.3. 8-Bit Mode

Setting the ADC08BE bit in register ADC0CF to 1 will put the ADC in 8-bit mode. In 8-bit mode, only the 8 MSBs of data are converted, allowing the conversion to be completed in two fewer SAR clock cycles than a 10-bit conversion. This can result in an overall lower power consumption since the system can spend more time in a low power mode. The two LSBs of a conversion are always 00 in this mode, and the ADC0L register will always read back 0x00.

5.4. 12-Bit Mode (C8051F980/6 and C8051F990/6 devices only)

C8051F980/6 and C8051F990/6 devices have an enhanced SAR converter that provides 12-bit resolution while retaining the 10- and 8-bit operating modes of the other devices in the family. When configured for 12-bit conversions, the ADC performs four 10-bit conversions using four different reference voltages and combines the results into a single 12-bit value. Unlike simple averaging techniques, this method provides true 12-bit resolution of AC or DC input signals without depending on noise to provide dithering. The converter also employs a hardware Dynamic Element Matching algorithm that reconfigures the largest elements of the internal DAC for each of the four 10-bit conversions to cancel any matching errors, enabling the converter to achieve 12-bit linearity performance to go along with its 12-bit resolution. For best performance, the Low Power Oscillator should be selected as the system clock source while taking 12-bit ADC measurements.

The 12-bit mode is enabled by setting the AD012BE bit (ADC0AC.7) to logic 1 and configuring Burst Mode for four conversions as described in Section 5.2.3. The conversion can be initiated using any of the methods described in Section 5.2.1, and the 12-bit result will appear in the ADC0H and ADC0L registers. Since the 12-bit result is formed from a combination of four 10-bit results, the maximum output value is $4 \times (1023) = 4092$, rather than the max value of $(2^{12} - 1) = 4095$ that is produced by a traditional 12-bit converter. To further increase resolution, the burst mode repeat value may be configured to any multiple of four conversions. For example, if a repeat value of 16 is selected, the ADC0 output will be a 14-bit number (sum of four 12-bit numbers) with 13 effective bits of resolution.

5.5. Low Power Mode

The SAR converter provides a low power mode that allows a significant reduction in operating current when operating at low SAR clock frequencies. Low power mode is enabled by setting the AD0LPM bit (ADC0PWR.7) to 1. In general, low power mode is recommended when operating with SAR conversion clock frequency at 4 MHz or less. See the Electrical Characteristics chapter for details on power consumption and the maximum clock frequencies allowed in each mode. Setting the Low Power Mode bit reduces the bias currents in both the SAR converter and in the High-Speed Voltage Reference.



SFR Definition 13.7. IT01CF: INT0/INT1 Configuration

Bit	7	6	5	4	3	2	1	0
Name	IN1PL	IN1SL[2:0]			IN0PL	IN0SL[2:0]		
Туре	R/W	R/W			R/W		R/W	
Reset	0	0	0	0	0	0	0	1

SFR Page = 0x0; SFR Address = 0xE4

Bit	Name	Function
7	IN1PL	INT1 Polarity. 0: INT1 input is active low. 1: INT1 input is active high.
6:4	IN1SL[2:0]	INT1 Port Pin Selection Bits. These bits select which Port pin is assigned to INT1. Note that this pin assignment is independent of the Crossbar; INT1 will monitor the assigned Port pin without disturb- ing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7
3	IN0PL	INTO Polarity. 0: INTO input is active low. 1: INTO input is active high.
2:0	INOSL[2:0]	INTO Port Pin Selection Bits. These bits select which Port pin is assigned to INTO. Note that this pin assignment is independent of the Crossbar; INTO will monitor the assigned Port pin without disturb- ing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.7



14. Flash Memory

On-chip, re-programmable Flash memory is included for program code and non-volatile data storage. The Flash memory can be programmed in-system through the C2 interface or by software using the MOVX write instruction. Once cleared to logic 0, a Flash bit must be erased to set it back to logic 1. Flash bytes would typically be erased (set to 0xFF) before being reprogrammed. The write and erase operations are automatically timed by hardware for proper execution; data polling to determine the end of the write/erase operations is not required. Code execution is stalled during Flash write/erase operations. Refer to Table 4.6 for complete Flash memory electrical characteristics.

14.1. Programming the Flash Memory

The simplest means of programming the Flash memory is through the C2 interface using programming tools provided by Silicon Laboratories or a third party vendor. This is the only means for programming a non-initialized device. For details on the C2 commands to program Flash memory, see Section "27. C2 Interface" on page 319.

The Flash memory can be programmed by software using the MOVX write instruction with the address and data byte to be programmed provided as normal operands. Before programming Flash memory using MOVX, Flash programming operations must be enabled by: (1) setting the PSWE Program Store Write Enable bit (PSCTL.0) to logic 1 (this directs the MOVX writes to target Flash memory); and (2) Writing the Flash key codes in sequence to the Flash Lock register (FLKEY). The PSWE bit remains set until cleared by software. For detailed guidelines on programming Flash from firmware, please see Section "14.5. Flash Write and Erase Guidelines" on page 156.

To ensure the integrity of the Flash contents, the on-chip VDD Monitor must be enabled and enabled as a reset source in any system that includes code that writes and/or erases Flash memory from software. Furthermore, there should be no delay between enabling the V_{DD} Monitor and enabling the V_{DD} Monitor as a reset source. Any attempt to write or erase Flash memory while the V_{DD} Monitor is disabled, or not enabled as a reset source, will cause a Flash Error device reset.

14.1.1. Flash Lock and Key Functions

Flash writes and erases by user software are protected with a lock and key function. The Flash Lock and Key Register (FLKEY) must be written with the correct key codes, in sequence, before Flash operations may be performed. The key codes are: 0xA5, 0xF1. The timing does not matter, but the codes must be written in order. If the key codes are written out of order, or the wrong codes are written, Flash writes and erases will be disabled until the next system reset. Flash writes and erases will also be disabled if a Flash write or erase is attempted before the key codes have been written properly. The Flash lock resets after each write or erase; the key codes must be written again before a following Flash operation can be performed. The FLKEY register is detailed in SFR Definition 14.4.



14.3. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to 1 before software can modify the Flash memory; both PSWE and PSEE must be set to 1 before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. See Section "10. Memory Organization" on page 128 for the location of the security byte. The Flash security mechanism allows the user to lock n 512-byte Flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where n is the 1s complement number represented by the Security Lock Byte. The page containing the Flash Security Lock Byte is unlocked when no other Flash pages are locked (all bits of the Lock Byte is 0).

Security Lock Byte:	1111 1011b
ones Complement:	0000 0100b
Flash pages locked:	5 (First four Flash pages + Lock Byte Page)



Figure 14.1. Flash Program Memory Map (8 kB and smaller devices)

The level of Flash security depends on the Flash access method. The three Flash access methods that can be restricted are reads, writes, and erases from the C2 debug interface, user firmware executing on unlocked pages, and user firmware executing on locked pages. Table 14.1 summarizes the Flash security features of the C8051F99x-C8051F98x devices.



SFR Definition 14.2. REVID: Revision Identification

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xE2

Bit	Name	Function
7:0	REVID[7:0]	Revision Identification.
		These bits contain a value that can be decoded to determine the silicon revision. For example, 0x00 for Rev A, 0x01 for Rev B, 0x02 for Rev C, etc.



15. Power Management

C8051F99x-C8051F98x devices support 5 power modes: Normal, Idle, Stop, Suspend, and Sleep. The power management unit (PMU0) allows the device to enter and wake-up from the available power modes. A brief description of each power mode is provided in Table 15.1. Detailed descriptions of each mode can be found in the following sections.

Power Mode	Description	Wake-Up Sources	Power Savings
Normal	Device fully functional	N/A	Excellent MIPS/mW
Idle	All peripherals fully functional. Very easy to wake up.	Any Interrupt	Good No Code Execution
Stop	Legacy 8051 low power mode. A reset is required to wake up.	Any Reset	Good No Code Execution Precision Oscillator Disabled
Suspend	Similar to Stop Mode, but very fast wake-up time and code resumes execution at the next instruction.	CS0, SmaRTClock, Port Match, Comparator0, RST pin	Very Good No Code Execution All Internal Oscillators Disabled System Clock Gated
Sleep	Ultra Low Power and flexible wake-up sources. Code resumes execution at the next instruction. Comparator0 only functional in two-cell mode.	SmaRTClock, Port Match, Comparator0, RST pin	Excellent Power Supply Gated All Oscillators except SmaRT- Clock Disabled

In battery powered systems, the system should spend as much time as possible in sleep mode in order to preserve battery life. When a task with a fixed number of clock cycles needs to be performed, the device should switch to normal mode, finish the task as quickly as possible, and return to sleep mode. Idle mode and suspend modes provide a very fast wake-up time; however, the power savings in these modes will not be as much as in sleep mode. Stop mode is included for legacy reasons; the system will be more power efficient and easier to wake up when idle, suspend, or sleep mode are used.

Although switching power modes is an integral part of power management, enabling/disabling individual peripherals as needed will help lower power consumption in all power modes. Each analog peripheral can be disabled when not in use or placed in a low power mode. Digital peripherals such as timers or serial busses draw little power whenever they are not in use. Digital peripherals draw no power in sleep mode.



RAM and SFR register contents are preserved in sleep mode as long as the voltage on V_{DD} does not fall below V_{POR} . The PC counter and all other volatile state information is preserved allowing the device to resume code execution upon waking up from sleep mode.

Important Note: On device reset or upon waking up from Sleep mode, address 0x0000 of external memory may be overwritten by an indeterminate value. The indeterminate value is 0x00 in most situations. A dummy variable should be placed at address 0x0000 in external memory to ensure that the application firmware does not store any data that needs to be retained during sleep or reset at this memory location.

The following wake-up sources can be configured to wake the device from sleep mode:

- SmaRTClock Oscillator Fail
- SmaRTClock Alarm
- Port Match Event
- Comparator0 Rising Edge

The comparator requires a supply voltage of at least 1.8 V to operate properly. On C8051F99x-C8051F98x devices, the POR supply monitor can be disabled to save power by writing 1 to the MONDIS (PMU0MD.5) bit. When the POR supply monitor is disabled, all reset sources will trigger a full POR and will re-enable the POR supply monitor.

Important Note: The POR Supply Monitor should not be disabled if the supply voltage is greater than 2.4 V. The lowest power sleep mode current, 10 nA typical, can only be achieved when the supply voltage is less than 2.4 V. The lowest power sleep mode for voltages above 2.4 V is 50 nA typical with the POR Supply Monitor enabled.

In addition, any falling edge on \overrightarrow{RST} (due to a pin reset or a noise glitch) will cause the device to exit sleep mode. In order for the MCU to respond to the pin reset event, software must not place the device back into sleep mode for a period of 15 µs. The PMU0CF register may be checked to determine if the wake-up was due to a falling edge on the RST pin. If the wake-up source is not due to a falling edge on RST, there is no time restriction on how soon software may place the device back into sleep mode. A 4.7 kΩ pullup resistor to VDD is recommend for RST to prevent noise glitches from waking the device.

15.6. Configuring Wakeup Sources

Before placing the device in a low power mode, one or more wakeup sources should be enabled so that the device does not remain in the low power mode indefinitely. For Idle Mode, this includes enabling any interrupt. For Stop Mode, this includes enabling any reset source or relying on the RST pin to reset the device.

Wake-up sources for suspend and sleep modes are configured through the PMU0CF register. Wake-up sources are enabled by writing 1 to the corresponding wake-up source enable bit. Wake-up sources must be re-enabled each time the device is placed in suspend or sleep mode, in the same write that places the device in the low power mode.

The reset pin is always enabled as a wake-up source. On the falling edge of \overline{RST} , the device will be awaken from sleep mode. The device must remain awake for more than 15 µs in order for the reset to take place.



SFR Definition 15.1. PMU0CF: Power Management Unit Configuration^{1,2,3}

Bit	7	6	5	4	3	2	1	0
Name	SLEEP	SUSPEND	CLEAR	RSTWK	RTCFWK	RTCAWK	PMATWK	CPT0WK
Туре	W	W	W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	Varies	Varies	Varies	Varies	Varies

SFR Page = 0x0; SFR Address = 0xB5

Bit	Name	Description	Write	Read
7	SLEEP	Sleep Mode Select	Writing 1 places the device in Sleep Mode.	N/A
6	SUSPEND	Suspend Mode Select	Writing 1 places the device in Suspend Mode.	N/A
5	CLEAR	Wake-up Flag Clear	Writing 1 clears all wake- up flags.	N/A
4	RSTWK	Reset Pin Wake-up Flag	N/A	Set to 1 if a glitch <u>has</u> been detected on RST.
3	RTCFWK	SmaRTClock Oscillator Fail Wake-up Source Enable and Flag	0: Disable wake-up on SmaRTClock Osc. Fail. 1: Enable wake-up on SmaRTClock Osc. Fail.	Set to 1 if the SmaRT- Clock Oscillator has failed.
2	RTCAWK	SmaRTClock Alarm Wake-up Source Enable and Flag	0: Disable wake-up on SmaRTClock Alarm. 1: Enable wake-up on SmaRTClock Alarm.	Set to 1 if a SmaRTClock Alarm has occurred.
1	PMATWK	Port Match Wake-up Source Enable and Flag	0: Disable wake-up on Port Match Event. 1: Enable wake-up on Port Match Event.	Set to 1 if a Port Match Event has occurred.
0	CPTOWK	Comparator0 Wake-up Source Enable and Flag	0: Disable wake-up on Comparator0 rising edge. 1: Enable wake-up on Comparator0 rising edge.	Set to 1 if Comparator0 rising edge caused the last wake-up.

Notes:

1. Read-modify-write operations (ORL, ANL, etc.) should not be used on this register. Wake-up sources must be re-enabled each time the SLEEP or SUSPEND bits are written to 1.

2. The Low Power Internal Oscillator cannot be disabled and the MCU cannot be placed in Suspend or Sleep Mode if any wake-up flags are set to 1. Software should clear all wake-up sources after each reset and after each wake-up from Suspend or Sleep Modes.

3. PMU0 requires two system clocks to update the wake-up source flags after waking from Suspend mode. The wake-up source flags will read '0' during the first two system clocks following the wake from Suspend mode.



SFR Definition 15.2. PMU0FL: Power Management Unit Flag^{1,2}

Bit	7	6	5	4	3	2	1	0
Name								CS0WK
Туре	R	R	R	R	R	R	R	R/W
Reset	0	0	0	0	0	0	0	Varies

SFR Page = 0x0; SFR Address = 0xCE

Bit	Name	Description	Write	Read
7:1	Unused	Unused	Don't Care.	000000b
0	CSOWK	CS0 Wake-up Source Enable and Flag	0: Disable wake-up on CS0 event. 1: Enable wake-up on CS0 event.	Set to 1 if CS0 event caused the last wake-up.

Notes:

1. The Low Power Internal Oscillator cannot be disabled and the MCU cannot be placed in Suspend or Sleep Mode if any wake-up flags are set to 1. Software should clear all wake-up sources after each reset and after each wake-up from Suspend or Sleep Modes.

2. PMU0 requires two system clocks to update the wake-up source flags after waking from Suspend mode. The wake-up source flags will read '0' during the first two system clocks following the wake from Suspend mode.



SFR Definition 18.2. RSTSRC: Reset Source

Bit	7	6	5	4	3	2	1	0
Name	RTC0RE	FERROR	CORSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF
Туре	R/W	R	R/W	R/W	R	R/W	R/W	R
Reset	Varies							

SFR Page = 0x0; SFR Address = 0xEF.

Bit	Name	Description	Write	Read
7	RTC0RE	SmaRTClock Reset Enable and Flag	0: Disable SmaRTClock as a reset source. 1: Enable SmaRTClock as a reset source.	Set to 1 if SmaRTClock alarm or oscillator fail caused the last reset.
6	FERROR	Flash Error Reset Flag.	N/A	Set to 1 if Flash read/write/erase error caused the last reset.
5	CORSEF	Comparator0 Reset Enable and Flag.	0: Disable Comparator0 as a reset source.1: Enable Comparator0 as a reset source.	Set to 1 if Comparator0 caused the last reset.
4	SWRSF	Software Reset Force and Flag.	Writing a 1 forces a sys- tem reset.	Set to 1 if last reset was caused by a write to SWRSF.
3	WDTRSF	Watchdog Timer Reset Flag.	N/A	Set to 1 if Watchdog Timer overflow caused the last reset.
2	MCDRSF	Missing Clock Detector (MCD) Enable and Flag.	0: Disable the MCD. 1: Enable the MCD. The MCD triggers a reset if a missing clock condition is detected.	Set to 1 if Missing Clock Detector timeout caused the last reset.
1	PORSF	Power-On / Power-Fail Reset Flag, and Power-Fail Reset Enable.	 0: Disable the VDD Supply Monitor as a reset source. 1: Enable the VDD Supply Monitor as a reset source.³ 	Set to 1 anytime a power- on or V _{DD} monitor reset occurs. ²
0	PINRSF	HW Pin Reset Flag.	N/A	Set to 1 if RST pin caused the last reset.
Notes	5:			

1. It is safe to use read-modify-write operations (ORL, ANL, etc.) to enable or disable specific interrupt sources.

- 2. If PORSF read back 1, the value read from all other bits in this register are indeterminate.
- 3. Writing a 1 to PORSF before the VDD Supply Monitor is stabilized may generate a system reset.



Internal Register Definition 20.4. RTC0CN: SmaRTClock Control

Bit	7	6	5	4 3 2 1 0						
Name	RTC0EN	MCLKEN	OSCFAIL	RTC0TR	RTC0AEN	ALRM	RTC0SET	RTC0CAP		
Туре	Type R/W R/W R/W R/W R/W					R/W	R/W	R/W		
Reset	et 0 0 Varies 0 0 0 0							0		
SmaR	Clock Add	ress = $0x04$								
Bit	Name	Name Function								
7	RTC0EN	SmaRTClock	Enable.							
		Enables/disable 0: SmaRTClock 1: SmaRTClock	Enables/disables the SmaRTClock oscillator and associated bias currents.): SmaRTClock oscillator disabled. 1: SmaRTClock oscillator enabled.							
6	MCLKEN	Missing SmaR	TClock Dete	ctor Enable.						
		Enables/disable 0: Missing Sma 1: Missing Sma	Enables/disables the missing SmaRTClock detector. D: Missing SmaRTClock detector disabled. 1: Missing SmaRTClock detector enabled.							
5	OSCFAIL	SmaRTClock	Oscillator Fai	I Event Flag	•					
		Set by hardwar software. The v oscillator is dis	e when a mis alue of this bi abled.	sing SmaRT(t is not define	Clock detector ed when the Sr	timeout occu naRTClock	rs. Must be cle	eared by		
4	RTC0TR	SmaRTClock	Timer Run Co	ontrol.						
		Controls if the 3 0: SmaRTCloc 1: SmaRTCloc	SmaRTClock t k timer is stop k timer is runn	timer is runni ped. ing.	ng or stopped	(holds currer	it value).			
3	RTC0AEN	SmaRTClock	Alarm Enable							
		Enables/disable 0: SmaRTClock 1: SmaRTClock	es the SmaRT k alarm disabl k alarm enable	Clock alarm ed. ed.	function. Also	clears the Al	.RM flag.			
2	ALRM	SmaRTClock	Alarm Event	Read:		Wri	te:			
		Flag and Auto Reads return the alarm event fla Writes enable/of Auto Reset fun	Reset Enables be state of the g. disable the ction.	e. 0: Smal flag is d 1: Smal flag is a	RTClock alarm e-asserted. RTClock alarm sserted.	event 0: 1 1: E event	Disable Auto R Enable Auto Re	eset. eset.		
1	RTC0SET	SmaRTClock	Timer Set.							
		Writing 1 initiates a SmaRTClock timer set operation. This bit is cleared to 0 by hardware to indi- cate that the timer set operation is complete.								
0	RTC0CAP	SmaRTClock	Timer Captur	e.						
		Writing 1 initiates a SmaRTClock timer capture operation. This bit is cleared to 0 by hardware to indicate that the timer capture operation is complete.								
Note:	The ALRM flag will remain asserted for a maximum of one SmaRTClock cycle. See Section "Power Management" on page 162 for information on how to capture a SmaRTClock Alarm event using a flag which is not automatically cleared by hardware.									



Table 22.5. SMBus Status Decoding With Hardware ACK Generation Disabled (EHACK = 0)(Continued)

	Valu	Values Read			Va V	lues Nrit	sto e	:us ected		
Mode	Status Vector	ACKRQ	ARBLOST	ACK	Current SMbus State	Typical Response Options	STA	STO	ACK	Next Sta Vector Exp
<u> </u>		0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	Х	0001
smitte	0100	0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	х	0100
ve Tran		0	1	x	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	х	0001
Slav	0101	0	x	х	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	х	
						If Write, Acknowledge received address	0	0	1	0000
		1	0	Х	received; ACK requested.	If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	—
	0010					If Write, Acknowledge received address	0	0	1	0000
eiver		1	1	x	Lost arbitration as master; slave address + R/W received;	If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
sece					ACK requested.	NACK received address.	0	0	0	—
slave R						Reschedule failed transfer; NACK received address.	1	0	0	1110
(0)	0001	0001 A STOP was detected while addressed as a Slave Trans- mitter or Slave Receiver.		A STOP was detected while addressed as a Slave Trans- mitter or Slave Receiver.	Clear STO.	0	0	х		
		1	1 X Lost arbitration while attempt- ing a STOP.		Lost arbitration while attempt- ing a STOP.	No action required (transfer complete/aborted).	0	0	0	
	0000	1	0	x	A slave byte was received;	Acknowledge received byte; Read SMB0DAT.	0	0	1	0000
						NACK received byte.	0	0	0	
on	0010	0	1	x	Lost arbitration while attempt-	Abort failed transfer.	0	0	Х	—
nditi		Ľ			ing a repeated START.	Reschedule failed transfer.	1	0	Х	1110
Ö	0001	0	1	х	Lost arbitration due to a	Abort failed transfer.	0	0	Х	—
:rror					detected STOP.	Reschedule failed transfer.	1	0	Х	1110
SL	0000	1	1	х	Lost arbitration while transmit-	Abort failed transfer.	0	0	0	—
щ					ting a data byte as master.	Reschedule failed transfer.	1	0	0	1110





Figure 25.1. T0 Mode 0 Block Diagram

25.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.



SFR Definition 25.14. TMR3RLL: Timer 3 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0			
Name	TMR3RLL[7:0]										
Туре	R/W										
Reset	0	0	0	0	0	0	0	0			
SFR Pa	SFR Page = 0x0; SFR Address = 0x92										
D ''											

Bit	Name	Function					
7:0	TMR3RLL[7:0]	Timer 3 Reload Register Low Byte.					
		TMR3RLL holds the low byte of the reload value for Timer 3.					

SFR Definition 25.15. TMR3RLH: Timer 3 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0		
Name TMR3RLH[7:0]										
Type R/W										
Rese	et O	0	0	0	0	0	0	0		
SFR F	SFR Page = 0x0; SFR Address = 0x93									
Bit	Name		Function							
7:0	TMR3RLH[7:0] Timer 3 I	Timer 3 Reload Register High Byte.							
		TMR3RLH holds the high byte of the reload value for Timer 3.								



298

26.3.3. High-Speed Output Mode

In High-Speed Output mode, a module's associated CEXn pin is toggled each time a match occurs between the PCA Counter and the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode. If ECOMn is cleared, the associated pin will retain its state, and not toggle on the next match event.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.





26.3.4. Frequency Output Mode

Frequency Output Mode produces a programmable-frequency square wave on the module's associated CEXn pin. The capture/compare module high byte holds the number of PCA clocks to count before the output is toggled. The frequency of the square wave is then defined by Equation 26.1.

$$F_{CEXn} = \frac{F_{PCA}}{2 \times PCA0CPHn}$$

Note: A value of 0x00 in the PCA0CPHn register is equal to 256 for this equation.

Equation 26.1. Square Wave Frequency Output

