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Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f989-c-gmr

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C8051F99x-C8051F98x

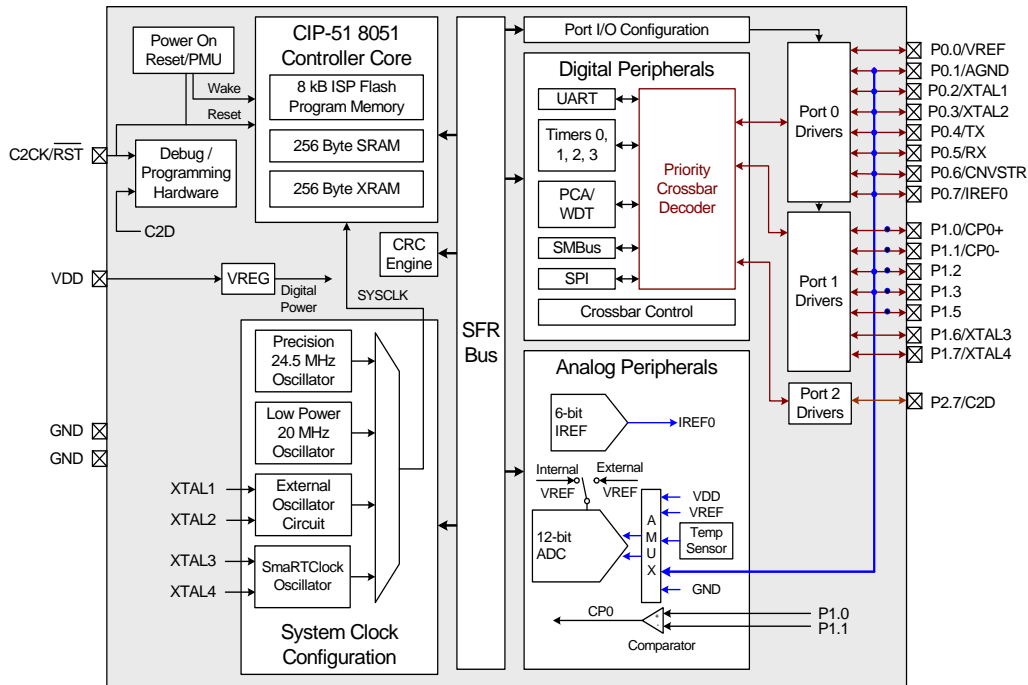


Figure 1.1. C8051F980 Block Diagram

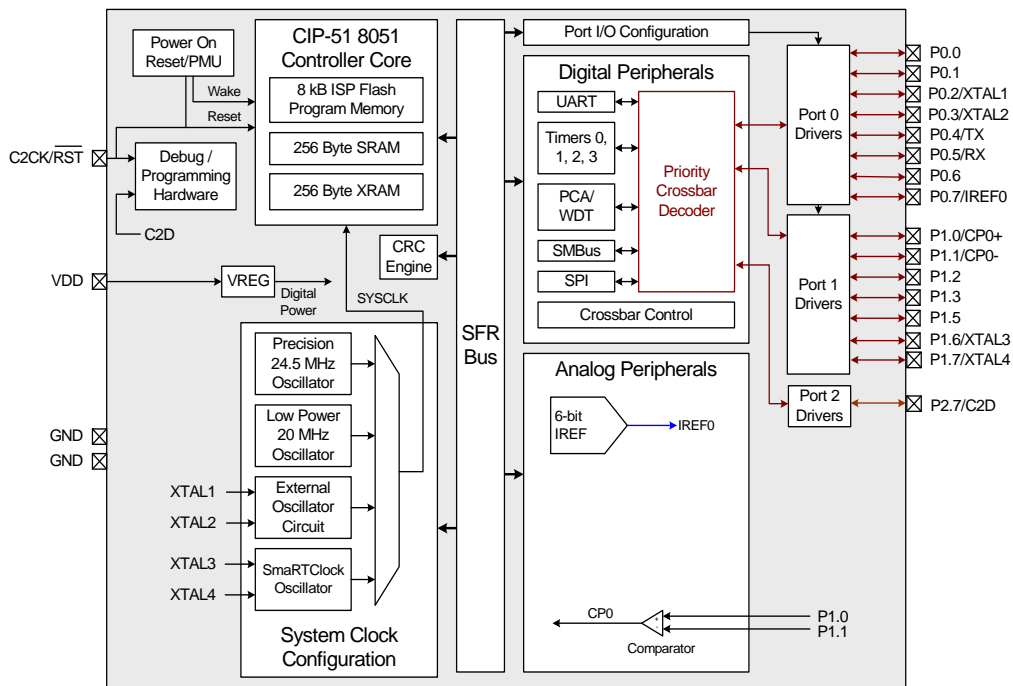


Figure 1.2. C8051F981 Block Diagram

C8051F99x-C8051F98x

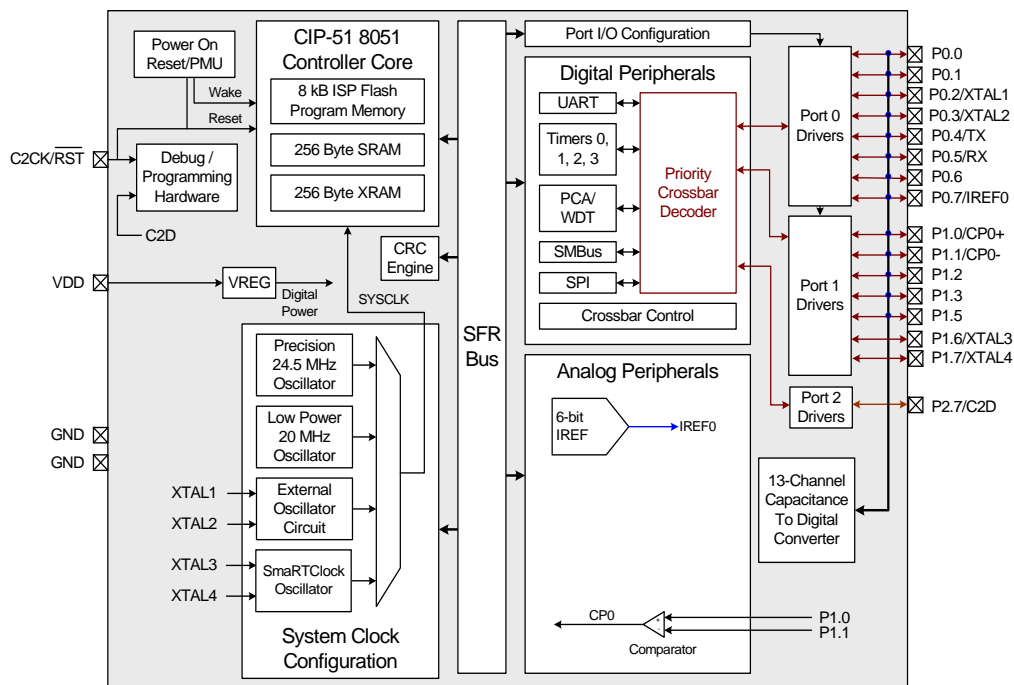


Figure 1.11. C8051F991 Block Diagram

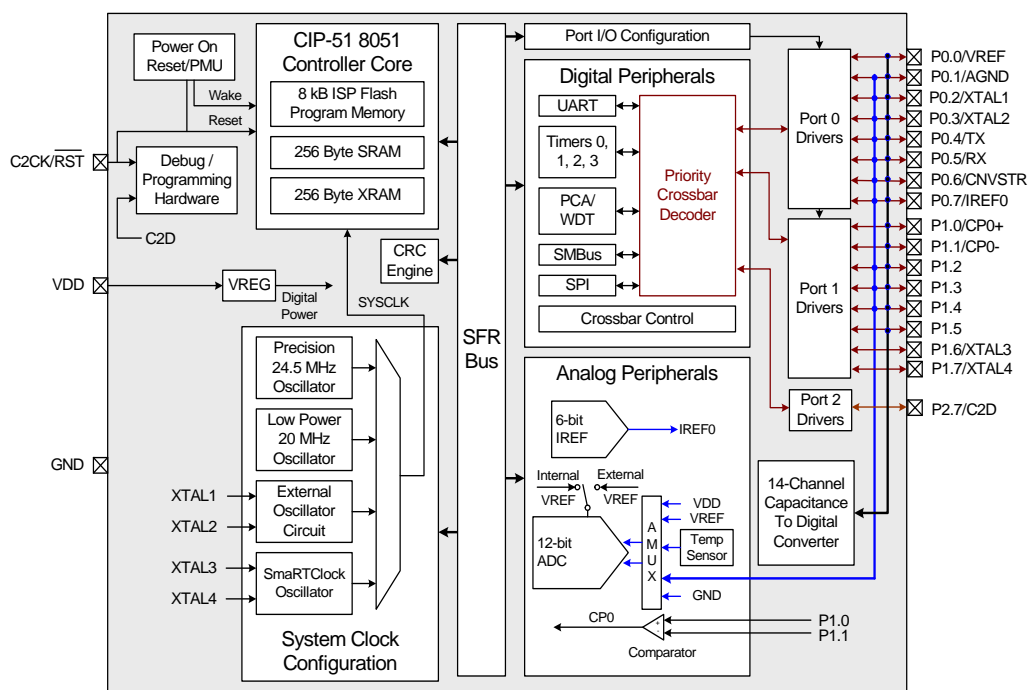


Figure 1.12. C8051F996 Block Diagram

C8051F99x-C8051F98x

1.3. Serial Ports

The C8051F99x-C8051F98x Family includes an SMBus/I²C interface, a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.4. Programmable Counter Array

An on-chip programmable counter/timer array (PCA) is included in addition to the four 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with three programmable capture/compare modules. The PCA clock is derived from one of seven sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, an External Clock Input (ECI), the system clock, the external oscillator clock source divided by 8, or the SmartClock divided by 8.

Each capture/compare module can be configured to operate in a variety of modes: edge-triggered capture, software timer, high-speed output, pulse width modulator (8, 9, 10, 11, or 16-bit), or frequency output. Additionally, Capture/Compare Module 2 offers watchdog timer (WDT) capabilities. Following a system reset, Module 2 is configured and enabled in WDT mode. The PCA Capture/Compare Module I/O and External Clock Input may be routed to Port I/O via the Digital Crossbar.

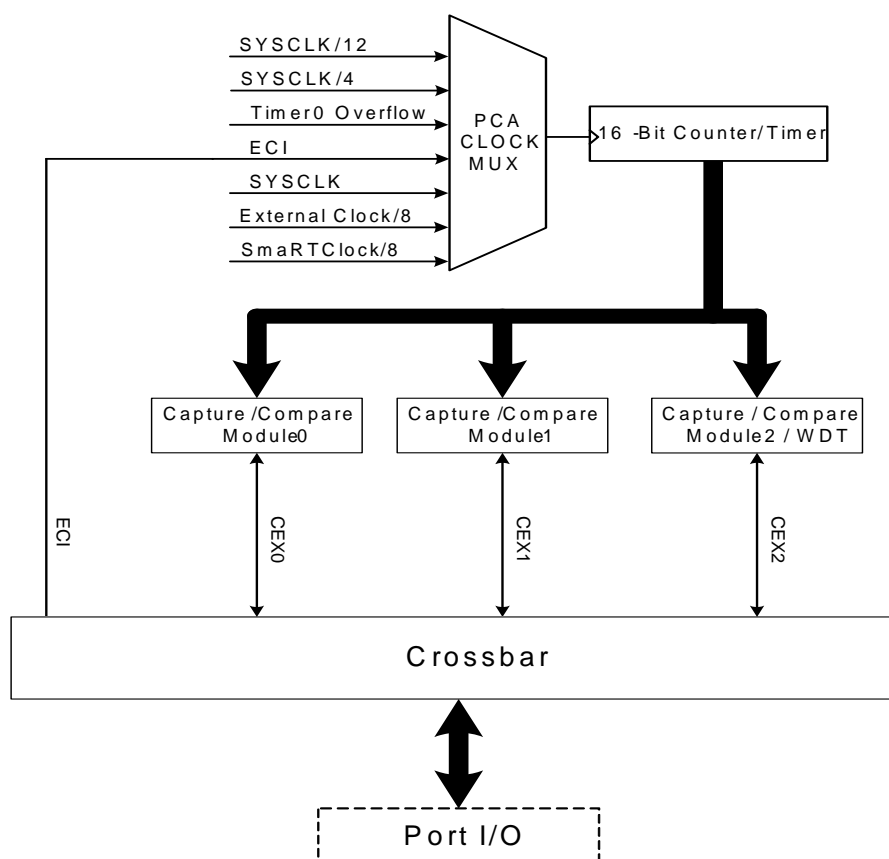


Figure 1.15. PCA Block Diagram

C8051F99x-C8051F98x

2. Ordering Information

Table 2.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (bytes)	SmartClock Real Time Clock	SMBus/I ² C, UART, Enhanced SPI	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	Analog to Digital Converter Inputs	ADC with internal voltage reference and temperature sensor	Capacitive Touch Inputs	Programmable Current Reference	Analog Comparators	Lead-free (RoHS Compliant)	Package
C8051F980-C-GM	25	8	512	✓	✓	4	✓	16	9	12-bit	—	✓	1	✓	QFN-20
C8051F981-C-GM	25	8	512	✓	✓	4	✓	16	—	—	—	✓	1	✓	QFN-20
C8051F982-C-GM	25	4	512	✓	✓	4	✓	16	9	10-bit	—	✓	1	✓	QFN-20
C8051F983-C-GM	25	4	512	✓	✓	4	✓	16	—	—	—	✓	1	✓	QFN-20
C8051F985-C-GM	25	2	512	✓	✓	4	✓	16	—	—	—	✓	1	✓	QFN-20
C8051F986-C-GM	25	8	512	✓	✓	4	✓	17	10	12-bit	—	✓	1	✓	QFN-24
C8051F986-C-GU	25	8	512	✓	✓	4	✓	17	10	12-bit	—	✓	1	✓	QSOP-24
C8051F987-C-GM	25	8	512	✓	✓	4	✓	17	—	—	—	✓	1	✓	QFN-24
C8051F987-C-GU	25	8	512	✓	✓	4	✓	17	—	—	—	✓	1	✓	QSOP-24
C8051F988-C-GM	25	4	512	✓	✓	4	✓	17	10	10-bit	—	✓	1	✓	QFN-24
C8051F988-C-GU	25	4	512	✓	✓	4	✓	17	10	10-bit	—	✓	1	✓	QSOP-24
C8051F989-C-GM	25	4	512	✓	✓	4	✓	17	—	—	—	✓	1	✓	QFN-24
C8051F989-C-GU	25	4	512	✓	✓	4	✓	17	—	—	—	✓	1	✓	QSOP-24
C8051F990-C-GM	25	8	512	✓	✓	4	✓	16	9	12-bit	13	✓	1	✓	QFN-20
C8051F991-C-GM	25	8	512	✓	✓	4	✓	16	—	—	13	✓	1	✓	QFN-20
C8051F996-C-GM	25	8	512	✓	✓	4	✓	17	10	12-bit	14	✓	1	✓	QFN-24
C8051F996-C-GU	25	8	512	✓	✓	4	✓	17	10	12-bit	14	✓	1	✓	QSOP-24
C8051F997-C-GM	25	8	512	✓	✓	4	✓	17	—	—	14	✓	1	✓	QFN-24
C8051F997-C-GU	25	8	512	✓	✓	4	✓	17	—	—	14	✓	1	✓	QSOP-24

Note: Starting with silicon revision C, the ordering part numbers have been updated to include the silicon revision and use this format: "C8051F990-C-GM". Package marking diagrams are included as Figure 3.4, Figure 3.5, and Figure 3.6 to identify the silicon revision.

C8051F99x-C8051F98x

Table 4.5. Power Management Electrical Specifications

$V_{DD} = 1.8$ to 3.6 V, -40 to $+85$ °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Idle Mode Wake-up Time		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	CLKDIV = 0x00 Low Power or Precision Osc.	—	400	—	ns
Sleep Mode Wake-up Time		—	2	—	μs

Table 4.6. Flash Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V, -40 to $+85$ °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	C8051F980/1/6/7, C8051F990/1/6/7	8192	—	—	bytes
	C8051F982/3/8/9	4096	—	—	bytes
	C8051F985	2048	—	—	bytes
Endurance		20 k	100k	—	Erase/Write Cycles
Erase Cycle Time		28	32	36	ms
Write Cycle Time		57	64	71	μs

Table 4.7. Internal Precision Oscillator Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V; $T_A = -40$ to $+85$ °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	-40 to $+85$ °C, $V_{DD} = 1.8$ – 3.6 V	24	24.5	25	MHz
Oscillator Supply Current (from V_{DD})	25 °C; includes bias current of 90 – 100 μA	—	300*	—	μA

***Note:** Does not include clock divider or clock tree supply current.

Table 4.8. Internal Low-Power Oscillator Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V; $T_A = -40$ to $+85$ °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	-40 to $+85$ °C, $V_{DD} = 1.8$ – 3.6 V	18	20	22	MHz
Oscillator Supply Current (from V_{DD})	25 °C No separate bias current required	—	100*	—	μA

***Note:** Does not include clock divider or clock tree supply current.

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Table 4.10. ADC0 Electrical Characteristics (Continued)

$V_{DD} = 1.8$ to 3.6 V, $V_{REF} = 1.65$ V ($REFSL[1:0] = 11$), -40 to $+85$ °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Inputs					
ADC Input Voltage Range	Single Ended ($A_{IN+} - GND$)	0	—	V_{REF}	V
Absolute Pin Voltage with respect to GND	Single Ended	0	—	V_{DD}	V
Sampling Capacitance	1x Gain	—	16	—	pF
	0.5x Gain	—	13	—	pF
Input Multiplexer Impedance		—	5	—	k Ω
Power Specifications					
Power Supply Current (V_{DD} supplied to ADC0)	Normal Power Mode:				
	Conversion Mode (300 ksps)	—	650	—	μ A
	Tracking Mode (0 ksps)	—	740	—	μ A
	Low Power Mode:				
	Conversion Mode (150 ksps)	—	370	—	μ A
	Tracking Mode (0 ksps)	—	400	—	μ A
Power Supply Rejection	Internal High Speed V_{REF}	—	67	—	dB
	External V_{REF}	—	74	—	dB
<ol style="list-style-type: none"> 1. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes. 2. The maximum code in 12-bit mode is 0xFFFC. The Full Scale Error is referenced from the maximum code. 3. Performance in 8-bit mode is similar to 10-bit mode. 					

Table 4.11. Temperature Sensor Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V, -40 to $+85$ °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Linearity		—	± 1	—	°C
Slope		—	3.40	—	mV/°C
Slope Error*		—	40	—	μ V/°C
Offset	Temp = 25 °C	—	1025	—	mV
Offset Error*	Temp = 25 °C	—	18	—	mV
Temperature Sensor Turn-On Time		—	1.7	—	μ s
Supply Current		—	35	—	μ A
*Note: Represents one standard deviation from the mean.					

5.2. Modes of Operation

ADC0 has a maximum conversion speed of 300 ksp/s in 10-bit mode. The ADC0 conversion clock (SARCLK) is a divided version of the system clock when burst mode is disabled (BURSTEN = 0), or a divided version of the low power oscillator when burst mode is enabled (BURSEN = 1). The clock divide value is determined by the AD0SC bits in the ADC0CF register.

5.2.1. Starting a Conversion

A conversion can be initiated in one of five ways, depending on the programmed states of the ADC0 Start of Conversion Mode bits (AD0CM2–0) in register ADC0CN. Conversions may be initiated by one of the following:

1. Writing a 1 to the AD0BUSY bit of register ADC0CN
2. A Timer 0 overflow (i.e., timed continuous conversions)
3. A Timer 2 overflow
4. A Timer 3 overflow
5. A rising edge on the CNVSTR input signal (pin P0.6)

Writing a 1 to AD0BUSY provides software control of ADC0 whereby conversions are performed "on-demand". During conversion, the AD0BUSY bit is set to logic 1 and reset to logic 0 when the conversion is complete. The falling edge of AD0BUSY triggers an interrupt (when enabled) and sets the ADC0 interrupt flag (AD0INT). When polling for ADC conversion completions, the ADC0 interrupt flag (AD0INT) should be used. Converted data is available in the ADC0 data registers, ADC0H:ADC0L, when bit AD0INT is logic 1. When Timer 2 or Timer 3 overflows are used as the conversion source, Low Byte overflows are used if Timer 2/3 is in 8-bit mode; High byte overflows are used if Timer 2/3 is in 16-bit mode. See "25. Timers" on page 278 for timer configuration.

Important Note About Using CNVSTR: The CNVSTR input pin also functions as Port pin P0.6. When the CNVSTR input is used as the ADC0 conversion source, Port pin P0.6 should be skipped by the Digital Crossbar. To configure the Crossbar to skip P0.6, set to 1 Bit 6 in register P0SKIP. See "21. Port Input/Output" on page 215 for details on Port I/O configuration.

SFR Definition 5.2. ADC0CF: ADC0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD0SC[4:0]					AD08BE	AD0TM	AMP0GN
Type	R/W					R/W	R/W	R/W
Reset	1	1	1	1	1	0	0	0

SFR Page = 0x0; SFR Address = 0x97

Bit	Name	Function
7:3	AD0SC[4:0]	ADC0 SAR Conversion Clock Divider. SAR Conversion clock is derived from FCLK by the following equation, where AD0SC refers to the 5-bit value held in bits AD0SC[4:0]. SAR Conversion clock requirements are given in Table 4.10. BURSTEN = 0: FCLK is the current system clock. BURSTEN = 1: FCLK is the 20 MHz low power oscillator, independent of the system clock. $AD0SC = \frac{FCLK}{CLK_{SAR}} - 1 *$ *Round the result up. or $CLK_{SAR} = \frac{FCLK}{AD0SC + 1}$
2	AD08BE	ADC0 8-Bit Mode Enable. 0: ADC0 operates in 10-bit mode (normal operation). 1: ADC0 operates in 8-bit mode.
1	AD0TM	ADC0 Track Mode. Selects between Normal or Delayed Tracking Modes. 0: Normal Track Mode: When ADC0 is enabled, conversion begins immediately following the start-of-conversion signal. 1: Delayed Track Mode: When ADC0 is enabled, conversion begins 3 SAR clock cycles following the start-of-conversion signal. The ADC is allowed to track during this time.
0	AMP0GN	ADC0 Gain Control. 0: The on-chip PGA gain is 0.5. 1: The on-chip PGA gain is 1.

SFR Definition 8.3. CS0DH: Capacitive Sense Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	CS0DH[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xEE

Bit	Name	Description
7:0	CS0DH	CS0 Data High Byte. Stores the high byte of the last completed 16-bit Capacitive Sense conversion.

SFR Definition 8.4. CS0DL: Capacitive Sense Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	CS0DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xED

Bit	Name	Description
7:0	CS0DL	CS0 Data Low Byte. Stores the low byte of the last completed 16-bit Capacitive Sense conversion.

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SFR Definition 13.1. IE: Interrupt Enable

Bit	7	6	5	4	3	2	1	0
Name	EA	ESPI0	ET2	ES0	ET1	EX1	ET0	EX0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All; SFR Address = 0xA8; Bit-Addressable

Bit	Name	Function
7	EA	Enable All Interrupts. Globally enables/disables all interrupts. It overrides individual interrupt mask settings. 0: Disable all interrupt sources. 1: Enable each interrupt according to its individual mask setting.
6	ESPI0	Enable Serial Peripheral Interface (SPI0) Interrupt. This bit sets the masking of the SPI0 interrupts. 0: Disable all SPI0 interrupts. 1: Enable interrupt requests generated by SPI0.
5	ET2	Enable Timer 2 Interrupt. This bit sets the masking of the Timer 2 interrupt. 0: Disable Timer 2 interrupt. 1: Enable interrupt requests generated by the TF2L or TF2H flags.
4	ES0	Enable UART0 Interrupt. This bit sets the masking of the UART0 interrupt. 0: Disable UART0 interrupt. 1: Enable UART0 interrupt.
3	ET1	Enable Timer 1 Interrupt. This bit sets the masking of the Timer 1 interrupt. 0: Disable all Timer 1 interrupt. 1: Enable interrupt requests generated by the TF1 flag.
2	EX1	Enable External Interrupt 1. This bit sets the masking of External Interrupt 1. 0: Disable external interrupt 1. 1: Enable interrupt requests generated by the $\overline{\text{INT1}}$ input.
1	ET0	Enable Timer 0 Interrupt. This bit sets the masking of the Timer 0 interrupt. 0: Disable all Timer 0 interrupt. 1: Enable interrupt requests generated by the TF0 flag.
0	EX0	Enable External Interrupt 0. This bit sets the masking of External Interrupt 0. 0: Disable external interrupt 0. 1: Enable interrupt requests generated by the $\overline{\text{INT0}}$ input.

SFR Definition 13.7. IT01CF: $\overline{\text{INT0}}/\overline{\text{INT1}}$ Configuration

Bit	7	6	5	4	3	2	1	0
Name	IN1PL	IN1SL[2:0]			IN0PL	IN0SL[2:0]		
Type	R/W	R/W			R/W	R/W		
Reset	0	0	0	0	0	0	0	1

SFR Page = 0x0; SFR Address = 0xE4

Bit	Name	Function
7	IN1PL	$\overline{\text{INT1}}$ Polarity. 0: $\overline{\text{INT1}}$ input is active low. 1: $\overline{\text{INT1}}$ input is active high.
6:4	IN1SL[2:0]	$\overline{\text{INT1}}$ Port Pin Selection Bits. These bits select which Port pin is assigned to $\overline{\text{INT1}}$. Note that this pin assignment is independent of the Crossbar; $\overline{\text{INT1}}$ will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7
3	IN0PL	$\overline{\text{INT0}}$ Polarity. 0: $\overline{\text{INT0}}$ input is active low. 1: $\overline{\text{INT0}}$ input is active high.
2:0	IN0SL[2:0]	$\overline{\text{INT0}}$ Port Pin Selection Bits. These bits select which Port pin is assigned to $\overline{\text{INT0}}$. Note that this pin assignment is independent of the Crossbar; $\overline{\text{INT0}}$ will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7

SFR Definition 14.3. PSCTL: Program Store R/W Control

Bit	7	6	5	4	3	2	1	0
Name							PSEE	PSWE
Type	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page =All; SFR Address = 0x8F

Bit	Name	Function
7:2	Unused	Read = 000000b, Write = don't care.
1	PSEE	Program Store Erase Enable. Setting this bit (in combination with PSWE) allows an entire page of Flash program memory to be erased. If this bit is logic 1 and Flash writes are enabled (PSWE is logic 1), a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter. 0: Flash program memory erasure disabled. 1: Flash program memory erasure enabled.
0	PSWE	Program Store Write Enable. Setting this bit allows writing a byte of data to the Flash program memory using the MOVX write instruction. The Flash location should be erased before writing data. 0: Writes to Flash program memory disabled. 1: Writes to Flash program memory enabled; the MOVX write instruction targets Flash memory.

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SFR Definition 19.4. OSCXCN: External Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	XCLKVLD	XOSCMD[2:0]			Reserved	XFCN[2:0]		
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xB1

Bit	Name	Function
7	XCLKVLD	External Oscillator Valid Flag. Provides External Oscillator status and is valid at all times for all modes of operation except External CMOS Clock Mode and External CMOS Clock Mode with divide by 2. In these modes, XCLKVLD always returns 0. 0: External Oscillator is unused or not yet stable. 1: External Oscillator is running and stable.
6:4	XOSCMD	External Oscillator Mode Bits. Configures the external oscillator circuit to the selected mode. 00x: External Oscillator circuit disabled. 010: External CMOS Clock Mode. 011: External CMOS Clock Mode with divide by 2 stage. 100: RC Oscillator Mode. 101: Capacitor Oscillator Mode. 110: Crystal Oscillator Mode. 111: Crystal Oscillator Mode with divide by 2 stage.
3	Reserved	Read = 0b. Must Write 0b.
2:0	XFCN	External Oscillator Frequency Control Bits. Controls the external oscillator bias current. 000-111: See Table 19.1 on page 190 (Crystal Mode) or Table 19.2 on page 191 (RC or C Mode) for recommended settings.

20.1.5. RTC0ADR Autoincrement Feature

For ease of reading and writing the 32-bit CAPTURE and ALARM values, RTC0ADR automatically increments after each read or write to a CAPTUREn or ALARMn register. This speeds up the process of setting an alarm or reading the current SmarTClock timer value. Autoincrement is always enabled.

Recommended Instruction Timing for a multi-byte register read with short strobe and auto read enabled:

```
mov RTC0ADR, #0d0h
nop
nop
nop
nop
mov A, RTC0DAT
nop
nop
mov A, RTC0DAT
nop
nop
mov A, RTC0DAT
nop
nop
mov A, RTC0DAT
```

Recommended Instruction Timing for a multi-byte register write with short strobe enabled:

```
mov RTC0ADR, #010h
mov RTC0DAT, #05h
nop
mov RTC0DAT, #06h
nop
mov RTC0DAT, #07h
nop
mov RTC0DAT, #08h
nop
```

20.3.3. Software Considerations for using the SmaRTClock Timer and Alarm

The SmaRTClock timer and alarm have two operating modes to suit varying applications. The two modes are described below:

Mode 1:

The first mode uses the SmaRTClock timer as a perpetual timebase which is never reset to zero. Every 36 hours, the timer is allowed to overflow without being stopped or disrupted. The alarm interval is software managed and is added to the ALRMn registers by software after each alarm. This allows the alarm match value to always stay ahead of the timer by one software managed interval. If software uses 32-bit unsigned addition to increment the alarm match value, then it does not need to handle overflows since both the timer and the alarm match value will overflow in the same manner.

This mode is ideal for applications which have a long alarm interval (e.g., 24 or 36 hours) and/or have a need for a perpetual timebase. An example of an application that needs a perpetual timebase is one whose wake-up interval is constantly changing. For these applications, software can keep track of the number of timer overflows in a 16-bit variable, extending the 32-bit (36 hour) timer to a 48-bit (272 year) perpetual timebase.

Mode 2:

The second mode uses the SmaRTClock timer as a general purpose up counter which is auto reset to zero by hardware after each alarm. The alarm interval is managed by hardware and stored in the ALRMn registers. Software only needs to set the alarm interval once during device initialization. After each alarm, software should keep a count of the number of alarms that have occurred in order to keep track of time.

This mode is ideal for applications that require minimal software intervention and/or have a fixed alarm interval. This mode is the most power efficient since it requires less CPU time per alarm.

21.1. Port I/O Modes of Operation

Port pins P0.0–P1.7 use the Port I/O cell shown in Figure 21.2. Each Port I/O cell can be configured by software for analog I/O or digital I/O using the PnMDIN registers. On reset, all Port I/O cells default to a digital high impedance state with weak pull-ups enabled.

21.1.1. Port Pins Configured for Analog I/O

Any pins to be used as Comparator or ADC input, oscillator input/output, or AGND, VREF, or Current Reference output should be configured for analog I/O (PnMDIN.n = 0). When a pin is configured for analog I/O, its weak pullup and digital receiver are disabled. In most cases, software should also disable the digital output drivers. Port pins configured for analog I/O will always read back a value of 0 regardless of the actual voltage on the pin.

Configuring pins as analog I/O saves power and isolates the Port pin from digital interference. Port pins configured as digital inputs may still be used by analog peripherals; however, this practice is not recommended and may result in measurement errors.

21.1.2. Port Pins Configured For Digital I/O

Any pins to be used by digital peripherals (UART, SPI, SMBus, etc.), external digital event capture functions, or as GPIO should be configured as digital I/O (PnMDIN.n = 1). For digital I/O pins, one of two output modes (push-pull or open-drain) must be selected using the PnMDOUT registers.

Push-pull outputs (PnMDOUT.n = 1) drive the Port pad to the VDD or GND supply rails based on the output logic value of the Port pin. Open-drain outputs have the high side driver disabled; therefore, they only drive the Port pad to GND when the output logic value is 0 and become high impedance inputs (both high and low drivers turned off) when the output logic value is 1.

When a digital I/O cell is placed in the high impedance state, a weak pull-up transistor pulls the Port pad to the VDD supply voltage to ensure the digital input is at a defined logic state. Weak pull-ups are disabled when the I/O cell is driven to GND to minimize power consumption and may be globally disabled by setting WEAKPUD to 1. The user must ensure that digital I/O are always internally or externally pulled or driven to a valid logic state. Port pins configured for digital I/O always read back the logic state of the Port pad, regardless of the output logic value of the Port pin.

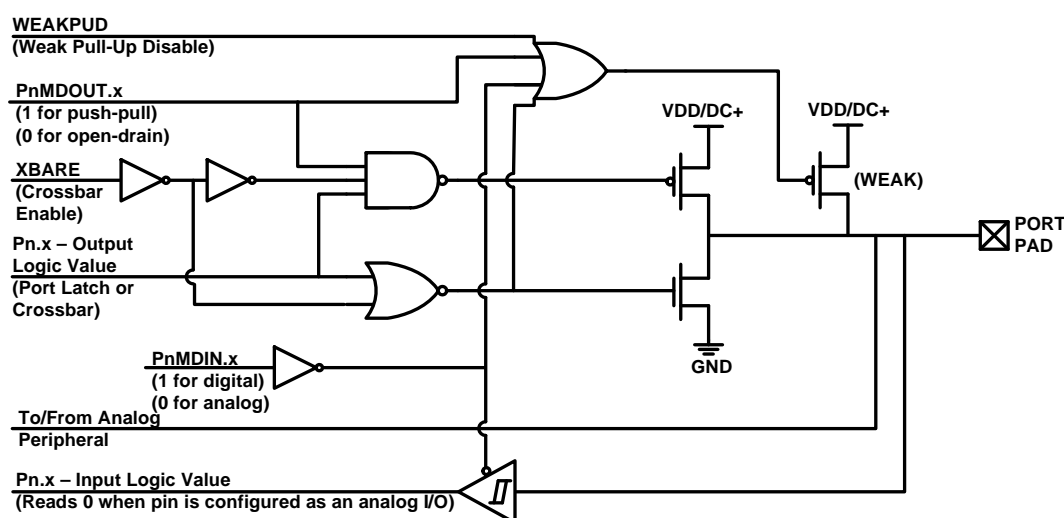


Figure 21.2. Port I/O Cell Block Diagram

SFR Definition 22.1. SMB0CF: SMBus Clock/Configuration

Bit	7	6	5	4	3	2	1	0
Name	ENSMB	INH	BUSY	EXTHOLD	SMBTOE	SMBFTE	SMBCS[1:0]	
Type	R/W	R/W	R	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC1

Bit	Name	Function
7	ENSMB	SMBus Enable. This bit enables the SMBus interface when set to 1. When enabled, the interface constantly monitors the SDA and SCL pins.
6	INH	SMBus Slave Inhibit. When this bit is set to logic 1, the SMBus does not generate an interrupt when slave events occur. This effectively removes the SMBus slave from the bus. Master Mode interrupts are not affected.
5	BUSY	SMBus Busy Indicator. This bit is set to logic 1 by hardware when a transfer is in progress. It is cleared to logic 0 when a STOP or free-timeout is sensed.
4	EXTHOLD	SMBus Setup and Hold Time Extension Enable. This bit controls the SDA setup and hold times according to Table 22.2. 0: SDA Extended Setup and Hold Times disabled. 1: SDA Extended Setup and Hold Times enabled.
3	SMBTOE	SMBus SCL Timeout Detection Enable. This bit enables SCL low timeout detection. If set to logic 1, the SMBus forces Timer 3 to reload while SCL is high and allows Timer 3 to count when SCL goes low. If Timer 3 is configured to Split Mode, only the High Byte of the timer is held in reload while SCL is high. Timer 3 should be programmed to generate interrupts at 25 ms, and the Timer 3 interrupt service routine should reset SMBus communication.
2	SMBFTE	SMBus Free Timeout Detection Enable. When this bit is set to logic 1, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods.
1:0	SMBCS[1:0]	SMBus Clock Source Selection. These two bits select the SMBus clock source, which is used to generate the SMBus bit rate. The selected device should be configured according to Equation 22.1. 00: Timer 0 Overflow 01: Timer 1 Overflow 10: Timer 2 High Byte Overflow 11: Timer 2 Low Byte Overflow

SFR Definition 25.8. TMR2CN: Timer 2 Control

Bit	7	6	5	4	3	2	1	0
Name	TF2H	TF2L	TF2LEN	TF2CEN	T2SPLIT	TR2	T2XCLK[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC8; Bit-Addressable

Bit	Name	Function
7	TF2H	Timer 2 High Byte Overflow Flag. Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF2L	Timer 2 Low Byte Overflow Flag. Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. TF2L will be set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.
5	TF2LEN	Timer 2 Low Byte Interrupt Enable. When set to 1, this bit enables Timer 2 Low Byte interrupts. If Timer 2 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 2 overflows.
4	TF2CEN	Timer 2 Capture Enable. When set to 1, this bit enables Timer 2 Capture Mode.
3	T2SPLIT	Timer 2 Split Mode Enable. When set to 1, Timer 2 operates as two 8-bit timers with auto-reload. Otherwise, Timer 2 operates in 16-bit auto-reload mode.
2	TR2	Timer 2 Run Control. Timer 2 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in split mode.
1:0	T2XCLK[1:0]	Timer 2 External Clock Select. This bit selects the “external” and “capture trigger” clock sources for Timer 2. If Timer 2 is in 8-bit mode, this bit selects the “external” clock source for both timer bytes. Timer 2 Clock Select bits (T2MH and T2ML in register CKCON) may still be used to select between the “external” clock and the system clock for either timer. Note: External clock sources are synchronized with the system clock. 00: External Clock is SYSCLK/12. Capture trigger is SmarTClock/8. 01: External Clock is Comparator 0. Capture trigger is SmarTClock/8. 10: External Clock is SYSCLK/12. Capture trigger is Comparator 0. 11: External Clock is SmarTClock/8. Capture trigger is Comparator 0.

C8051F99x-C8051F98x

SFR Definition 26.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	WDTE	WDLCK		CPS2	CPS1	CPS0	ECF
Type	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xD9

Bit	Name	Function
7	CIDL	PCA Counter/Timer Idle Control. Specifies PCA behavior when CPU is in Idle Mode. 0: PCA continues to function normally while the system controller is in Idle Mode. 1: PCA operation is suspended while the system controller is in Idle Mode.
6	WDTE	Watchdog Timer Enable. If this bit is set, PCA Module 2 is used as the watchdog timer. 0: Watchdog Timer disabled. 1: PCA Module 2 enabled as Watchdog Timer.
5	WDLCK	Watchdog Timer Lock. This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset. 0: Watchdog Timer Enable unlocked. 1: Watchdog Timer Enable locked.
4	Unused	Read = 0b, Write = don't care.
3:1	CPS[2:0]	PCA Counter/Timer Pulse Select. These bits select the timebase source for the PCA counter 000: System clock divided by 12 001: System clock divided by 4 010: Timer 0 overflow 011: High-to-low transitions on ECI (max rate = system clock divided by 4) 100: System clock 101: External clock divided by 8 (synchronized with the system clock) 110: SmarTClock divided by 8 (synchronized with the system clock) 111: Reserved
0	ECF	PCA Counter/Timer Overflow Interrupt Enable. This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.
Note: When the WDTE bit is set to 1, the other bits in the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.		