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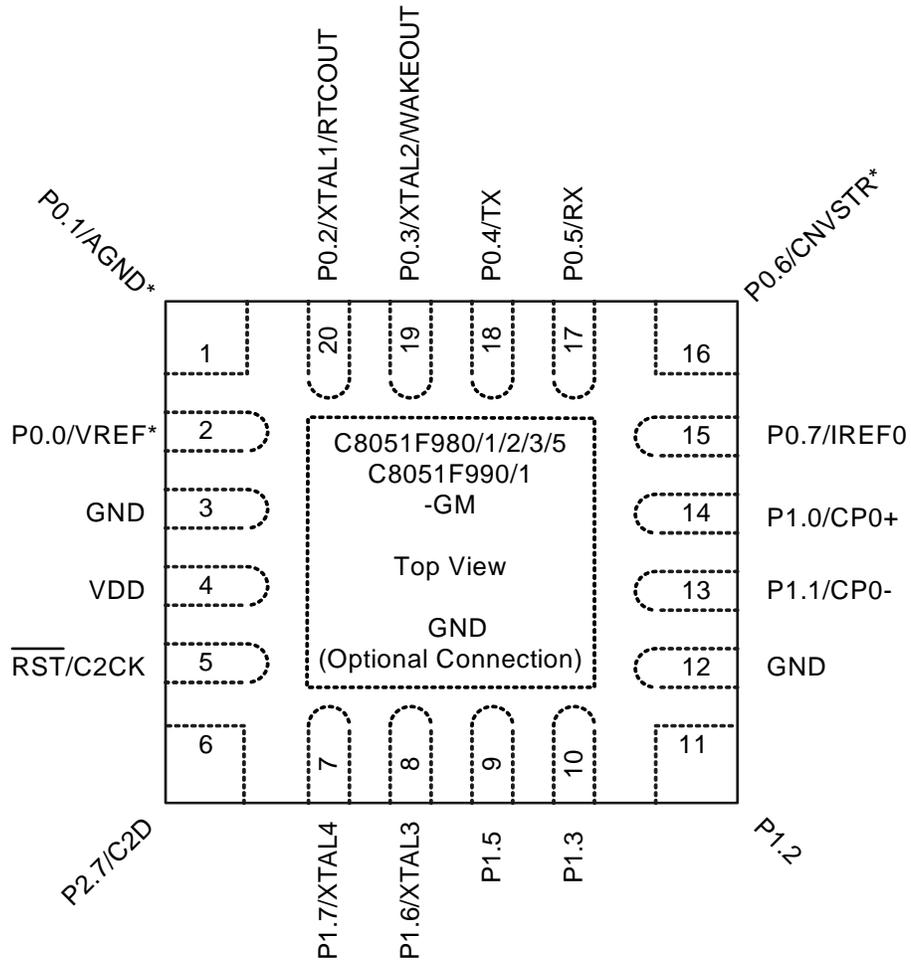
### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I <sup>2</sup> C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/c8051f989-gm">https://www.e-xfl.com/product-detail/silicon-labs/c8051f989-gm</a>



**\*Note:** Signal only available on 'F980, 'F982 and 'F990 devices.

**Figure 3.1. QFN-20 Pinout Diagram (Top View)**

**Table 3.3. PCB Land Pattern**

Dimension	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 REF	
GD	2.10	—
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

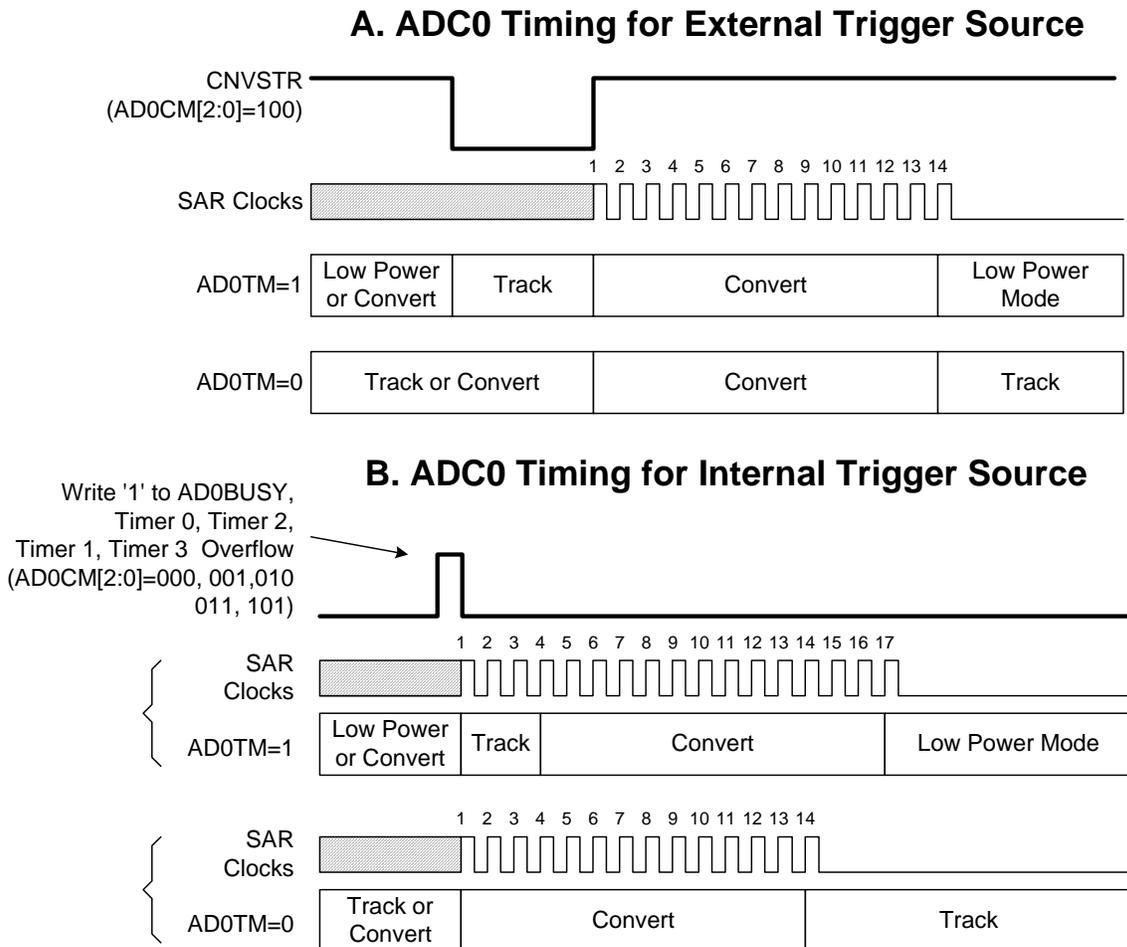
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 5.2.2. Tracking Modes

Each ADC0 conversion must be preceded by a minimum tracking time in order for the converted result to be accurate. The minimum tracking time is given in Table 4.10. The AD0TM bit in register ADC0CN controls the ADC0 track-and-hold mode. In its default state when Burst Mode is disabled, the ADC0 input is continuously tracked, except when a conversion is in progress. When the AD0TM bit is logic 1, ADC0 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR signal is used to initiate conversions in low-power tracking mode, ADC0 tracks only when CNVSTR is low; conversion begins on the rising edge of CNVSTR (see Figure 5.2). Tracking can also be disabled (shutdown) when the device is in low power standby or sleep modes. Low-power track-and-hold mode is also useful when AMUX settings are frequently changed, due to the settling time requirements described in “5.2.4. Settling Time Requirements” on page 71.



**Figure 5.2. 10-Bit ADC Track and Conversion Example Timing (BURSTEN = 0)**

## 5.2.4. Settling Time Requirements

A minimum amount of tracking time is required before each conversion can be performed, to allow the sampling capacitor voltage to settle. This tracking time is determined by the AMUX0 resistance, the ADC0 sampling capacitance, any external source resistance, and the accuracy required for the conversion. Note that in low-power tracking mode, three SAR clocks are used for tracking at the start of every conversion. For many applications, these three SAR clocks will meet the minimum tracking time requirements, and higher values for the external source impedance will increase the required tracking time.

Figure 5.4 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 5.1. When measuring the Temperature Sensor output or  $V_{DD}$  with respect to GND,  $R_{TOTAL}$  reduces to  $R_{MUX}$ . See Table 4.10 for ADC0 minimum settling time requirements as well as the mux impedance and sampling capacitor values.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

**Equation 5.1. ADC0 Settling Time Requirements**

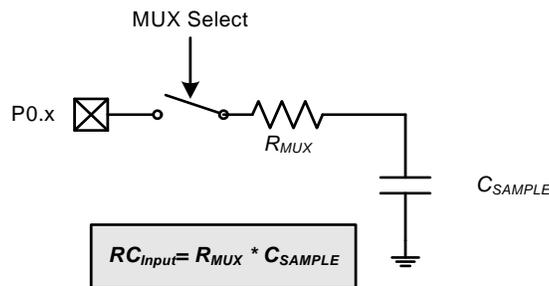
Where:

SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)

$t$  is the required settling time in seconds

$R_{TOTAL}$  is the sum of the AMUX0 resistance and any external source resistance.

$n$  is the ADC resolution in bits (10).



**Note:** The value of  $C_{SAMPLE}$  depends on the PGA Gain. See Table 4.10 for details.

**Figure 5.4. ADC0 Equivalent Input Circuits**

# C8051F99x-C8051F98x

## SFR Definition 8.12. CS0MD2: Capacitive Sense Mode 2

Bit	7	6	5	4	3	2	1	0
Name	CS0CR[1:0]		CS0DT[2:0]			CS0IA[2:0]		
Type	R/W		R/W			R/W		
Reset	0	1	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xF3

Bit	Name	Description
7:6	CS0CR[1:0]	<p><b>CS0 Conversion Rate.</b>            These bits control the conversion rate of the CS0 module. See the electrical specifications table for specific timing.            00: Conversions last 12 internal CS0 clocks and are 12 bits in length.            01: Conversions last 13 internal CS0 clocks and are 13 bits in length.            10: Conversions last 14 internal CS0 clocks and are 14 bits in length.            11: Conversions last 16 internal CS0 clocks and are 16 bits in length.</p>
5:3	CS0DT[2:0]	<p><b>CS0 Discharge Time.</b>            These bits adjust the primary CS0 reset time. For most touch-sensitive switches, the default (fastest) value is sufficient. See the discussion in Section 8.13 for more information.            000: Discharge time is 0.75 <math>\mu</math>s (recommended for most switches)            001: Discharge time is 1.0 <math>\mu</math>s            010: Discharge time is 1.2 <math>\mu</math>s            011: Discharge time is 1.5 <math>\mu</math>s            100: Discharge time is 2 <math>\mu</math>s            101: Discharge time is 3 <math>\mu</math>s            110: Discharge time is 6 <math>\mu</math>s            111: Discharge time is 12 <math>\mu</math>s</p>
2:0	CS0IA[2:0]	<p><b>CS0 Output Current Adjustment.</b>            These bits allow the user to adjust the output current used to charge up the capacitive sensor element. For most touch-sensitive switches, the default (highest) current is sufficient. See the discussion in Section 8.13 for more information.            000: Full Current            001: 1/8 Current            010: 1/4 Current            011: 3/8 Current            100: 1/2 Current            101: 5/8 Current            110: 3/4 Current            111: 7/8 Current</p>

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

## 9.2. Programming and Debugging Support

In-system programming of the Flash program memory and communication with on-chip debug support logic is accomplished via the Silicon Labs 2-Wire Development Interface (C2).

The on-chip debug support logic facilitates full speed in-circuit debugging, allowing the setting of hardware breakpoints, starting, stopping and single stepping through program execution (including interrupt service routines), examination of the program's call stack, and reading/writing the contents of registers and memory. This method of on-chip debugging is completely non-intrusive, requiring no RAM, Stack, timers, or other on-chip resources. C2 details can be found in Section "27. C2 Interface" on page 319.

The CIP-51 is supported by development tools from Silicon Labs and third party vendors. Silicon Labs provides an integrated development environment (IDE) including editor, debugger and programmer. The IDE's debugger and programmer interface to the CIP-51 via the C2 interface to provide fast and efficient in-system device programming and debugging. Third party macro assemblers and C compilers are also available.

## 9.3. Instruction Set

The instruction set of the CIP-51 System Controller is fully compatible with the standard MCS-51™ instruction set. Standard 8051 development tools can be used to develop software for the CIP-51. All CIP-51 instructions are the binary and functional equivalent of their MCS-51™ counterparts, including opcodes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051.

### 9.3.1. Instruction and CPU Timing

In many 8051 implementations, a distinction is made between machine cycles and clock cycles, with machine cycles varying from 2 to 12 clock cycles in length. However, the CIP-51 implementation is based solely on clock cycle timing. All instruction timings are specified in terms of clock cycles.

Due to the pipelined architecture of the CIP-51, most instructions execute in the same number of clock cycles as there are program bytes in the instruction. Conditional branch instructions take one less clock cycle to complete when the branch is not taken as opposed to when the branch is taken. Table 9.1 is the CIP-51 Instruction Set Summary, which includes the mnemonic, number of bytes, and number of clock cycles for each instruction.

# C8051F99x-C8051F98x

## 11. On-Chip XRAM

The C8051F99x-C8051F98x MCUs include on-chip RAM mapped into the external data memory space (XRAM). The external memory space may be accessed using the external move instruction (MOVX) with the target address specified in either the data pointer (DPTR), or with the target address low byte in R0 or R1. On C8051F99x-C8051F98x devices, the target address high byte is a don't care.

When using the MOVX instruction to access on-chip RAM, no additional initialization is required and the MOVX instruction execution time is as specified in the CIP-51 chapter.

**Important Note:** MOVX write operations can be configured to target Flash memory, instead of XRAM. See Section “14. Flash Memory” on page 150 for more details. The MOVX instruction accesses XRAM by default.

**Important Note:** On device reset or upon waking up from Sleep mode, address 0x0000 of external memory may be overwritten by an indeterminate value. The indeterminate value is 0x00 in most situations. A dummy variable should be placed at address 0x0000 in external memory to ensure that the application firmware does not store any data that needs to be retained during sleep or reset at this memory location.

### 11.1. Accessing XRAM

The XRAM memory space is accessed using the MOVX instruction. The MOVX instruction has two forms, both of which use an indirect addressing method. The first method uses the Data Pointer, DPTR, a 16-bit register which contains the effective address of the XRAM location to be read from or written to. The second method uses R0 or R1 to generate the effective XRAM address. Examples of both of these methods are given below.

#### 11.1.1. 16-Bit MOVX Example

The 16-bit form of the MOVX instruction accesses the memory location pointed to by the contents of the DPTR register. The following series of instructions reads the value of the byte at address 0x1234 into the accumulator A:

```
MOV    DPTR, #0034h        ; load DPTR with 16-bit address to read (0x0034)
MOVX   A, @DPTR           ; load contents of 0x0034 into accumulator A
```

The above example uses the 16-bit immediate MOV instruction to set the contents of DPTR. Alternately, the DPTR can be accessed through the SFR registers DPH, which contains the upper 8-bits of DPTR, and DPL, which contains the lower 8-bits of DPTR.

#### 11.1.2. 8-Bit MOVX Example

The 8-bit form of the MOVX instruction uses the contents of R0 or R1 to determine the 8-bits of the effective address to be accessed. The following series of instructions read the contents of the byte at address 0x0034 into the accumulator A.

```
MOV    R0, #34h           ; load low byte of address into R0 (or R1)
MOVX   a, @R0             ; load contents of 0x0034 into accumulator A
```

## SFR Definition 13.7. IT01CF: $\overline{\text{INT0}}/\overline{\text{INT1}}$ Configuration

Bit	7	6	5	4	3	2	1	0
<b>Name</b>	IN1PL	IN1SL[2:0]			IN0PL	IN0SL[2:0]		
<b>Type</b>	R/W	R/W			R/W	R/W		
<b>Reset</b>	0	0	0	0	0	0	0	1

SFR Page = 0x0; SFR Address = 0xE4

Bit	Name	Function
7	IN1PL	<p><b><math>\overline{\text{INT1}}</math> Polarity.</b>                      0: <math>\overline{\text{INT1}}</math> input is active low.                      1: <math>\overline{\text{INT1}}</math> input is active high.</p>
6:4	IN1SL[2:0]	<p><b><math>\overline{\text{INT1}}</math> Port Pin Selection Bits.</b>                      These bits select which Port pin is assigned to <math>\overline{\text{INT1}}</math>. Note that this pin assignment is independent of the Crossbar; <math>\overline{\text{INT1}}</math> will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin.                      000: Select P0.0                      001: Select P0.1                      010: Select P0.2                      011: Select P0.3                      100: Select P0.4                      101: Select P0.5                      110: Select P0.6                      111: Select P0.7</p>
3	IN0PL	<p><b><math>\overline{\text{INT0}}</math> Polarity.</b>                      0: <math>\overline{\text{INT0}}</math> input is active low.                      1: <math>\overline{\text{INT0}}</math> input is active high.</p>
2:0	IN0SL[2:0]	<p><b><math>\overline{\text{INT0}}</math> Port Pin Selection Bits.</b>                      These bits select which Port pin is assigned to <math>\overline{\text{INT0}}</math>. Note that this pin assignment is independent of the Crossbar; <math>\overline{\text{INT0}}</math> will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin.                      000: Select P0.0                      001: Select P0.1                      010: Select P0.2                      011: Select P0.3                      100: Select P0.4                      101: Select P0.5                      110: Select P0.6                      111: Select P0.7</p>

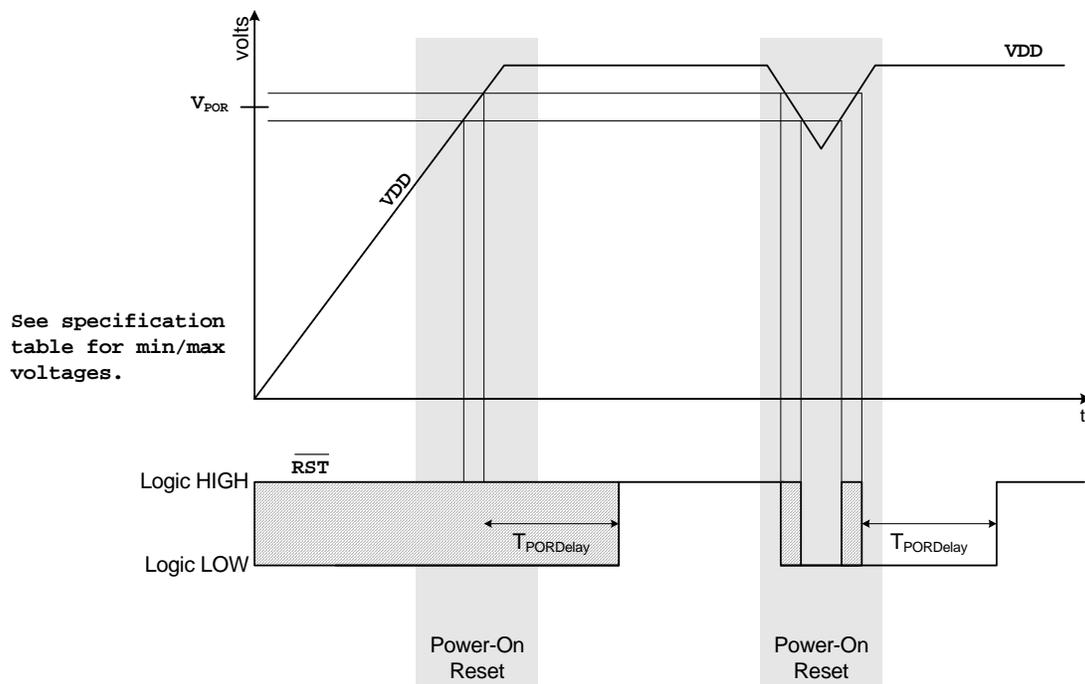
## 18.1. Power-On Reset

During power-up, the device is held in a reset state and the  $\overline{\text{RST}}$  pin voltage tracks  $V_{\text{DD}}$  (through a weak pull-up) until the device is released from reset. After  $V_{\text{DD}}$  settles above  $V_{\text{POR}}$ , a delay occurs before the device is released from reset; the delay decreases as the  $V_{\text{DD}}$  ramp time increases ( $V_{\text{DD}}$  ramp time is defined as how fast  $V_{\text{DD}}$  ramps from 0 V to  $V_{\text{POR}}$ ). Figure 18.2 plots the power-on and  $V_{\text{DD}}$  monitor reset timing. For valid ramp times (less than 3 ms), the power-on reset delay ( $T_{\text{PORDelay}}$ ) is typically 7 ms ( $V_{\text{DD}} = 1.8 \text{ V}$ ) or 15 ms ( $V_{\text{DD}} = 3.6 \text{ V}$ ).

**Note:** The maximum  $V_{\text{DD}}$  ramp time is 3 ms; slower ramp times may cause the device to be released from reset before  $V_{\text{DD}}$  reaches the  $V_{\text{POR}}$  level.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset.

The POR supply monitor can be disabled to save power by writing 1 to the MONDIS (PMU0MD.5) bit. When the POR supply monitor is disabled, all reset sources will trigger a full POR and will re-enable the POR supply monitor.



**Figure 18.2. Power-Fail Reset Timing Diagram**

# C8051F99x-C8051F98x

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## SFR Definition 20.1. RTC0KEY: SmartClock Lock and Key

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Bit	7	6	5	4	3	2	1	0
Name	RTC0ST[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xAE

Bit	Name	Function
7:0	RTC0ST	<b>SmaRTClock Interface Status.</b> Provides lock status when read.  <b>Read:</b> <b>0x02:</b> SmaRTClock Interface is unlocked.  <b>Write:</b> Writes to RTC0KEY have no effect.

## 20.2.2. Using the SmaRTClock Oscillator in Self-Oscillate Mode

When using Self-Oscillate Mode, the XTAL3 and XTAL4 pins are internally shorted together. The following steps show how to configure SmaRTClock for use in Self-Oscillate Mode:

1. Set SmaRTClock to Self-Oscillate Mode (XMODE = 0).
2. Set the desired oscillation frequency:  
For oscillation at about 20 kHz, set BIASX2 = 0.  
For oscillation at about 40 kHz, set BIASX2 = 1.
3. The oscillator starts oscillating instantaneously.
4. Fine tune the oscillation frequency by adjusting the load capacitance (RTC0XCF).

## 20.2.3. Using the Low Frequency Oscillator (LFO)

The low frequency oscillator provides an ultra low power, on-chip clock source to the SmaRTClock. The typical frequency of oscillation is 16.4 kHz  $\pm$ 20%. No external components are required to use the LFO and the XTAL3 and XTAL4 pins do not need to be shorted together.

The following steps show how to configure SmaRTClock for use with the LFO:

1. Enable and select the Low Frequency Oscillator (LFOEN = 1).
2. The LFO starts oscillating instantaneously.

When the LFO is enabled, the SmaRTClock oscillator increments bit 1 of the 32-bit timer (instead of bit 0). This effectively multiplies the LFO frequency by 2, making the RTC timebase behave as if a 32.768 kHz crystal is connected at the output.

# C8051F99x-C8051F98x

## 21. Port Input/Output

Digital and analog resources are available through 16 or 17 I/O pins. Port pins are organized as three byte-wide ports. Port pins P0.0–P1.7 can be defined as digital or analog I/O. Digital I/O pins can be assigned to one of the internal digital resources or used as general purpose I/O (GPIO). Analog I/O pins are used by the internal analog resources. P2.7 can be used as GPIO and is shared with the C2 Interface Data signal (C2D). See Section “27. C2 Interface” on page 319 for more details.

The designer has complete control over which digital and analog functions are assigned to individual Port pins, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. See Section 21.3 for more information on the Crossbar.

All Port I/Os can tolerate voltages up to the supply rail when used as digital inputs or open-drain outputs. For Port I/Os configured as push-pull outputs, current is sourced from the  $V_{DD}$  supply. Port I/Os used for analog functions can operate up to the  $V_{DD}$  supply voltage. See Section 21.1 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications.

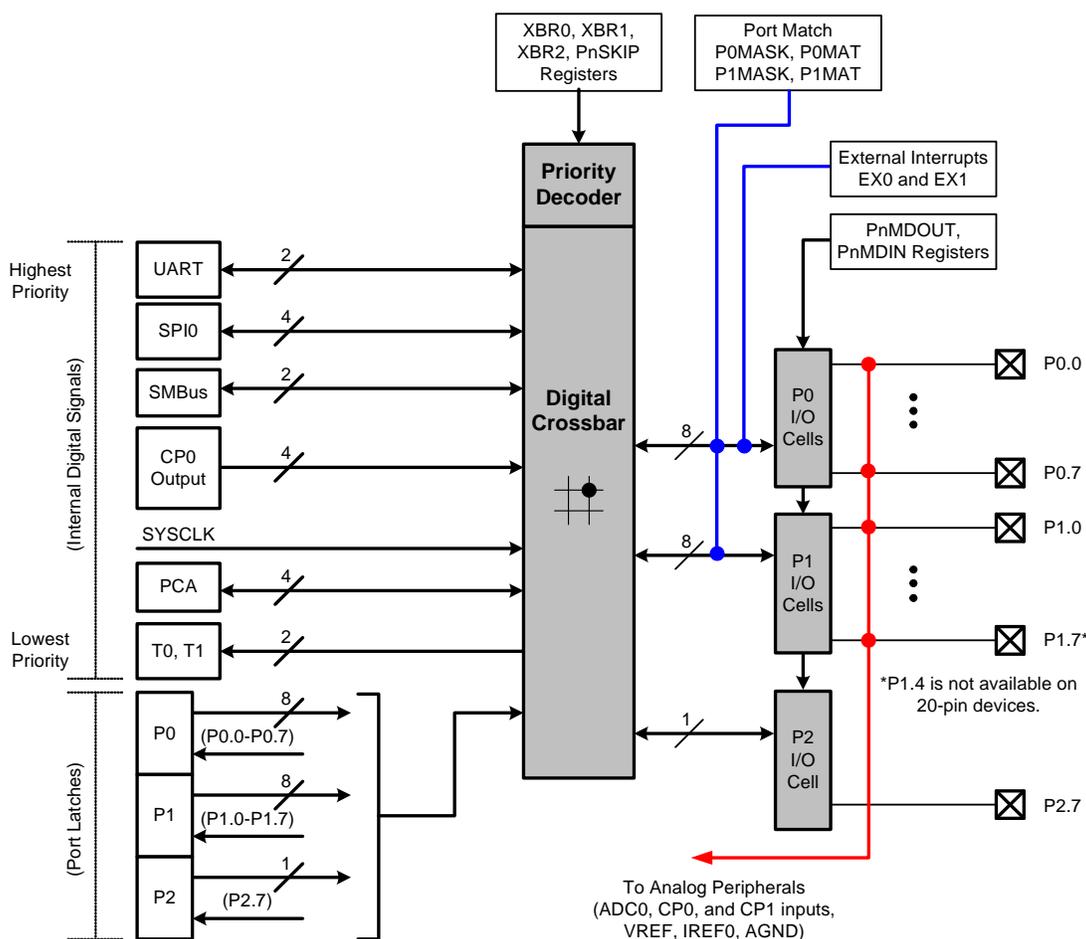


Figure 21.1. Port I/O Functional Block Diagram

# C8051F99x-C8051F98x

## SFR Definition 21.13. P1: Port1

Bit	7	6	5	4	3	2	1	0
Name	P1[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = All; SFR Address = 0x90; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P1[6:0]	<b>Port 1 Data.</b> Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P1.n Port pin is logic LOW. 1: P1.n Port pin is logic HIGH.

## SFR Definition 21.14. P1SKIP: Port1 Skip

Bit	7	6	5	4	3	2	1	0
Name	P1SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xD5

Bit	Name	Function
7:0	P1SKIP[6:0]	<b>Port 1 Crossbar Skip Enable Bits.</b> These bits select Port 1 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P1.n pin is not skipped by the Crossbar. 1: Corresponding P1.n pin is skipped by the Crossbar.

# C8051F99x-C8051F98x

## 23.2. Operational Modes

UART0 provides standard asynchronous, full duplex communication. The UART mode (8-bit or 9-bit) is selected by the S0MODE bit (SCON0.7). Typical UART connection options are shown below.

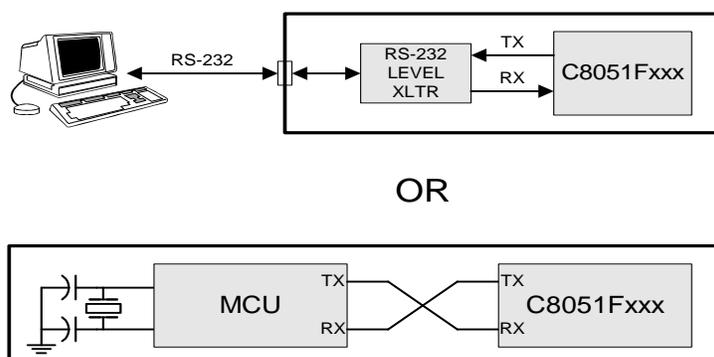


Figure 23.3. UART Interconnect Diagram

### 23.2.1. 8-Bit UART

8-Bit UART mode uses a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when software writes a data byte to the SBUF0 register. The T10 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if MCE0 is logic 1, the stop bit must be logic 1. In the event of a receive data overrun, the first received 8 bits are latched into the SBUF0 receive register and the following overrun data bits are lost.

If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either T10 or RI0 is set.

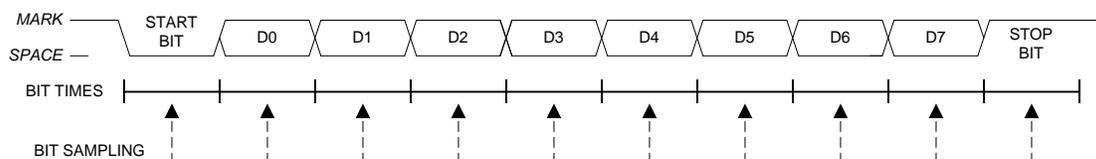


Figure 23.4. 8-Bit UART Timing Diagram

## 23.2.2. 9-Bit UART

9-bit UART mode uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB80 (SCON0.3), which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB80 (SCON0.2) and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TIO Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: (1) RI0 must be logic 0, and (2) if MCE0 is logic 1, the 9th bit must be logic 1 (when MCE0 is logic 0, the state of the ninth data bit is unimportant). If these conditions are met, the eight bits of data are stored in SBUF0, the ninth bit is stored in RB80, and the RI0 flag is set to 1. If the above conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set to 1. A UART0 interrupt will occur if enabled when either TIO or RI0 is set to 1.

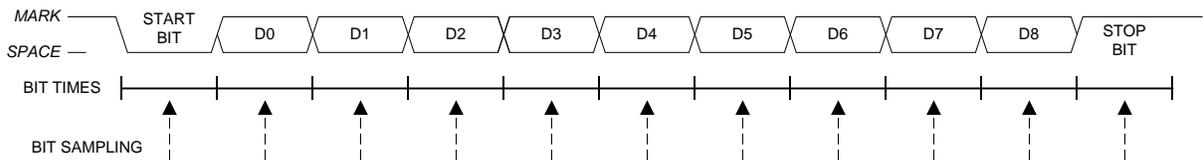


Figure 23.5. 9-Bit UART Timing Diagram

## 23.3. Multiprocessor Communications

9-Bit UART mode supports multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the MCE0 bit (SCON0.5) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic 1 (RB80 = 1) signifying an address byte has been received. In the UART interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its MCE0 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their MCE0 bits set and do not generate interrupts on the reception of the following data bytes, thereby ignoring the data. Once the entire message is received, the addressed slave resets its MCE0 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).

# C8051F99x-C8051F98x

**Table 24.1. SPI Slave Timing Parameters**

Parameter	Description	Min	Max	Units
<b>Master Mode Timing</b> (See Figure 24.8 and Figure 24.9)				
$T_{MCKH}$	SCK High Time	$1 \times T_{SYSCLK}$	—	ns
$T_{MCKL}$	SCK Low Time	$1 \times T_{SYSCLK}$	—	ns
$T_{MIS}$	MISO Valid to SCK Shift Edge	$1 \times T_{SYSCLK} + 20$	—	ns
$T_{MIH}$	SCK Shift Edge to MISO Change	0	—	ns
<b>Slave Mode Timing</b> (See Figure 24.10 and Figure 24.11)				
$T_{SE}$	NSS Falling to First SCK Edge	$2 \times T_{SYSCLK}$	—	ns
$T_{SD}$	Last SCK Edge to NSS Rising	$2 \times T_{SYSCLK}$	—	ns
$T_{SEZ}$	NSS Falling to MISO Valid	—	$4 \times T_{SYSCLK}$	ns
$T_{SDZ}$	NSS Rising to MISO High-Z	—	$4 \times T_{SYSCLK}$	ns
$T_{CKH}$	SCK High Time	$5 \times T_{SYSCLK}$	—	ns
$T_{CKL}$	SCK Low Time	$5 \times T_{SYSCLK}$	—	ns
$T_{SIS}$	MOSI Valid to SCK Sample Edge	$2 \times T_{SYSCLK}$	—	ns
$T_{SIH}$	SCK Sample Edge to MOSI Change	$2 \times T_{SYSCLK}$	—	ns
$T_{SOH}$	SCK Shift Edge to MISO Change	—	$4 \times T_{SYSCLK}$	ns
$T_{SLH}$	Last SCK Edge to MISO Change (CKPHA = 1 ONLY)	$6 \times T_{SYSCLK}$	$8 \times T_{SYSCLK}$	ns
<b>Note:</b> $T_{SYSCLK}$ is equal to one period of the device system clock (SYSCLK).				

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## 25. Timers

Each MCU includes four counter/timers: two are 16-bit counter/timers compatible with those found in the standard 8051, and two are 16-bit auto-reload timer for use with the ADC, SMBus, or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 and Timer 3 offer 16-bit and split 8-bit timer functionality with auto-reload. Additionally, Timer 2 and Timer 3 have a Capture Mode that can be used to measure the SmarTClock or a Comparator period with respect to another oscillator. This is particularly useful when using Capacitive Touch Switches.

Timer 0 and Timer 1 Modes	Timer 2 Modes	Timer 3 Modes
13-bit counter/timer	16-bit timer with auto-reload	16-bit timer with auto-reload
16-bit counter/timer		
8-bit counter/timer with auto-reload	Two 8-bit timers with auto-reload	Two 8-bit timers with auto-reload
Two 8-bit counter/timers (Timer 0 only)		

Timers 0 and 1 may be clocked by one of five sources, determined by the Timer Mode Select bits (T1M–T0M) and the Clock Scale bits (SCA1–SCA0). The Clock Scale bits define a pre-scaled clock from which Timer 0 and/or Timer 1 may be clocked (See SFR Definition 25.1 for pre-scaled clock selection).

Timer 0/1 may then be configured to use this pre-scaled clock signal or the system clock. Timer 2 and Timer 3 may be clocked by the system clock, the system clock divided by 12. Timer 2 may additionally be clocked by the SmarTClock divided by 8 or the Comparator0 output. Timer 3 may additionally be clocked by the external oscillator clock source divided by 8 or the Comparator1 output.

Timer 0 and Timer 1 may also be operated as counters. When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin (T0 or T1). Events with a frequency of up to one-fourth the system clock frequency can be counted. The input signal need not be periodic, but it should be held at a given level for at least two full system clock cycles to ensure the level is properly sampled.

## SFR Definition 25.11. TMR2L: Timer 2 Low Byte

<b>Bit</b>	7	6	5	4	3	2	1	0
<b>Name</b>	TMR2L[7:0]							
<b>Type</b>	R/W							
<b>Reset</b>	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xCC

Bit	Name	Function
7:0	TMR2L[7:0]	<b>Timer 2 Low Byte.</b> In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

## SFR Definition 25.12. TMR2H Timer 2 High Byte

<b>Bit</b>	7	6	5	4	3	2	1	0
<b>Name</b>	TMR2H[7:0]							
<b>Type</b>	R/W							
<b>Reset</b>	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xCD

Bit	Name	Function
7:0	TMR2H[7:0]	<b>Timer 2 High Byte.</b> In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8-bit mode, TMR2H contains the 8-bit high byte timer value.

## 26.3.5.2. 9/10/11-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 9/10/11-bit PWM mode should be varied by writing to an “Auto-Reload” Register, which is dual-mapped into the PCA0CPHn and PCA0CPLn register locations. The data written to define the duty cycle should be right-justified in the registers. The auto-reload registers are accessed (read or written) when the bit ARSEL in PCA0PWM is set to 1. The capture/compare registers are accessed when ARSEL is set to 0.

When the least-significant N bits of the PCA0 counter match the value in the associated module’s capture/compare register (PCA0CPn), the output on CEXn is asserted high. When the counter overflows from the Nth bit, CEXn is asserted low (see Figure 26.9). Upon an overflow from the Nth bit, the COVF flag is set, and the value stored in the module’s auto-reload register is loaded into the capture/compare register. The value of N is determined by the CLSEL bits in register PCA0PWM.

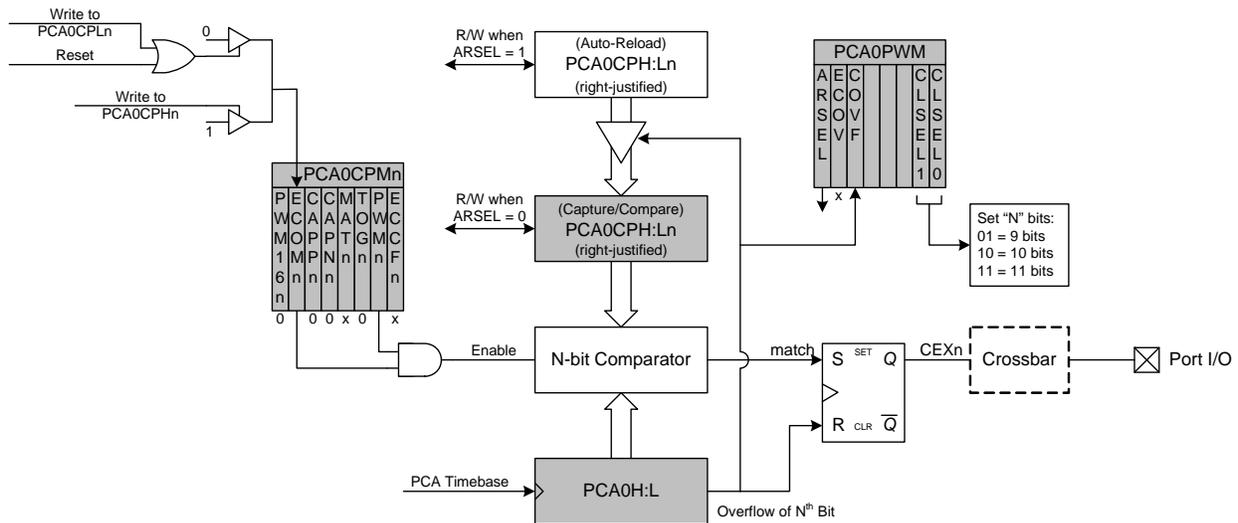
The 9, 10 or 11-bit PWM mode is selected by setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to the desired cycle length (other than 8-bits). If the MATn bit is set to 1, the CCFn flag for the module will be set each time a comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 512 (9-bit), 1024 (10-bit) or 2048 (11-bit) PCA clock cycles. The duty cycle for 9/10/11-Bit PWM Mode is given in Equation 26.2, where N is the number of bits in the PWM cycle.

**Important Note About PCA0CPHn and PCA0CPLn Registers:** When writing a 16-bit value to the PCA0CPn registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(2^N - \text{PCA0CPn})}{2^N}$$

**Equation 26.3. 9, 10, and 11-Bit PWM Duty Cycle**

A 0% duty cycle may be generated by clearing the ECOMn bit to 0.



**Figure 26.9. PCA 9, 10 and 11-Bit PWM Mode Diagram**

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## SFR Definition 26.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	WDTE	WDLCK		CPS2	CPS1	CPS0	ECF
Type	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xD9

Bit	Name	Function
7	CIDL	<b>PCA Counter/Timer Idle Control.</b> Specifies PCA behavior when CPU is in Idle Mode. 0: PCA continues to function normally while the system controller is in Idle Mode. 1: PCA operation is suspended while the system controller is in Idle Mode.
6	WDTE	<b>Watchdog Timer Enable.</b> If this bit is set, PCA Module 2 is used as the watchdog timer. 0: Watchdog Timer disabled. 1: PCA Module 2 enabled as Watchdog Timer.
5	WDLCK	<b>Watchdog Timer Lock.</b> This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset. 0: Watchdog Timer Enable unlocked. 1: Watchdog Timer Enable locked.
4	Unused	Read = 0b, Write = don't care.
3:1	CPS[2:0]	<b>PCA Counter/Timer Pulse Select.</b> These bits select the timebase source for the PCA counter 000: System clock divided by 12 001: System clock divided by 4 010: Timer 0 overflow 011: High-to-low transitions on ECI (max rate = system clock divided by 4) 100: System clock 101: External clock divided by 8 (synchronized with the system clock) 110: SmartClock divided by 8 (synchronized with the system clock) 111: Reserved
0	ECF	<b>PCA Counter/Timer Overflow Interrupt Enable.</b> This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.
<b>Note:</b> When the WDTE bit is set to 1, the other bits in the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.		