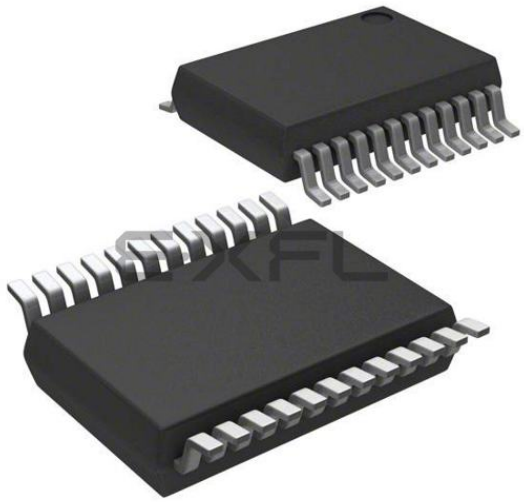


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | CIP-51 8051 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | SMBus (2-Wire/I²C), SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 17 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-SSOP (0.154", 3.90mm Width) |
| Supplier Device Package | 24-QSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/c8051f989-gu |

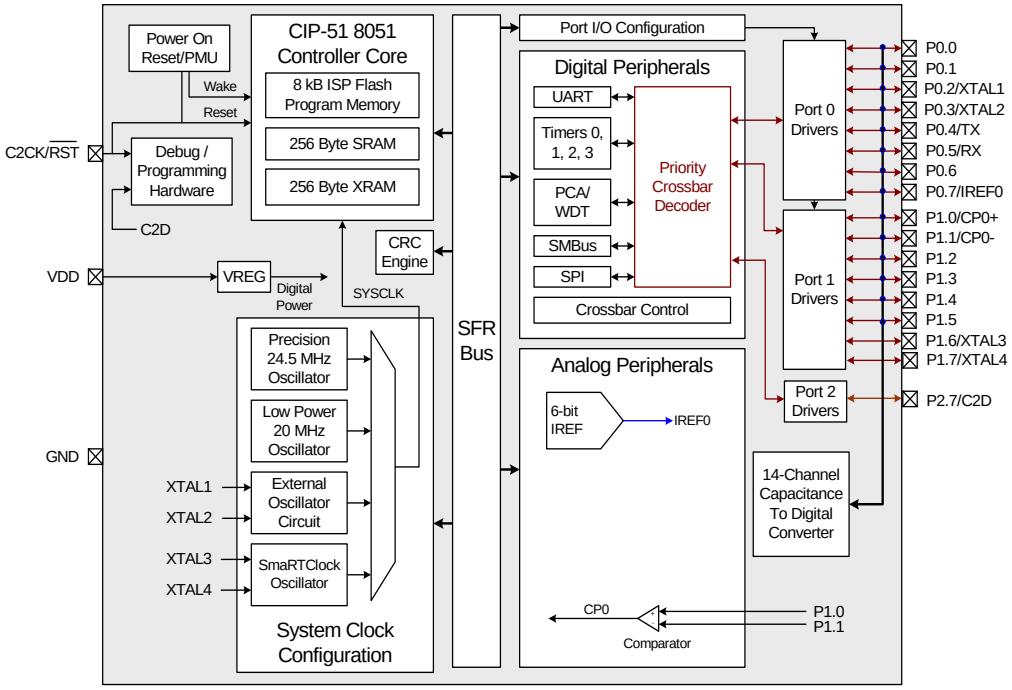



**Figure 1.13. C8051F997 Block Diagram**

## 1.2. Port Input/Output

Digital and analog resources are available through 16 or 17 I/O pins. Port pins are organized as three byte-wide ports. Port pins P0.0–P1.7 can be defined as digital or analog I/O. Digital I/O pins can be assigned to one of the internal digital resources or used as general purpose I/O (GPIO). Analog I/O pins are used by the internal analog resources. P2.7 can be used as GPIO and is shared with the C2 Interface Data signal (C2D). See Section “27. C2 Interface” on page 319 for more details.

The designer has complete control over which digital and analog functions are assigned to individual Port pins, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. See Section “21.3. Priority Crossbar Decoder” on page 219 for more information on the Crossbar.

All Port I/Os can tolerate voltages up to the supply rail when used as digital inputs or open-drain outputs. For Port I/Os configured as push-pull outputs, current is sourced from the VDD supply. Port I/Os used for analog functions can operate up to the VDD supply voltage. See Section “21.1. Port I/O Modes of Operation” on page 216 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications.

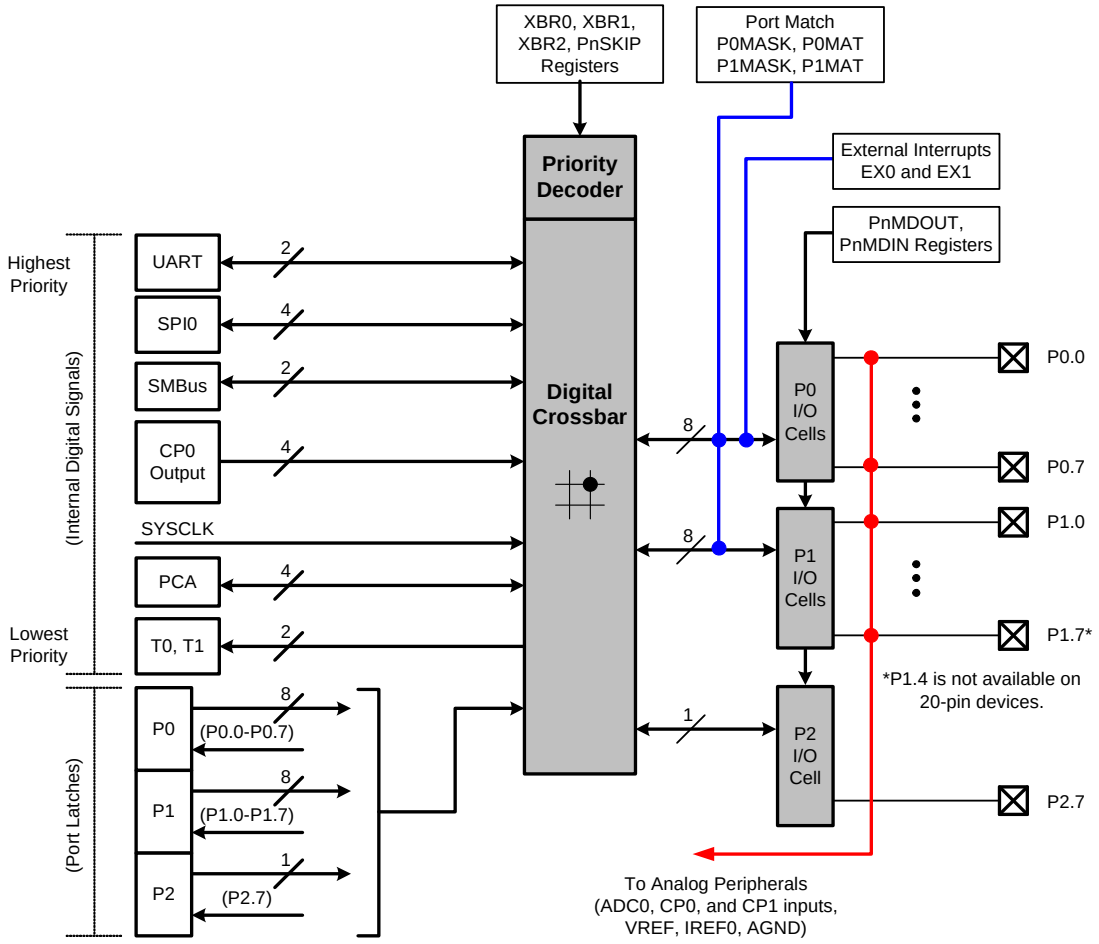



**Figure 1.14. Port I/O Functional Block Diagram**

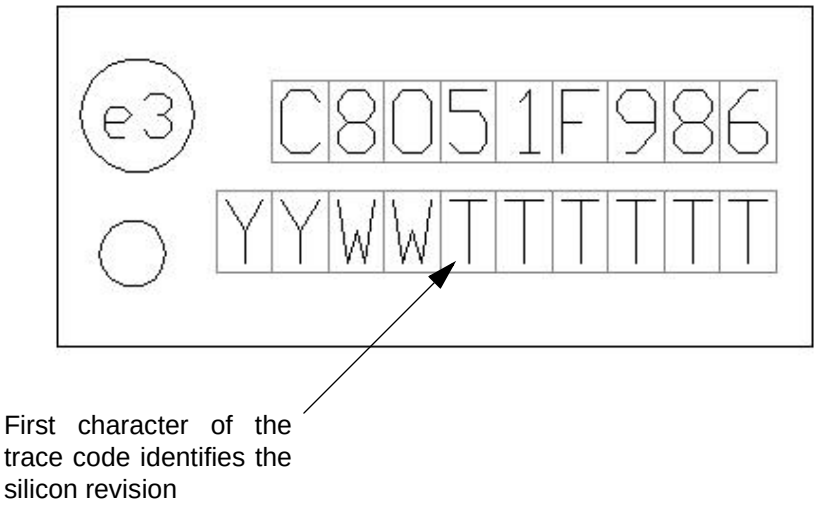



**Figure 3.6. QSOP-24 Package Marking Diagram**

# 4. Electrical Characteristics

Throughout the Electrical Characteristics chapter, “VDD” refers to the Supply Voltage.

## 4.1. Absolute Maximum Specifications

**Table 4.1. Absolute Maximum Ratings**

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Ambient Temperature under Bias | | –55 | — | 125 | °C |
| Storage Temperature | | –65 | — | 150 | °C |
| Voltage on any Port I/O Pin or $\overline{\text{RST}}$ with Respect to GND | | –0.3 | — | $V_{DD}$ + 0.3 | V |
| Voltage on $V_{DD}$ with Respect to GND | | –0.3 | — | 4.0 | V |
| Maximum Total Current through $V_{DD}$ or GND | | — | — | 500 | mA |
| Maximum Current through $\overline{\text{RST}}$ or any Port Pin | | — | — | 100 | mA |
| Maximum Total Current through all Port Pins | | — | — | 200 | mA |

**Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## Table 4.2. Global Electrical Characteristics (Continued)

–40 to +85 °C, 25 MHz system clock unless otherwise specified. See "AN358: Optimizing Low Power Operation of the ‘F9xx" for details on how to achieve the supply current specifications listed in this table.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|

**Notes:**

1. Based on device characterization data; Not production tested.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp $” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the Flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of Flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 64-byte Flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 64-byte address boundaries.
4. Includes oscillator and regulator supply current.
5. IDD can be estimated for frequencies $\leq$ 14 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 84 µA. When using these numbers to estimate $I_{DD}$ for > 14 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD}$ = 3.0 V; F = 20 MHz, $I_{DD}$ = 3.6 mA – (25 MHz – 20 MHz) x 0.088 mA/MHz = 3.16 mA assuming the same oscillator setting.
6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD}$ = 3.0 V; F = 5 MHz, Idle $I_{DD}$ = 1.75 mA – (25 MHz – 5 MHz) x 0.067 mA/MHz = 0.41 mA.

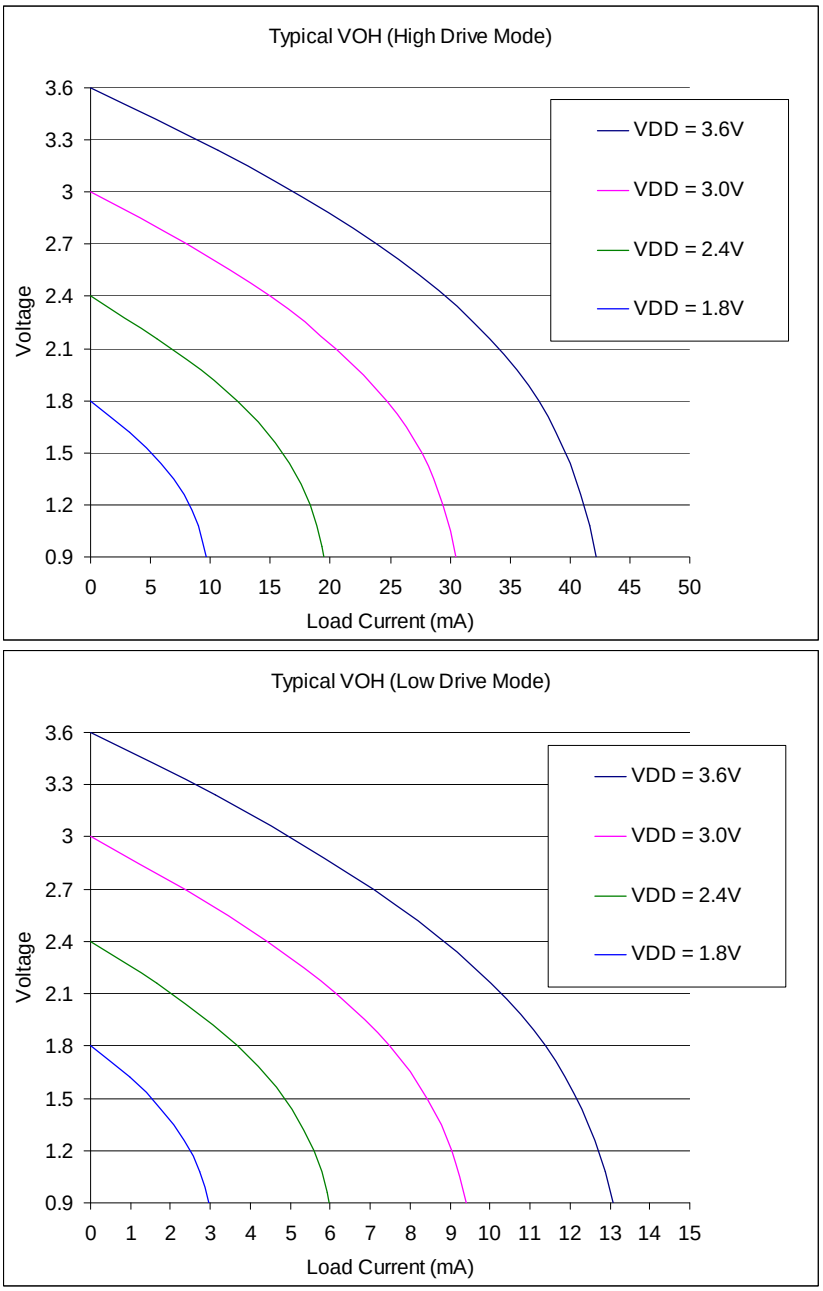



**Figure 4.3. Typical VOH Curves, 1.8–3.6 V**

**Table 4.14. Comparator Electrical Characteristics (Continued)**
$V_{DD}$ = 1.8 to 3.6 V, –40 to +85 °C unless otherwise noted.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Hysteresis** | | | | | |
| Mode 0 | | | | | |
| Hysteresis 1 | (CPnHYP/N1–0 = 00) | — | 0 | — | mV |
| Hysteresis 2 | (CPnHYP/N1–0 = 01) | — | 8.5 | — | mV |
| Hysteresis 3 | (CPnHYP/N1–0 = 10) | — | 17 | — | mV |
| Hysteresis 4 | (CPnHYP/N1–0 = 11) | — | 34 | — | mV |
| Mode 1 | | | | | |
| Hysteresis 1 | (CPnHYP/N1–0 = 00) | — | 0 | — | mV |
| Hysteresis 2 | (CPnHYP/N1–0 = 01) | — | 6.5 | — | mV |
| Hysteresis 3 | (CPnHYP/N1–0 = 10) | — | 13 | — | mV |
| Hysteresis 4 | (CPnHYP/N1–0 = 11) | — | 26 | — | mV |
| Mode 2 | | | | | |
| Hysteresis 1 | (CPnHYP/N1–0 = 00) | — | 0 | 1 | mV |
| Hysteresis 2 | (CPnHYP/N1–0 = 01) | 2 | 5 | 10 | mV |
| Hysteresis 3 | (CPnHYP/N1–0 = 10) | 5 | 10 | 20 | mV |
| Hysteresis 4 | (CPnHYP/N1–0 = 11) | 12 | 20 | 30 | mV |
| Mode 3 | | | | | |
| Hysteresis 1 | (CPnHYP/N1–0 = 00) | — | 0 | — | mV |
| Hysteresis 2 | (CPnHYP/N1–0 = 01) | — | 4.5 | — | mV |
| Hysteresis 3 | (CPnHYP/N1–0 = 10) | — | 9 | — | mV |
| Hysteresis 4 | (CPnHYP/N1–0 = 11) | — | 17 | — | mV |
| ***Note:** Vcm is the common-mode voltage on CP0+ and CP0–. | | | | | |

**Table 4.15. VREG0 Electrical Characteristics**
$V_{DD}$ = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Voltage Range | | 1.8 | — | 3.6 | V |
| Bias Current | Normal, idle, suspend, or stop mode | — | 20 | — | µA |

## SFR Definition 8.1. CS0CN: Capacitive Sense Control

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CS0EN | CS0EOS | CS0INT | CS0BUSY | CS0CMPEN | Reserved | CS0PME | CS0CMPF |
| Type | R/W | R | R/W | R/W | R/W | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0x0; SFR Address = 0xB0

| Bit | Name | Description |
|---|---|---|
| 7 | CS0EN | **CS0 Enable.**<br>0: CS0 disabled and in low-power mode.<br>1: CS0 enabled and ready to convert. |
| 6 | CS0EOS | **CS0 End of Scan Interrupt Flag.**<br>0: CS0 has not completed a scan since the last time CS0EOS was cleared.<br>1: CS0 has completed a scan.<br>This bit is not automatically cleared by hardware. |
| 5 | CS0INT | **CS0 Interrupt Flag.**<br>0: CS0 has not completed a data conversion since the last time CS0INT was cleared.<br>1: CS0 has completed a data conversion.<br>This bit is not automatically cleared by hardware. |
| 4 | CS0BUSY | **CS0 Busy.**<br>Read:<br>0: CS0 conversion is complete or a conversion is not currently in progress.<br>1: CS0 conversion is in progress.<br>Write:<br>0: No effect.<br>1: Initiates CS0 conversion if CS0CM[2:0] = 000b, 110b, or 111b. |
| 3 | CS0CMPEN | **CS0 Digital Comparator Enable Bit.**<br>Enables the digital comparator, which compares accumulated CS0 conversion output to the value stored in CS0THH:CS0THL.<br>0: CS0 digital comparator disabled.<br>1: CS0 digital comparator enabled. |
| 2 | Reserved | Read = Varies. |
| 1 | CS0PME | **CS0 Pin Monitor Event.**<br>Set if any converter re-tries have occurred due to a pin monitor event. This bit remains set until cleared by firmware. |
| 0 | CS0CMPF | **CS0 Digital Comparator Interrupt Flag.**<br>0: CS0 result is smaller than the value set by CS0THH and CS0THL since the last time CS0CMPF was cleared.<br>1: CS0 result is greater than the value set by CS0THH and CS0THL since the last time CS0CMPF was cleared. |

## SFR Definition 14.2. REVID: Revision Identification

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REVID[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0xF; SFR Address = 0xE2

| Bit | Name | Function |
|---|---|---|
| 7:0 | REVID[7:0] | **Revision Identification.**<br>These bits contain a value that can be decoded to determine the silicon revision. For example, 0x00 for Rev A, 0x01 for Rev B, 0x02 for Rev C, etc. |

## 18. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled

All SFRs are reset to the predefined values noted in the SFR descriptions. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. Since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pullups are enabled during and after the reset. For power-on resets, the $\overline{\text{RST}}$ pin is high-impedance with the weak pull-up off until the device exits the reset state. For $V_{DD}$ Monitor resets, the $\overline{\text{RST}}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. Refer to Section “19. Clocking Sources” on page 188 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source (Section “26.4. Watchdog Timer Mode” on page 311 details the use of the Watchdog Timer). Program execution begins at location 0x0000.

**Important Note**: On device reset or upon waking up from Sleep mode, address 0x0000 of external memory may be overwritten by an indeterminate value. The indeterminate value is 0x00 in most situations. A dummy variable should be placed at address 0x0000 in external memory to ensure that the application firmware does not store any data that needs to be retained during sleep or reset at this memory location.

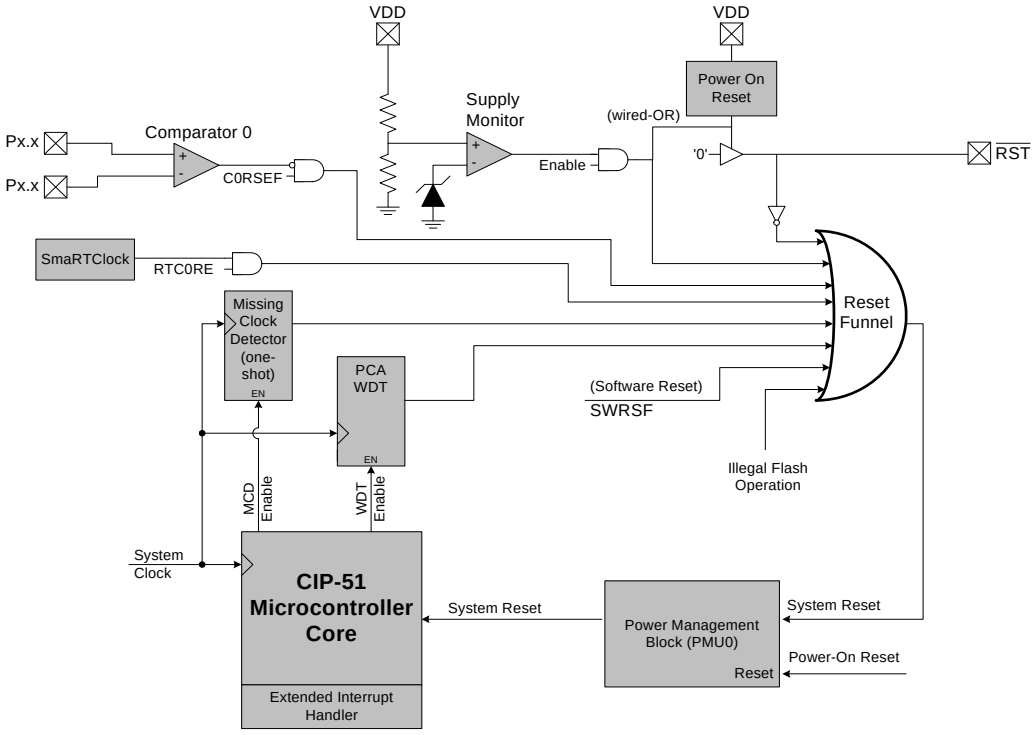



**Figure 18.1. Reset Sources**

## 19. Clocking Sources

C8051F99x-C8051F98x devices include a programmable precision internal oscillator, an external oscillator drive circuit, a low power internal oscillator, and a SmaRTClock real time clock oscillator. The precision internal oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 19.1. The external oscillator can be configured using the OSCXCN register. The low power internal oscillator is automatically enabled and disabled when selected and deselected as a clock source. SmaRTClock operation is described in the SmaRTClock oscillator chapter.

The system clock (SYSCLK) can be derived from the precision internal oscillator, external oscillator, low power internal oscillator, low power internal oscillator divided by 8, or SmaRTClock oscillator. The global clock divider can generate a system clock that is 1, 2, 4, 8, 16, 32, 64, or 128 times slower that the selected input clock source. Oscillator electrical specifications can be found in the Electrical Specifications Chapter.

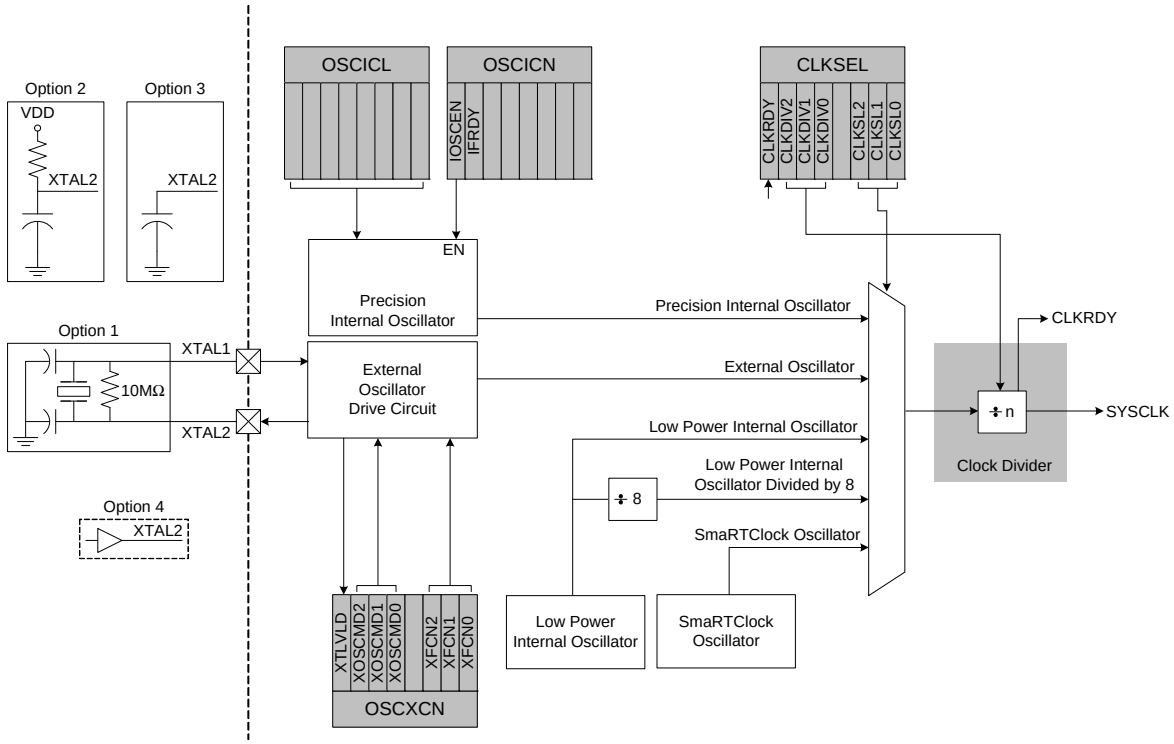



**Figure 19.1. Clocking Sources Block Diagram**

The proper way of changing the system clock when both the clock source and the clock divide value are being changed is as follows:

If switching from a fast “undivided” clock to a slower “undivided” clock:

1. Change the clock divide value.
2. Poll for CLKRDY > 1.
3. Change the clock source.

If switching from a slow “undivided” clock to a faster “undivided” clock:

1. Change the clock source.
2. Change the clock divide value.
3. Poll for CLKRDY > 1.

## 19.1. Programmable Precision Internal Oscillator

All C8051F99x-C8051F98x devices include a programmable precision internal oscillator that may be selected as the system clock. OSCICL is factory calibrated to obtain a 24.5 MHz frequency. See Section “4. Electrical Characteristics” on page 48 for complete oscillator specifications.

The precision oscillator supports a spread spectrum mode which modulates the output frequency in order to reduce the EMI generated by the system. When enabled (SSE = 1), the oscillator output frequency is modulated by a stepped triangle wave whose frequency is equal to the oscillator frequency divided by 384 (63.8 kHz using the factory calibration). The deviation from the nominal oscillator frequency is +0%, –1.6%, and the step size is typically 0.26% of the nominal frequency. When using this mode, the typical average oscillator frequency is lowered from 24.5 MHz to 24.3 MHz.

**Important Note**: The precision internal oscillator may potentially lock up after exiting Sleep mode. Systems using Sleep Mode should switch to the low power oscillator prior to entering Sleep Mode:

1. Switch the system clock to the low power oscillator (CLKSEL = 0x04).
2. Turn off the Precision Oscillator (OSCICN &= ~0x80).
3. Enter Sleep.
4. Exit Sleep.
5. Turn on the Precision Oscillator (OSCICN |= 0x80).
6. Switch the system clock to the Precision Oscillator (CLKSEL = 0x00).

## 19.2. Low Power Internal Oscillator

All C8051F99x-C8051F98x devices include a low power internal oscillator that defaults as the system clock after a system reset. The low power internal oscillator frequency is 20 MHz ± 10% and is automatically enabled when selected as the system clock and disabled when not in use. See Section “4. Electrical Characteristics” on page 48 for complete oscillator specifications.

## 19.3. External Oscillator Drive Circuit

All C8051F99x-C8051F98x devices include an external oscillator circuit that may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. Figure 19.1 shows a block diagram of the four external oscillator options. The external oscillator is enabled and configured using the OSCXCN register.

The external oscillator output may be selected as the system clock or used to clock some of the digital peripherals (e.g., Timers, PCA, etc.). See the data sheet chapters for each digital peripheral for details. See Section “4. Electrical Characteristics” on page 48 for complete oscillator specifications.

### 19.3.1. External Crystal Mode

If a crystal or ceramic resonator is used as the external oscillator, the crystal/resonator and a 10 MΩ resistor must be wired across the XTAL1 and XTAL2 pins as shown in Figure 19.1, Option 1. Appropriate loading capacitors should be added to XTAL1 and XTAL2, and both pins should be configured for analog I/O with the digital output drivers disabled.

Figure 19.2 shows the external oscillator circuit for a 20 MHz quartz crystal with a manufacturer recommended load capacitance of 12.5 pF. Loading capacitors are "in series" as seen by the crystal and "in parallel" with the stray capacitance of the XTAL1 and XTAL2 pins. The total value of the each loading capacitor and the stray capacitance of each XTAL pin should equal 12.5 pF x 2 = 25 pF. With a stray capacitance of 10 pF per pin, the 15 pF capacitors yield an equivalent series capacitance of 12.5 pF across the crystal.

**Note:** The recommended load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal data sheet when completing these calculations.

### 20.1.5. RTC0ADR Autoincrement Feature

For ease of reading and writing the 32-bit CAPTURE and ALARM values, RTC0ADR automatically increments after each read or write to a CAPTUREn or ALARMn register. This speeds up the process of setting an alarm or reading the current SmaRTClock timer value. Autoincrement is always enabled.

Recommended Instruction Timing for a multi-byte register read with short strobe and auto read enabled:

```
mov RTC0ADR, #0d0h
nop
nop
nop
mov A, RTC0DAT
nop
nop
mov A, RTC0DAT
nop
nop
mov A, RTC0DAT
nop
nop
mov A, RTC0DAT
```

Recommended Instruction Timing for a multi-byte register write with short strobe enabled:

```
mov RTC0ADR, #010h
mov RTC0DAT, #05h
nop
mov RTC0DAT, #06h
nop
mov RTC0DAT, #07h
nop
mov RTC0DAT, #08h
nop
```

### 21.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the Crossbar for pin assignment; however, some digital functions bypass the Crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in PnSKIP set to 1.** Table 21.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

**Table 21.2. Port I/O Assignment for Digital Functions**

| Digital Function | Potentially Assignable Port Pins | SFR(s) used for Assignment |
|---|---|---|
| UART0, SPI0, SMBus, CP0 Outputs, System Clock Output, PCA0, Timer0 and Timer1 External Inputs. | Any Port pin available for assignment by the Crossbar. This includes P0.0–P1.7 pins which have their PnSKIP bit set to 0.<br>**Note:** The Crossbar will always assign UART0 and SPI1 pins to fixed locations. | XBR0, XBR1, XBR2 |
| Any pin used for GPIO | P0.0–P1.7, P2.7 | P0SKIP, P1SKIP |

### 21.2.3. Assigning Port I/O Pins to External Digital Event Capture Functions

External digital event capture functions can be used to trigger an interrupt or wake the device from a low power mode when a transition occurs on a digital I/O pin. The digital event capture functions do not require dedicated pins and will function on both GPIO pins (PnSKIP = 1) and pins in use by the Crossbar (PnSKIP = 0). External digital even capture functions cannot be used on pins configured for analog I/O. Table 21.3 shows all available external digital event capture functions.

**Table 21.3. Port I/O Assignment for External Digital Event Capture Functions**

| Digital Function | Potentially Assignable Port Pins | SFR(s) used for Assignment |
|---|---|---|
| External Interrupt 0 | P0.0–P0.7 | IT01CF |
| External Interrupt 1 | P0.0–P0.7 | IT01CF |
| Port Match | P0.0–P1.7 | P0MASK, P0MAT<br>P1MASK, P1MAT |

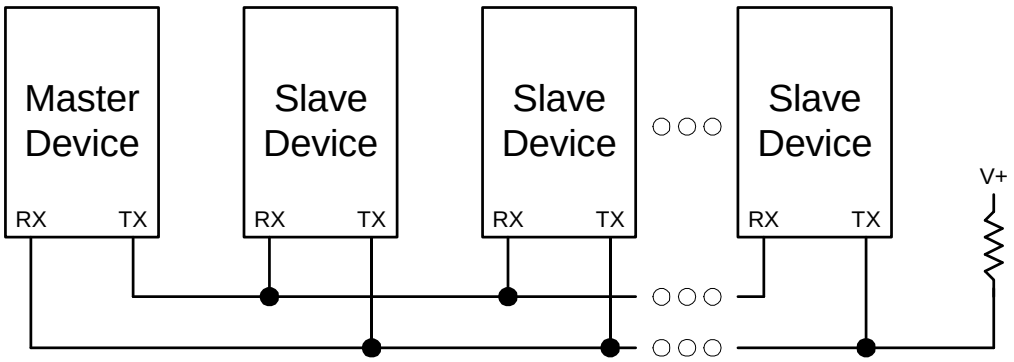



**Figure 23.6. UART Multi-Processor Mode Interconnect Diagram**

## SFR Definition 24.3. SPI0CKR: SPI0 Clock Rate

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SCR[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0x0; SFR Address = 0xA2

| Bit | Name | Function |
|---|---|---|
| 7:0 | SCR[7:0] | **SPI0 Clock Rate.**<br>These bits determine the frequency of the SCK output when the SPI0 module is configured for master mode operation. The SCK clock frequency is a divided version of the system clock, and is given in the following equation, where *SYSCLK* is the system clock frequency and *SPI0CKR* is the 8-bit value held in the SPI0CKR register.<br>$f_{SCK} = \frac{SYSCLK}{2 \times (SPI0CKR[7:0] + 1)}$<br>for 0 <= SPI0CKR <= 255<br><br>Example: If SYSCLK = 2 MHz and SPI0CKR = 0x04,<br>$f_{SCK} = \frac{2000000}{2 \times (4 + 1)}$<br>$f_{SCK} = 200kHz$ |

## SFR Definition 24.4. SPI0DAT: SPI0 Data

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SPI0DAT[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0x0; SFR Address = 0xA3

| Bit | Name | Function |
|---|---|---|
| 7:0 | SPI0DAT[7:0] | **SPI0 Transmit and Receive Data.**<br>The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0DAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer. |

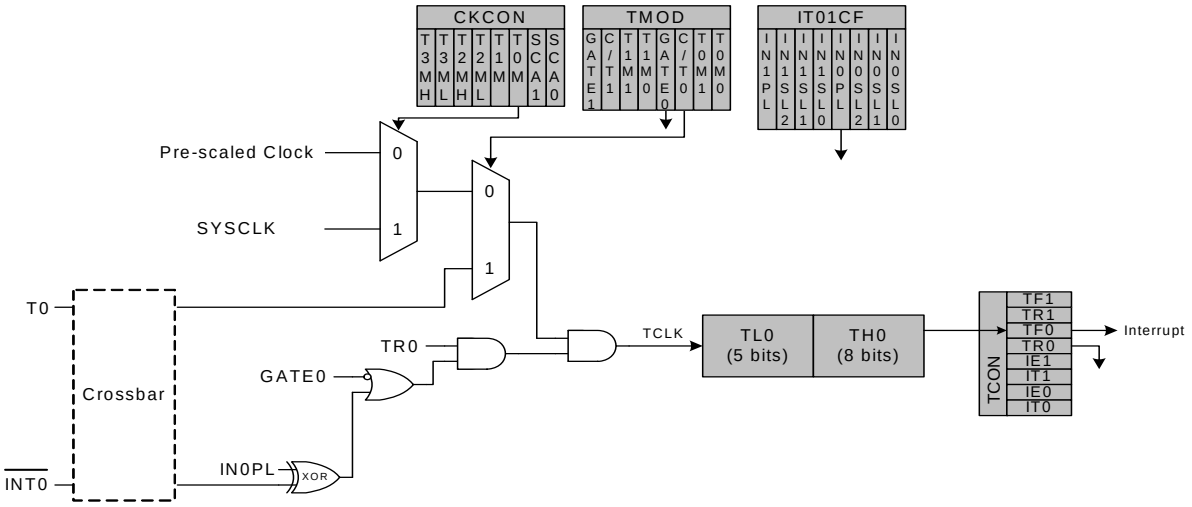



**Figure 25.1. T0 Mode 0 Block Diagram**

### 25.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

## SFR Definition 25.14. TMR3RLL: Timer 3 Reload Register Low Byte

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TMR3RLL[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0x0; SFR Address = 0x92

| Bit | Name | Function |
|---|---|---|
| 7:0 | TMR3RLL[7:0] | **Timer 3 Reload Register Low Byte.**<br>TMR3RLL holds the low byte of the reload value for Timer 3. |

## SFR Definition 25.15. TMR3RLH: Timer 3 Reload Register High Byte

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TMR3RLH[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0x0; SFR Address = 0x93

| Bit | Name | Function |
|---|---|---|
| 7:0 | TMR3RLH[7:0] | **Timer 3 Reload Register High Byte.**<br>TMR3RLH holds the high byte of the reload value for Timer 3. |

#### 26.3.5.1. 8-Bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 8-bit PWM mode is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 26.8). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the module's capture/compare high byte (PCA0CPHn) without software intervention. Setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to 00b enables 8-Bit Pulse Width Modulator mode. If the MATn bit is set to 1, the CCFn flag for the module will be set each time an 8-bit comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 256 PCA clock cycles. The duty cycle for 8-Bit PWM Mode is given in Equation 26.2.

**Important Note About Capture/Compare Registers**: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(256 - PCA0CPHn)}{256}$$

**Equation 26.2. 8-Bit PWM Duty Cycle**

Using Equation 26.2, the largest duty cycle is 100% (PCA0CPHn = 0), and the smallest duty cycle is 0.39% (PCA0CPHn = 0xFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

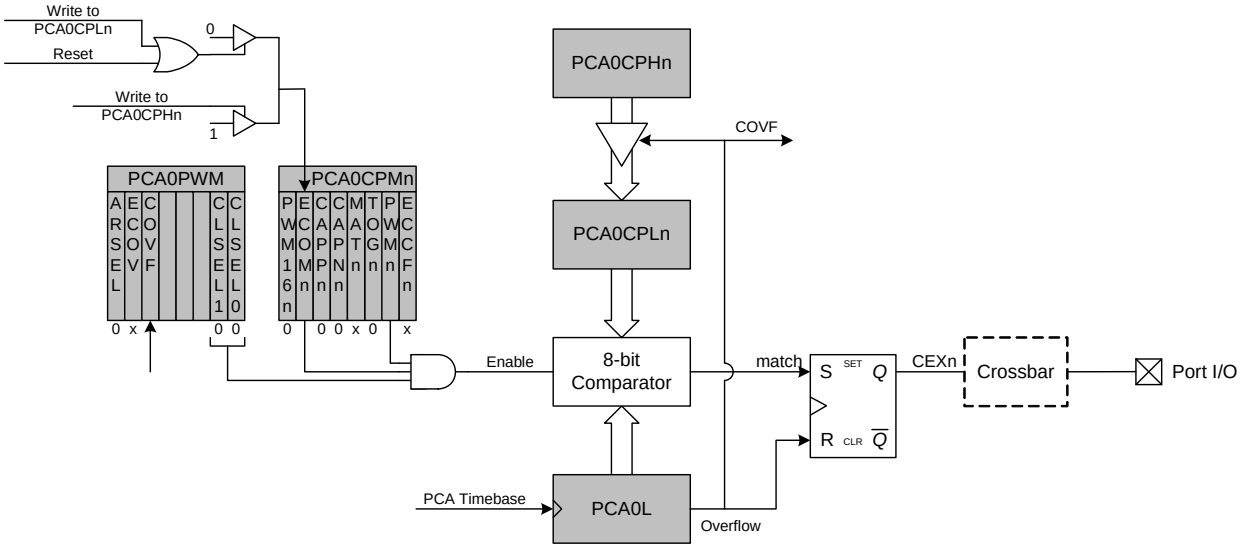
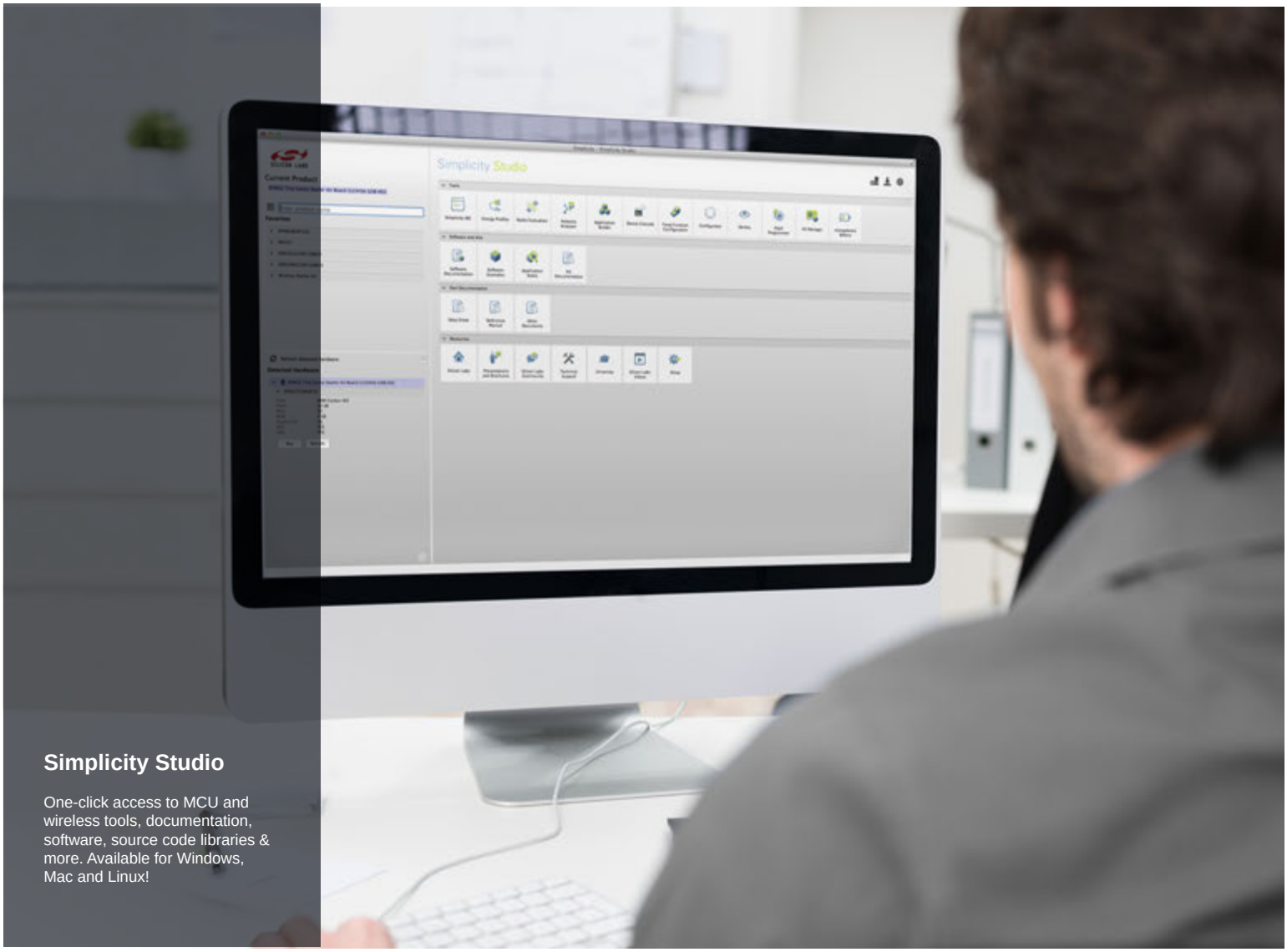



**Figure 26.8. PCA 8-Bit PWM Mode Diagram**




## Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

**IoT Portfolio**
*www.silabs.com/IoT*

**SW/HW**
*www.silabs.com/simplicity*

**Quality**
*www.silabs.com/quality*

**Support and Community**
*community.silabs.com*



SILICON LABS®

**Silicon Laboratories Inc.**
**400 West Cesar Chavez**
**Austin, TX 78701**
**USA**

**http://www.silabs.com**