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What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO
Peripherals	LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-LFSOP (0.173", 4.40mm Width)
Supplier Device Package	24-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87fbk08au-ssop-h

■Interrupts
- 15 sources, 9 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	None
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 128levels (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits   (5 tCYC execution time)
- 24 bits × 16 bits   (12 tCYC execution time)
- 16 bits ÷ 8 bits   (8 tCYC execution time)
- 24 bits ÷ 16 bits   (12 tCYC execution time)

■Oscillation Circuits
- Internal oscillation circuits
  Low-speed RC oscillation circuit (SRC):   For system clock / For Watchdog timer (100kHz)
  Medium-speed RC oscillation circuit (RC):   For system clock (1MHz)
  Frequency variable RC oscillation circuit (MRC):   For system clock (8MHz±2.5%, Ta=-10°C to +85°C)
- External oscillation circuits
  Hi-speed CF oscillation circuit (CF):   For system clock, with internal Rf
  Low speed crystal oscillation circuit (X'tal):   For low-speed system clock / For Watchdog timer,
  with internal Rf
  1) The CF and crystal oscillation circuits share the same pins. The active circuit is selected under program control.
  2) Both the CF and crystal oscillator circuits stop operation on a system reset. After reset is released, oscillation is stopped so start the oscillation operation by program.

■System Clock Divider Function
- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■Internal Reset Function
- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 4 levels (2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use or disuse of the LVD function and the low voltage threshold level (3 levels: 2.81V, 3.79V, 4.28V) can be selected by optional configuration.

■Standby Function
- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are four ways of resetting the HALT mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by low-voltage detection
     (3) System resetting by watchdog timer
     (4) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, low-/medium-/ Frequency variable RC, and crystal oscillators automatically stop operation.
     Note: The oscillation of the low-speed RC oscillator is also controlled directly by the watchdog timer and its standby-mode-time oscillation is also controlled.
  2) There are five ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) System resetting by low-voltage detection
     (3) System resetting by watchdog timer
     (4) Having an interrupt source established at either INT0, INT1, INT2, INT4
        * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (5) Having an interrupt source established at port 0.
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF, low-/medium-/ Frequency variable RC oscillators automatically stop operation.
     Note: The oscillation of the low-speed RC oscillator is also controlled directly by the watchdog timer and its standby-mode-time oscillation is also controlled.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are six ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) System resetting by watchdog timer or low-voltage detection.
     (3) System resetting by watchdog timer or low-voltage detection.
     (4) Having an interrupt source established at either INT0, INT1, INT2, INT4
        * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (5) Having an interrupt source established at port 0.
     (6) Having an interrupt source established in the base timer circuit.
        Note: Available only when X'tal oscillation is selected.

■Onchip Debugger (flash versions only)
- Supports software debugging with the IC mounted on the target board.
- Software break point setting for debugger.
- Stepwise execution on debugger.
- Real time RAM data monitoring function on debugger.
  All the RAM data map can be monitored on screen when the program is running.
  (The RAM & SFR data can be changed by screen patch when the program is running)
- Two channels of on-chip debugger pins are available to be compatible with small pin count devices.
  DBGP0 (P0), DBGP1 (P1)

■Data Security Function (flash versions only)
- Protects the program data stored in flash memory from unauthorized read or copy.
  Note: This data security function does not necessarily provide absolute data security.

■Package Form
- MFP24S (300mil) : Lead-/Halogen-free type (discontinued)
- SSOP24 (225mil) : Lead-/Halogen-free type
- SSOP24 (275mil) : Lead-/Halogen-free type (build-to-order)
- VCT24 (3mm×3mm) : Lead-/Halogen-free type (build-to-order)

■Development Tools
- On-chip-debugger : (1) TCB87 TypeB + LC87FBK08A
                     (2) TCB87 TypeC (3 wire version) + LC87FBK08A

LC87FBK08A

■Flash ROM Programming Boards

Package	Programming boards
MFP24S(300mil)	W87F2GM
SSOP24(225mil)	W87F2GS
SSOP24(275mil)	(build-to-order)
VCT24(3mm×3mm)	(build-to-order)

■Flash ROM Programmer

Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev 03.28 or later	87F008SU
	Gang Programmer	AF9723/AF9723B(Main body) (Including Ando Electric Co., Ltd. models)	-	-
		AF9833(Unit) (Including Ando Electric Co., Ltd. models)	-	-
Flash Support Group, Inc. (FSG) + Our company (Note 1)	In-circuit Programmer	AF9101/AF9103(Main body) (FSG models)	(Note 2)	-
		SIB87(Inter Face Driver) (Our company model)		
Our company	Single/Gang Programmer	SKK / SKK Type B / SKK Type C (SanyoFWS)	Application Version 1.06 or later	LC87FBK08
	In-circuit/Gang Programmer	SKK-DBG Type B / SKK-DBG Type C (SanyoFWS)	Chip Data Version 2.34 or later	

For information about AF-Series:
Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87) together
can give a PC-less, standalone on-board-programming capabilities.
Note2: It needs a special programming devices and applications depending on the use of programming environment.
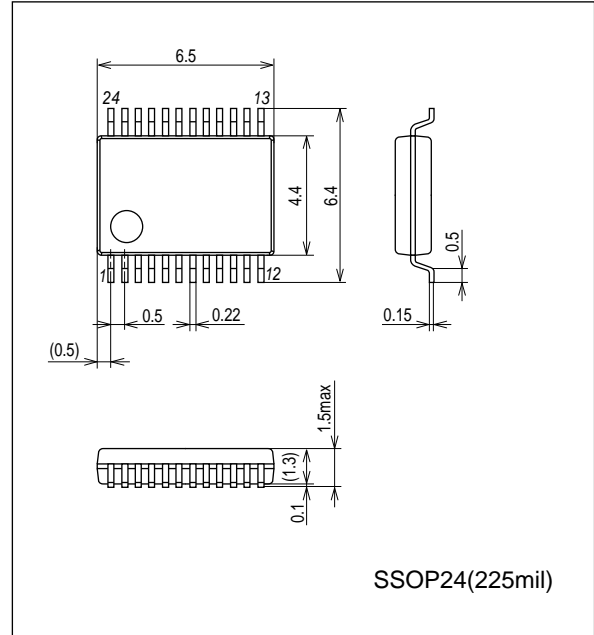Please ask FSG or Our company for the information.
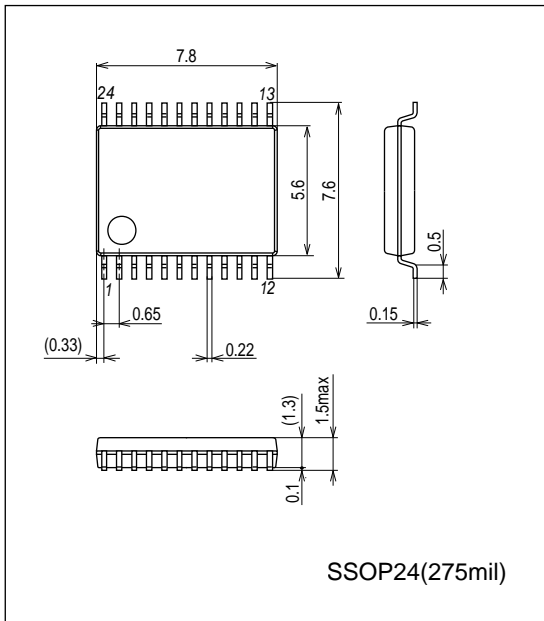
LC87FBK08A

Package Dimensions

unit : mm (typ)
3112B
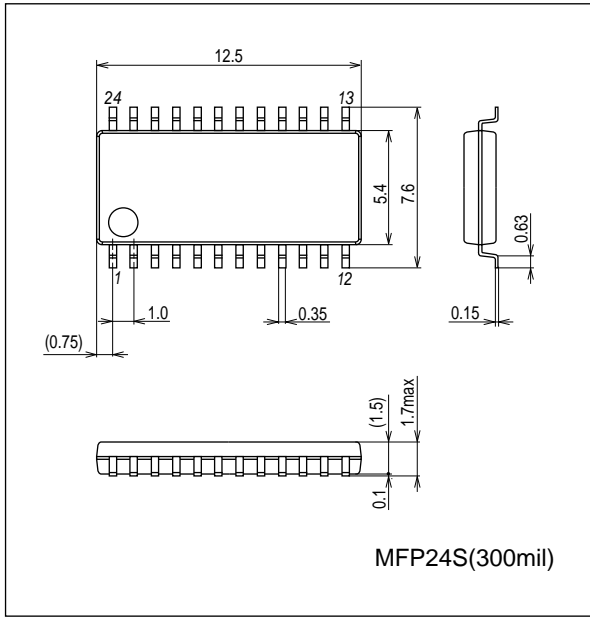
MFP24S(300mil)

Package Dimensions

unit : mm (typ)
3287

SSOP24(225mil)

Package Dimensions

unit : mm (typ)
3175C

SSOP24(275mil)

Package Dimensions

unit : mm (typ)
3366

TOP VIEW   SIDE VIEW   BOTTOM VIEW

SIDE VIEW

VCT24(3.0X3.0)

Pin Assignment

```
P70/INT0/T0LCP/AN8 ──┤ 1        24 ├── P07/T7O/DBGP02
              RES ──┤ 2        23 ├── P06/AN6/T6O/DBGP01
              VSS1 ──┤ 3        22 ├── P05/AN5/CKO/DBGP00
           CF1/XT1 ──┤ 4        21 ├── P04/AN4
           CF2/XT2 ──┤ 5        20 ├── P03/AN3
              VDD1 ──┤ 6    LC87FBK08A    19 ├── P02/AN2
               P10 ──┤ 7        18 ├── P01/AN1
               P11 ──┤ 8        17 ├── P00/AN0
               P12 ──┤ 9        16 ├── P21/INT4/T1IN
     P13/SO1/DBGP12 ──┤ 10       15 ├── P20/INT4/T1IN
 P14/SI1/SB1/DBGP11 ──┤ 11       14 ├── P17/T1PWMH/BUZ/INT1/T0HCP
P15/SCK1/INT3/T0IN/DBGP10 ──┤ 12  13 ├── P16/T1PWML/INT2/T0IN
```
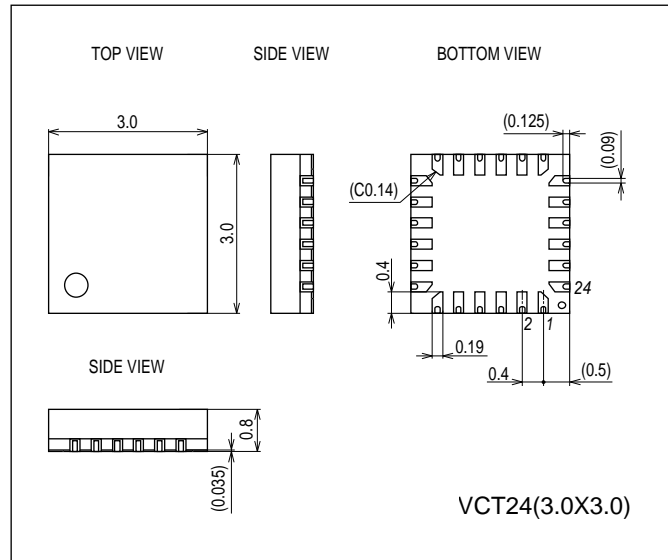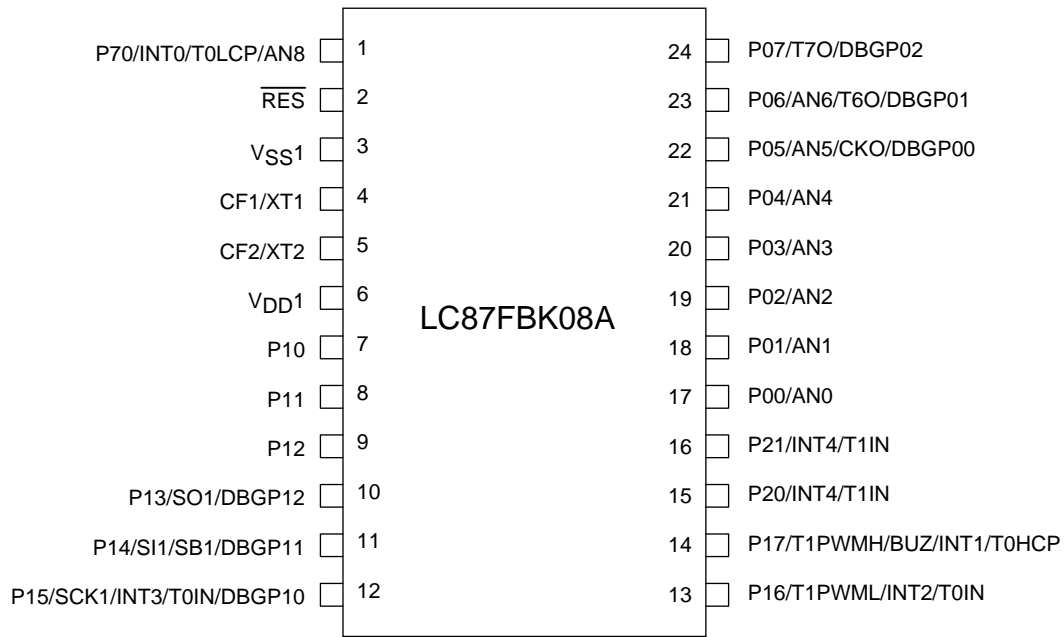
Top view

MFP24S(300mil)/SSOP24(225mil) "Lead-/Halogen-free Type"
SSOP24(275mil) "Lead-/Halogen-free Type"

MFP24S SSOP24	NAME	MFP24S SSOP24	NAME
1	P70/INT0/T0LCP/AN8	13	P16/T1PWML/INT2/T0IN
2	RES	14	P17/T1PWMH/BUZ/INT1/T0HCP
3	$V_{SS}1$	15	P20/INT4/T1IN
4	CF1/XT1	16	P21/INT4/T1IN
5	CF2/XT2	17	P00/AN0
6	$V_{DD}1$	18	P01/AN1
7	P10	19	P02/AN2
8	P11	20	P03/AN3
9	P12	21	P04/AN4
10	P13/SO1/DBGP12	22	P05/AN5/CKO/DBGP00
11	P14/SI1/SB1/DBGP11	23	P06/AN6/T6O/DBGP01
12	P15/SCK1/INT3/T0IN/DBGP10	24	P07/T7O/DBGP02

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Top view
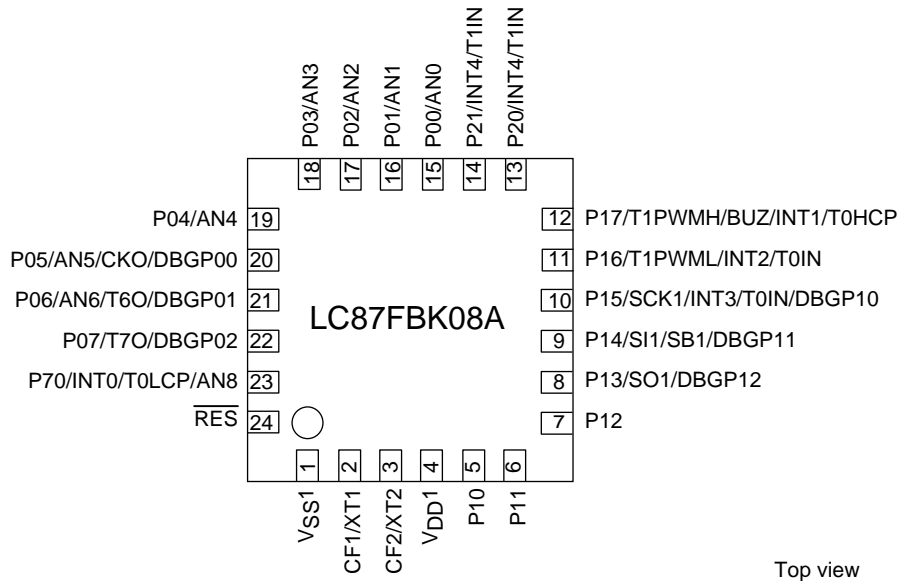
VCT24(3mm×3mm) "Lead-/Halogen-free Type"

VCT24	NAME	VCT24	NAME
1	$V_{SS}1$	13	P20/INT4/T1IN
2	CF1/XT1	14	P21/INT4/T1IN
3	CF2/XT2	15	P00/AN0
4	$V_{DD}1$	16	P01/AN1
5	P10	17	P02/AN2
6	P11	18	P03/AN3
7	P12	19	P04/AN4
8	P13/SO1/DBGP12	20	P05/AN5/CKO/DBGP00
9	P14/SI1/SB1/DBGP11	21	P06/AN6/T6O/DBGP01
10	P15/SCK1/INT3/T0IN/DBGP10	22	P07/T7O/DBGP02
11	P16/T1PWML/INT2/T0IN	23	P70/INT0/T0LCP/AN8
12	P17/T1PWMH/BUZ/INT1/T0HCP	24	$\overline{RES}$

Pin Description

Pin Name	I/O	Description	Option
$V_{SS}1$	-	- Power supply pin	No
$V_{DD}1$	-	+ Power supply pin	No

Port 0
 	
P00 to P07
	I/O	• 8-bit I/O port
		• I/O specifiable in 4-bit units
		• Pull-up resistors can be turned on and off in 4-bit units.
		• HOLD reset input
		• Port 0 interrupt input
		• Pin functions
		  P05: System clock output
		  P06: Timer 6 toggle output
		  P07: Timer 7 toggle output
		  P00(AN0) to P06(AN6): AD converter input
		  P05(DBGP00) to P07(DBGP02): On-chip debugger 0 port
			Yes

Port 1
 	
P10 to P17
	I/O	• 8-bit I/O port
		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1-bit units.
		• Pin functions
		  P13: SIO1 data output
		  P14: SIO1 data input / bus I/O
		  P15: SIO1 clock I/O / INT3 input (with noise filter) / timer 0 event input / timer 0H capture input
		  P16: Timer 1PWML output / INT2 input/HOLD reset input/timer 0 event input / timer 0L capture input
		  P17: Timer 1PWMH output / beeper output / INT1 input / HOLD reset input / timer 0H capture input
		  P15(DBGP10) to P13(DBGP12): On-chip-debugger 1 port
		Interrupt acknowledge type
		
		{INT_TABLE_1}
			Yes

Port 2 P20 to P21	I/O	• 2-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P20 to P21: INT4 input / HOLD reset input / timer 1 event input / timer 0L capture input / timer 0H capture input Interrupt acknowledge types {INT_TABLE_2}	Yes

Port 7
 	
P70
	I/O	• 1-bit I/O port
		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1-bit units.
		• Pin functions
		  P70: INT0 input / HOLD reset input / timer 0L capture input
		  P70(AN8): AD converter input
		Interrupt acknowledge types
		
		{INT_TABLE_3}
			No

INT_TABLE_1:

	Rising	Falling	Rising & Falling	H level	L level
INT1	enable	enable	disable	enable	enable
INT2	enable	enable	enable	disable	disable
INT3	enable	enable	enable	disable	disable

INT_TABLE_2:

	Rising	Falling	Rising & Falling	H level	L level
INT4	enable	enable	enable	disable	disable

INT_TABLE_3:

	Rising	Falling	Rising & Falling	H level	L level
INT0	enable	enable	disable	enable	enable

Continued on next page.

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Pin Name	I/O	Description	Option
$\overline{\text{RES}}$	I/O	External reset input / internal reset output	No
CF1/XT1	I	• Ceramic resonator or 32.768kHz crystal oscillator input pin • Pin function General-purpose input port	No
CF2/XT2	I/O	• Ceramic resonator or 32.768kHz crystal oscillator output pin • Pin function General-purpose I/O port	No

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P21	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
CF2/XT2	-	No	Ceramic resonator/32.768kHz crystal resonator output Nch-open drain (N-channel open drain when set to general-purpose output port)	No

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low-and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

User Option Table

Option Name	Option to be Applied on	Mask version *1	Flash-ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07	○	○	1 bit	CMOS
					Nch-open drain
	P10 to P17	○	○	1 bit	CMOS
					Nch-open drain
	P20 to P21	○	○	1 bit	CMOS
					Nch-open drain
Program start address	-	× *2	○	-	00000h
					01E00h
Low-voltage detection reset function	Detect function	○	○	-	Enable:Use
					Disable:Not Used
	Detect level	○	○	-	3-level
Power-on reset function	Power-On reset level	○	○	-	4-level

*1: Mask option selection - No change possible after mask is completed.

*2: Program start address of the mask version is 00000h.

Recommended Unused Pin Connections

| Port Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P10 to P17	Open	Output low
P20 to P21	Open	Output low
P70	Open	Output low
CF1/XT1	Pulled low with a 100kΩ resistor or less	General-purpose input port
CF2/XT2	Pulled low with a 100kΩ resistor or less	General-purpose input port

On-chip Debugger Pin Connection Requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "RD87 on-chip debugger installation manual".

Power Pin Treatment Recommendations ($V_{DD}1$, $V_{SS}1$)

Connect bypass capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins:

- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and bypass capacitors C1 and C2 with the shortest possible heavy lead wires, making sure that the impedances between the both pins and the bypass capacitors are as possible (L1=L1' , L2=L2').
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel.
  The capacitance of C2 should approximately 0.1μF.
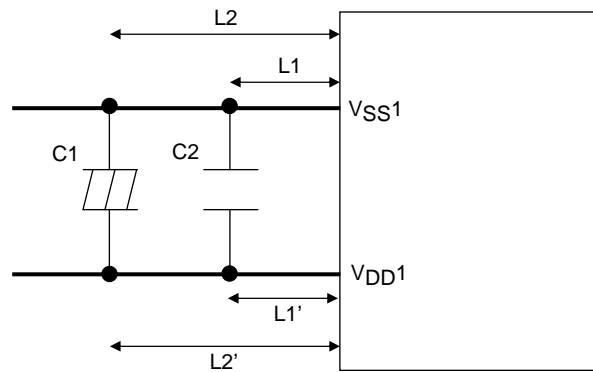
Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Operating supply voltage	V_{DD}	$V_{DD}1$	0.245μs ≤ tCYC ≤ 200μs		2.7		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	RAM and register contents sustained in HOLD mode.		1.6			
High level input voltage	$V_{IH}(1)$	Ports 1, 2, 7		2.7 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}(2)$	Ports 0		2.7 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	V
	$V_{IH}(3)$	CF1, CF2, $\overline{RES}$		2.7 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 7		4.0 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
				2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Ports 0		4.0 to 5.5	V_{SS}		$0.15V_{DD}+0.4$	
				2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	CF1, CF2, $\overline{RES}$		2.7 to 5.5	V_{SS}		$0.25V_{DD}$	
High level output current	$I_{OH}(1)$	Ports 0, 1, 2	Per 1 applicable pin	4.5 to 5.5	-1.0			
	$I_{OH}(2)$			2.7 to 4.5	-0.35			
	$I_{OH}(3)$	P05 (System clock output function used)	Per 1 applicable pin	4.5 to 5.5	-6.0			
	$I_{OH}(4)$			2.7 to 4.5	-1.4			
	$\Sigma I_{OH}(1)$	Ports 0, 1, 2	Total of all applicable pins	4.5 to 5.5	-25			
	$\Sigma I_{OH}(2)$			2.7 to 4.5	-8.0			
Low level output current	$I_{OL}(1)$	Ports 0, 1, 2	Per 1 applicable pin	4.5 to 5.5			7	
	$I_{OL}(2)$			2.7 to 4.5			1	mA
	$I_{OL}(3)$	P70, CF2	Per 1 applicable pin	2.7 to 5.5			1	
	$I_{OL}(4)$	P00, P01	Per 1 applicable pin	4.5 to 5.5			15	
	$I_{OL}(5)$			2.7 to 4.5			2	
	$\Sigma I_{OL}(1)$	Ports 0	Total of all applicable pins	4.5 to 5.5			40	
	$\Sigma I_{OL}(2)$			2.7 to 4.5			10	
	$\Sigma I_{OL}(3)$	Ports 0, 1, 2, CF2	Total of all applicable pins	4.5 to 5.5			70	
	$\Sigma I_{OL}(4)$			2.7 to 4.5			21	
	$\Sigma I_{OL}(5)$	Ports 7	Total of all applicable pins	2.7 to 5.5			1	
Instruction cycle time (Note 2-1)	tCYC			2.7 to 5.5	0.245		200	μs
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	2.7 to 5.5	0.1		12	MHz
			• CF2 pin open • System clock frequency division ratio=1/2 • External system clock duty=50±5%	3.0 to 5.5	0.2		24.4	

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

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Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Oscillation frequency range (Note 2-2)	FmCF(1)	CF1, CF2	12MHz ceramic oscillation. See Fig. 1.	2.7 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	10MHz ceramic oscillation. See Fig. 1.	2.7 to 5.5		10		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation. CF oscillation normal amplifier size selected. (CFLAMP=0) See Fig. 1.	2.7 to 5.5		4		
			4MHz ceramic oscillation. CF oscillation low amplifier size selected. (CFLAMP=1) See Fig. 1.	2.7 to 5.5		4		
	FmMRC(1)		Frequency variable RC oscillation. (Note 2-3)	2.7 to 5.5	7.76	8.0	8.24	
	FmMRC(2)		Frequency variable RC oscillation. • Ta=-10 to +85°C (Note 2-3)	2.7 to 5.5	7.80	8.0	8.20	
	FmRC		Internal medium-speed RC oscillation	2.7 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation	2.7 to 5.5	50	100	200	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 1.	2.7 to 5.5		32.768		
Oscillation stabilization time	tmsMRC		When Frequency variable RC oscillation state is switched from stopped to enabled. See Fig. 3.	2.7 to 5.5			100	μs

Note 2-2: See Tables 1 and 2 for the oscillation constants.

Note 2-3: When switching the system clock, allow an oscillation stabilization time of 100μs or longer after the frequency variable RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

SIO1 Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1$ = 0V (Note 4)

Parameter			Symbol	Pin/ Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 5.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 5.	2.7 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)					1/2		
		High level pulse width	tSCKH(4)					1/2		
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	2.7 to 5.5	(1/3)tCYC +0.01			μs
	Data hold time		thDI(2)				0.01			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 5.	2.7 to 5.5			(1/2)tCYC +0.05	

Note 4: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P17), INT2(P16), INT4(P20 to P21)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P15) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P15) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are nabled.	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P15) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	256			
	tPIL(5)	$\overline{RES}$	• Resetting is enabled.	2.7 to 5.5	200			μs

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AD Converter Characteristics at $V_{SS}1 = 0V$

<12bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
					min	typ	max	unit
Resolution	N	AN0(P00) to AN6(P06), AN8(P70)		2.7 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±16	LSB
				2.7 to 5.5			±20	
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		115	μs
				3.0 to 5.5	64		115	
				2.7 to 5.5	134		215	
Analog input voltage range	VAIN			2.7 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.7 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	2.7 to 5.5	-1			

<8bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
					min	typ	max	unit
Resolution	N	AN0(P00) to AN6(P06), AN8(P70)		2.7 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	2.7 to 5.5			±1.5	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	20		90	μs
				3.0 to 5.5	40		90	
				2.7 to 5.5	80		135	
Analog input voltage range	VAIN			2.7 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.7 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	2.7 to 5.5	-1			

Conversion time calculation formulas:

12bits AD Converter Mode: TCAD(Conversion time) = ((52/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD(Conversion time) = ((32/(AD division ratio))+2)×(1/3)×tCYC

External oscillation (FmCF)	Operating supply voltage range (V_{DD})	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD)	
					12bit AD	8bit AD
CF-12MHz	4.0V to 5.5V	1/1	250ns	1/8	34.8μs	21.5μs
	3.0V to 5.5V	1/1	250ns	1/16	69.5μs	42.8μs
	2.7V to 5.5V	1/1	250ns	1/32	138.8μs	85.5μs
CF-8MHz	4.0V to 5.5V	1/1	375ns	1/8	52.25μs	32.25μs
	3.0V to 5.5V	1/1	375ns	1/16	104.25μs	64.25μs
	2.7V to 5.5V	1/1	375ns	1/32	208.25μs	128.25μs
CF-4MHz	3.0V to 5.5V	1/1	750ns	1/8	104.5μs	64.5μs
	2.7V to 5.5V	1/1	750ns	1/16	208.5μs	128.5μs

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

• The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.

• The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Power-on Reset (POR) Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	min	typ	max	unit
						Specification		
POR release voltage	PORRL		• Select from option. (Note 7-1)	2.57V	2.45	2.57	2.69	V
				2.87V	2.75	2.87	2.99	
				3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	
Detection voltage unknown state	POUKS		• See Fig. 7. (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS		• Power supply rise time from 0V to 1.6V.				100	ms

Note7-1: The POR release level can be selected out of 4 levels only when the LVD reset function is disabled.

Note7-2: POR is in an unknown state before transistors start operation.

Low Voltage Detection Reset (LVD) Characteristics at Ta = -40°C to +85°C, $V_{SS}1=0V$

Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	min	typ	max	unit
						Specification		
LVD reset voltage (Note 8-2)	LVDET		• Select from option. (Note 8-1) (Note 8-3) • See Fig. 8.	2.81V	2.71	2.81	2.91	V
				3.79V	3.67	3.79	3.91	
				4.28V	4.15	4.28	4.41	
LVD hysteresys width	LVHYS			2.81V		60		mV
				3.79V		65		
				4.28V		65		
Detection voltage unknown state	LVUKS		• See Fig. 8. (Note 8-4)			0.7	0.95	V
Low voltage detection minimum width (Reply sensitivity)	TLVDW		• LVDET-0.5V • See Fig. 9.		0.2			ms

Note8-1: The LVD reset level can be selected out of 3 levels only when the LVD reset function is enabled.

Note8-2: LVD reset voltage specification values do not include hysteresis voltage.

Note8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4: LVD is in an unknown state before transistors start operation.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(1)	$V_{DD}1$	• FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		4.8	8.7	
			• Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		3.0	5.0	
	IDDOP(2)		• CF1=24MHz external clock • System clock set to CF1 side • Internal low speed and medium speed RC oscillation stopped.	3.0 to 5.5		5.0	9.6	
			• Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 3.6		3.2	6.0	
	IDDOP(3)		• FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		4.1	7.8	
			• Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		2.6	4.9	
	IDDOP(4)		• FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		2.2	5.1	mA
			• Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		1.5	2.7	
	IDDOP(5)		• CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side	2.7 to 5.5		0.95	2.4	
			• Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio	2.7 to 3.6		0.50	1.1	
	IDDOP(6)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low speed RC oscillation stopped. • System clock set to internal medium speed RC oscillation.	2.7 to 5.5		0.42	1.4	
			• Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.7 to 3.6		0.25	0.76	
	IDDOP(7)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		3.2	5.4	
			• System clock set to 8MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.7 to 3.6		2.3	4.2	
	IDDOP(8)		• External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation.	2.7 to 5.5		55	169	
			• Internal medium speed RC oscillation sopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		39	109	
	IDDOP(9)		• External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation stopped.	5.0		55	136	µA
			• Frequency variable RC oscillation stopped. • 1/1 frequency division ratio • Ta=-10 to +50°C	3.3		39	103	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V$_{DD}$[V]	min	typ	max	unit
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(10)	V$_{DD}$1	• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		28	89	µA
			• Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.7 to 3.6		11	38	
	IDDOP(11)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped.	5.0		28	78	
			• Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C	3.3		11	29	
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(1)		• HALT mode • FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		2.4	4.5	mA
			• Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		1.3	2.2	
	IDDHALT(2)		• HALT mode • CF1=24MHz external clock • System clock set to CF1 side • Internal low speed and medium speed RC oscillation stopped.	3.0 to 5.5		2.7	5.3	
			• Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 3.6		1.6	2.9	
	IDDHALT(3)		• HALT mode • FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		2.0	4.1	
			• Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		1.1	2.1	
	IDDHALT(4)		• HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		1.2	3.3	
			• Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		0.50	1.2	
	IDDHALT(5)		• HALT mode • CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side	2.7 to 5.5		0.70	1.8	
			• Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio	2.7 to 3.6		0.30	0.68	
	IDDHALT(6)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low speed RC oscillation stopped. • System clock set to internal medium speed RC oscillation	2.7 to 5.5		0.30	0.90	
			• Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.7 to 3.6		0.20	0.44	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

Continued from preceding page.

Parameter	Symbol	Pin/ remarks	Conditions	Specification				
				V$_{DD}$[V]	min	typ	max	unit
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(7)	V$_{DD}$1	• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		1.3	2.3	mA
			• System clock set to 8MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.7 to 3.6		0.90	1.5	
	IDDHALT(8)		• HALT mode • External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation.	2.7 to 5.5		18	68	
			• Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		11	35	
	IDDHALT(9)		• HALT mode • External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation.	5.0		18	46	
			• Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio • Ta=-10 to +50°C	3.3		11	27	
	IDDHALT(10)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped.	2.7 to 5.5		20	85	
			• Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.7 to 3.6		5.6	30	
	IDDHALT(11)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped.	5.0		20	51	μA
			• Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C	3.3		5.6	17	
HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(1)		HOLD mode • CF1=V$_{DD}$ or open (External clock mode)	2.7 to 5.5		0.012	23	
				2.7 to 3.6		0.008	11	
	IDDHOLD(2)		HOLD mode • CF1=V$_{DD}$ or open (External clock mode) • Ta=-10 to +50°C	5.0		0.012	1.2	
				3.3		0.008	0.59	
	IDDHOLD(3)		HOLD mode • CF1=V$_{DD}$ or open (External clock mode) • LVD option selected	2.7 to 5.5		2.0	26	
				2.7 to 3.6		1.6	13	
	IDDHOLD(4)		HOLD mode • CF1=V$_{DD}$ or open (External clock mode) • Ta=-10 to +50°C • LVD option selected	5.0		2.0	3.8	
				3.3		1.6	2.8	
Timer HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(5)		Timer HOLD mode • FsX'tal=32.768 kHz crystal oscillation mode	2.7 to 5.5		16	70	
				2.7 to 3.6		4.2	25	
	IDDHOLD(6)		Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode • Ta=-10 to +50°C	5.0		16	42	
				3.3		4.2	11	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

■EPSON TOYOCOM

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [s]	max [s]	
32.768kHz	SMD	MC-306	9	9	Open	330k	2.7 to 5.5	1.4	4.0	Applicable CL value = 7.0pF

■SEIKO INSTRUMENTS

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [s]	max [s]	
32.768kHz	SMD	SSP-T7-F	18	18	Open	0	2.7 to 5.5	0.75	2.0	Applicable CL value = 12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 3).
• The time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed.
• The time interval that is required for the oscillation to get stabilized after the Hold mode, under the state which the subclock oscillation is enabled, is reset and oscillation is started.

(Notes on the implementation of the oscillator circuit)
• Oscillation is influenced by the circuit pattern layout of printed circuit board. Place the oscillation-related components as close to the CPU chip and to each other as possible with the shortest possible pattern length.
• Keep the signal lines whose state changes suddenly or in which large current flows as far away from the oscillator circuit as possible and make sure that they do not cross one another.
• Be sure to insert a current limiting resistor (Rd) so that the oscillation amplitude never exceeds the input voltage level that is specified as the absolute maximum rating.
• The oscillator circuit constants shown above are sample characteristic values that are measured using the Our designated oscillation evaluation board. Since the accuracy of the oscillation frequency and other characteristics vary according to the board on which the IC is installed, it is recommended that the user consult the resonator vendor for oscillation evaluation of the IC on a user's production board when using the IC for applications that require high oscillation accuracy. For further information, contact your resonator vendor or Our company sales representative serving your locality.
• It must be noted, when replacing the flash ROM version of a microcontroller with a mask ROM version, that their operating voltage ranges may differ even when the oscillation constant of the external oscillator is the same.
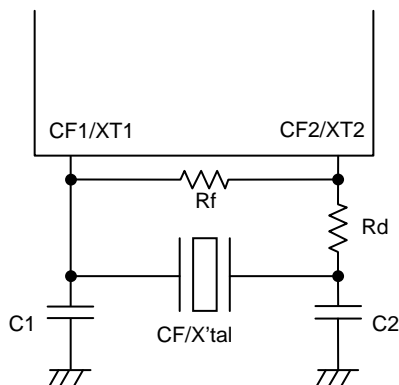

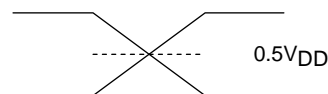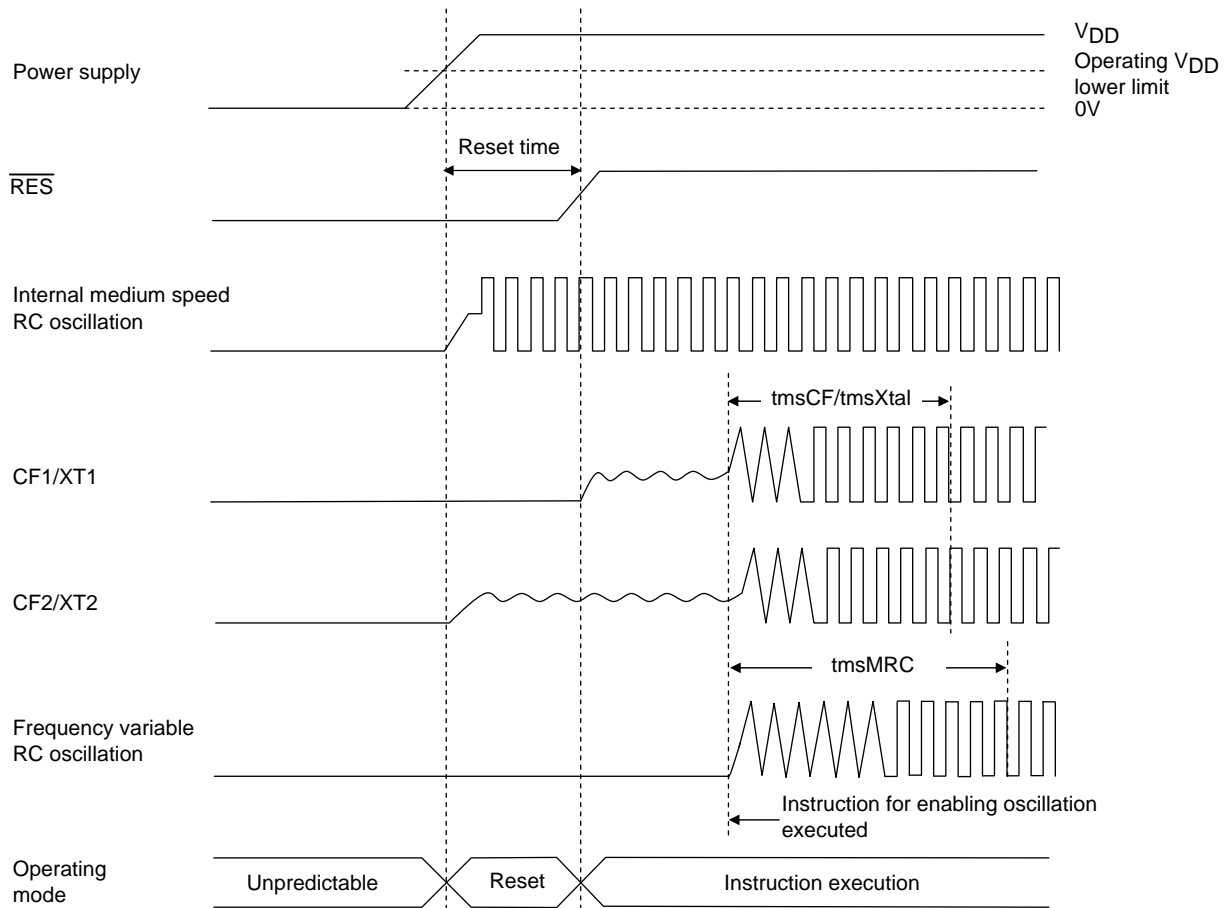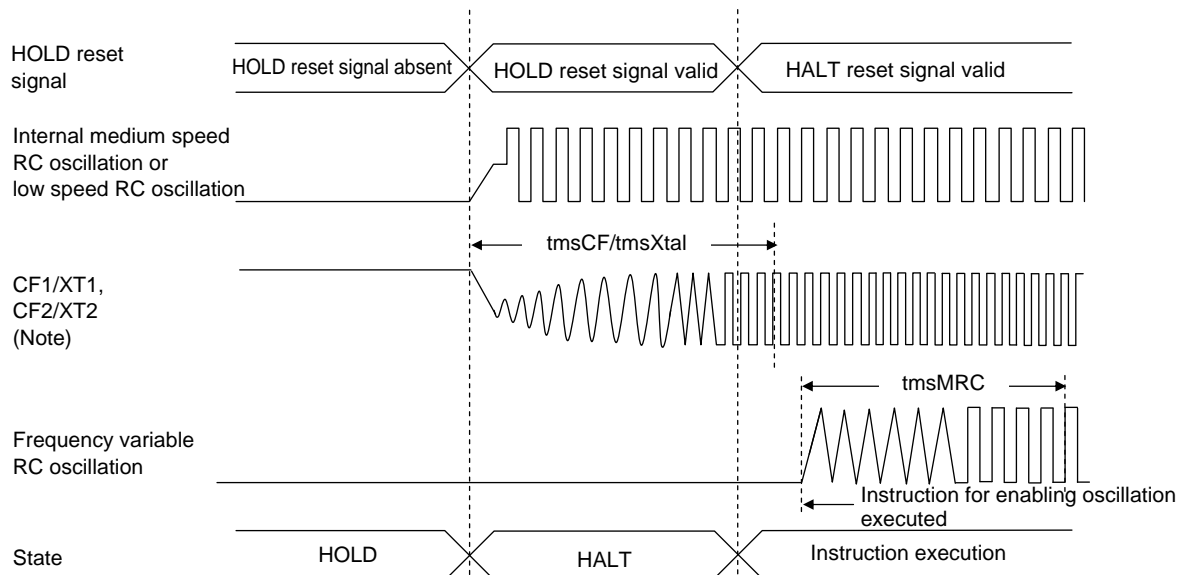Figure 1 CF and XT Oscillator Circuit

Figure 2 AC Timing Measurement Point

Power supply

V_{DD}

Operating V_{DD} lower limit

0V

Reset time

$\overline{RES}$

Internal medium speed RC oscillation

tmsCF/tmsXtal

CF1/XT1

CF2/XT2

tmsMRC

Frequency variable RC oscillation

Instruction for enabling oscillation executed

Operating mode

Unpredictable

Reset

Instruction execution

Reset Time and Oscillation Stabilization Time

HOLD reset signal

HOLD reset signal absent

HOLD reset signal valid

HALT reset signal valid

Internal medium speed RC oscillation or low speed RC oscillation

tmsCF/tmsXtal

CF1/XT1, CF2/XT2 (Note)

tmsMRC

Frequency variable RC oscillation

Instruction for enabling oscillation executed

State

HOLD

HALT

Instruction execution

HOLD Reset Signal and Oscillation Stabilization Time

Note: External oscillation circuit is selected.

Figure 3 Oscillation Stabilization Times
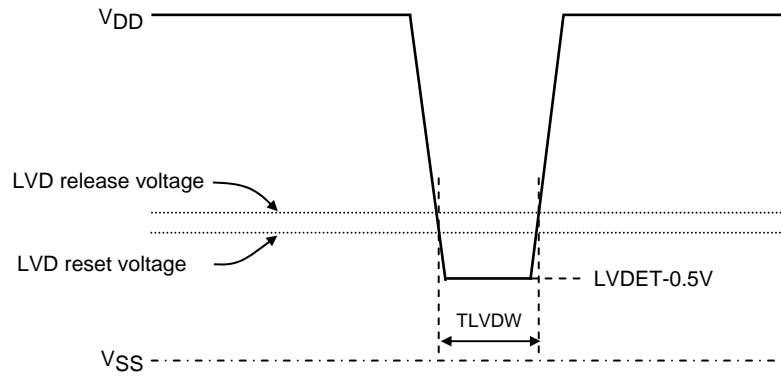
Figure 9 Low voltage detection minimum width
(Example of momentary power loss/Voltage variation waveform)