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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3444axa-116

For more details on the peripherals see the "Example Peripherals" section on page 40 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the "Digital Subsystem" section on page 40 of this data sheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.1-percent error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- Analog-to-digital converter (ADC)
- Digital-to-analog converters (DACs)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features [4]:

- Less than 100 µV offset
- A gain error of 0.2 percent
- INL less than ±2 LSB
- DNL less than ±1 LSB
- SINAD better than 84 dB in 16-bit mode

This converter addresses a wide variety of precision analog applications, including some of the most demanding sensors.

Two high-speed voltage or current DACs support 8-bit output signals at an update rate of up to 8 Msps. They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths. In addition to the ADC, and DACs, the analog subsystem provides multiple:

- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

See the "Analog Subsystem" section on page 51 of this data sheet for more details.

PSoC's 8051 CPU subsystem is built around a single cycle pipelined 8051 8-bit processor running at up to 50 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC's nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable, allowing you to tune active power consumption for specific applications.

PSoC's nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling bootloaders. You can enable an error correcting code (ECC) for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writeable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after POR.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive[5], CapSense[6], flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow V_{OH} to be set independently of Vddio when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with Full-Speed USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All of the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 33 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The internal main oscillator (IMO) is the clock base for the system, and has 1-percent accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 62 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate clock frequencies up to 50 MHz from the IMO, external crystal, or external reference clock.

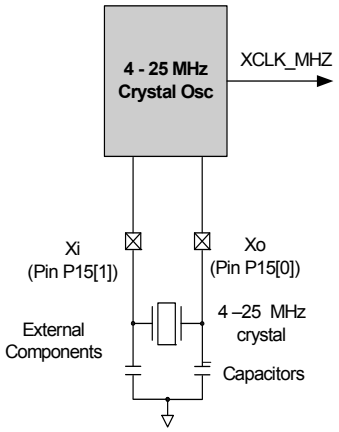
Notes
4. Refer Electrical Specifications on page 65 for the detailed ADC specification across entire voltage range and temperature
5. This feature on select devices only. See Ordering Information on page 133 for details.
6. GPIOs with opamp outputs are not recommended for use with CapSense.

6.1.2 External Oscillators

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports a wide variety of crystal types, in the range of 4 to 25 MHz. When used in conjunction with the PLL, it can generate other clocks up to the device's maximum frequency (see PLL). The GPIO pins connecting to the external crystal and capacitors are fixed. MHzECO accuracy depends on the crystal chosen.

Figure 6-2. MHzECO Block Diagram

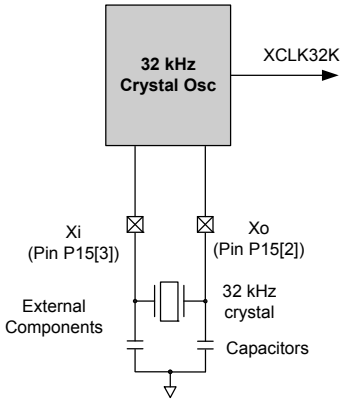


6.1.2.2 32.768-kHz ECO

The 32.768-kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see Figure 6-3). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1-second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the "GPIO" section on page 74.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The master clock is used to select and supply the fastest clock in the system for general clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the master clock to generate the bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADC and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50 percent duty cycle clocks, master clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

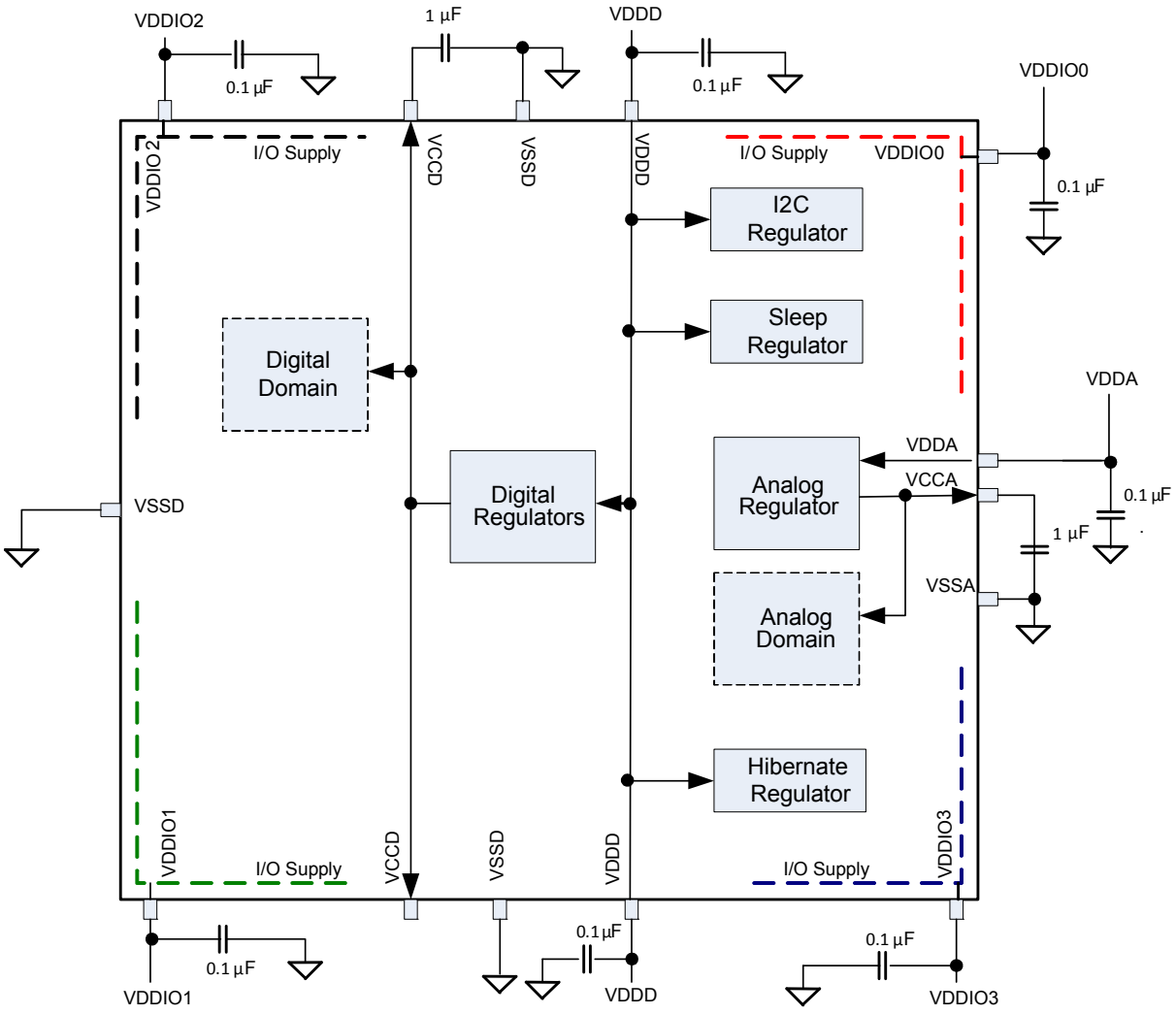
6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOX, respectively. It also includes two internal 1.8-V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in Figure 6-4. The two VCCD pins must be shorted together, with as short a trace as possible, and connected to a 1-µF ±10-percent X5R capacitor. The power system also contains a sleep regulator, an I^2C regulator, and a hibernate regulator.

Figure 6-4. PSoC Power System

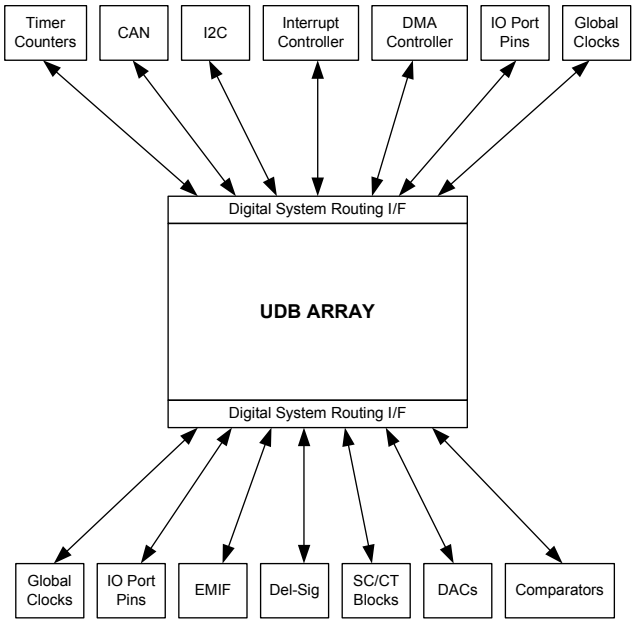


Note The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-6 on page 9.

You can power the device in internally regulated mode, where the voltage applied to the V_{DDx} pins is as high as 5.5 V, and the internal regulators provide the core voltages. **In this mode, do not apply power to the V_{CCx} pins, and do not tie the V_{DDx} pins to the V_{CCx} pins.**

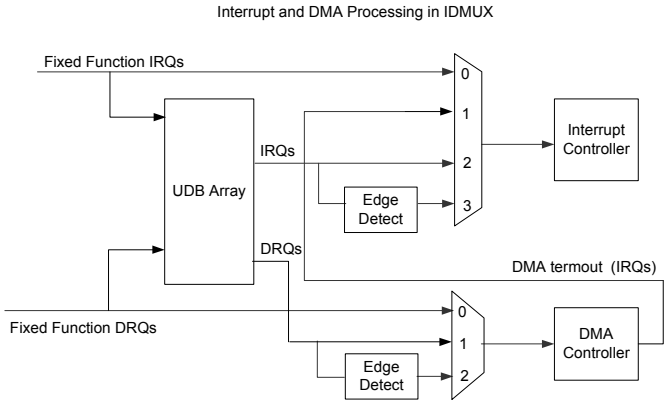
You can also power the device in externally regulated mode, that is, by directly powering the V_{CCD} and V_{CCA} pins. In this configuration, the V_{DDD} pins should be shorted to the V_{CCD} pins and the V_{DDA} pin should be shorted to the V_{CCA} pin. The allowed supply range in this configuration is 1.71 V to 1.89 V. After power up in this configuration, the internal regulators are on by default, and should be disabled to reduce power consumption.

Figure 7-9. Digital System Interconnect



Interrupt and DMA routing is very flexible in the CY8C34 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-10 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-10. Interrupt and DMA Processing in the IDMUX



7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the master clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-11. I/O Pin Synchronization Routing

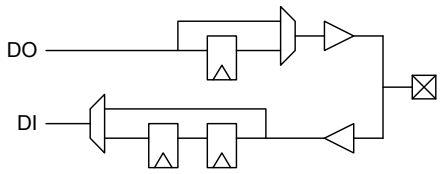
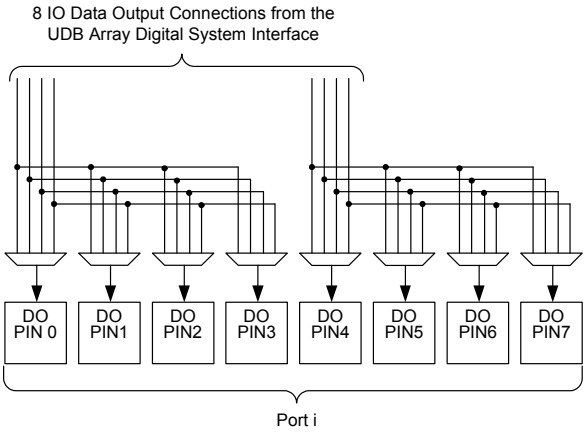
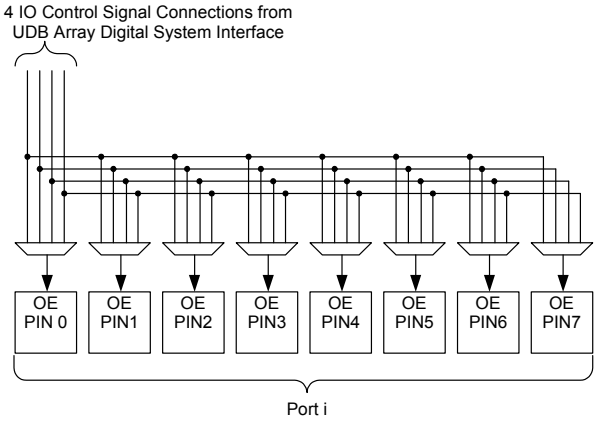


Figure 7-12. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Figure 7-13. I/O Pin Output Enable Connectivity



7.8 I²C

The I²C peripheral provides a synchronous two wire interface designed to interface the PSoC device with a two wire I²C serial communication bus. It is compatible[15] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I2C-bus specification and user manual (UM10204). The I2C bus I/O may be implemented with GPIO or SIO in open-drain modes. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master).[16]. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through DSI routing and allows direct connections to any GPIO or SIO pins.

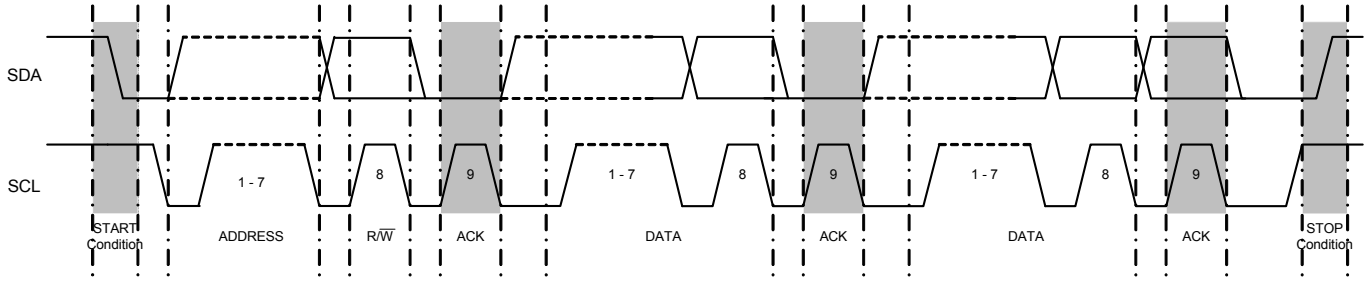
I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup functionality is required, I²C pin connections are limited to the two special sets of SIO pins.

I²C features include:

- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in Figure 7-18. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

Figure 7-18. I²C Complete Transfer Timing



Notes

15. The I²C peripheral is non-compliant with the NXP I²C specification in the following areas: analog glitch filter, I/O V_{OL}/I_{OL}, I/O hysteresis. The I²C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in "Inputs and Outputs" section on page 74 for details.
16. Fixed-block I²C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I²C component should be used instead.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

8.2.2.4 Multi Sample (Turbo)

The multi sample (turbo) mode operates identical to the Multi-sample mode for resolutions of 8 to 16 bits. For resolutions of 17 to 20 bits, the performance is about four times faster than the multi sample mode, because the ADC is only reset once at the end of conversion.

More information on output formats is provided in the Technical Reference Manual.

8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

8.3 Comparators

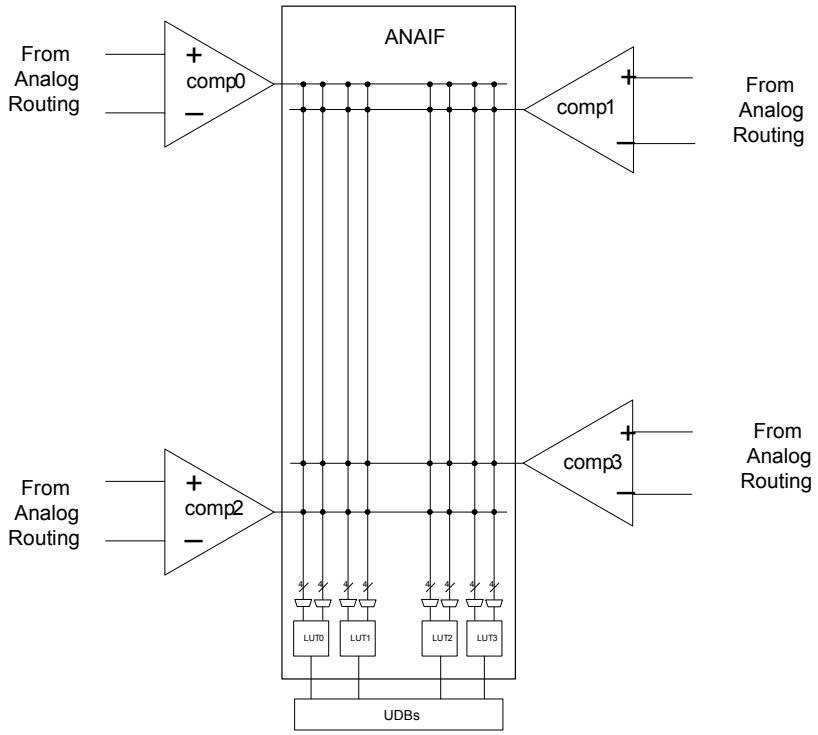
The CY8C34 family of devices contains four comparators in a device. Comparators have these features:

- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (VSSA to VDDA)
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB DSI.

Figure 8-5. Analog Comparator



10. Development Support

The CY8C34 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit psoc.cypress.com/getting-started to find out more.

10.1 Documentation

A suite of documentation, supports the CY8C34 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component data sheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

10.2 Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

10.3 Tools

With industry standard cores, programming, and debugging interfaces, the CY8C34 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 11-25. IDAC (Current Digital-to-Analog Converter) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fdac	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, High speed mode, Vdda = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-37. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, Vdda = 5 V

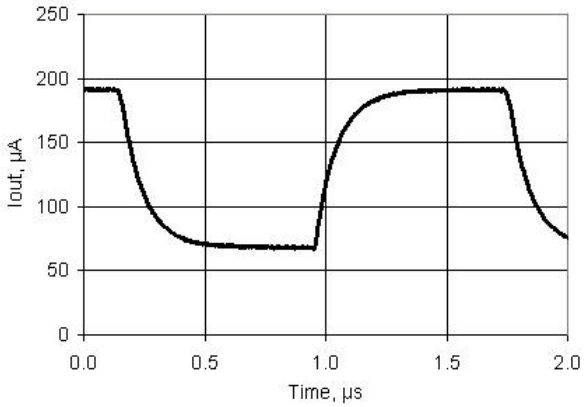


Figure 11-38. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, Vdda = 5 V

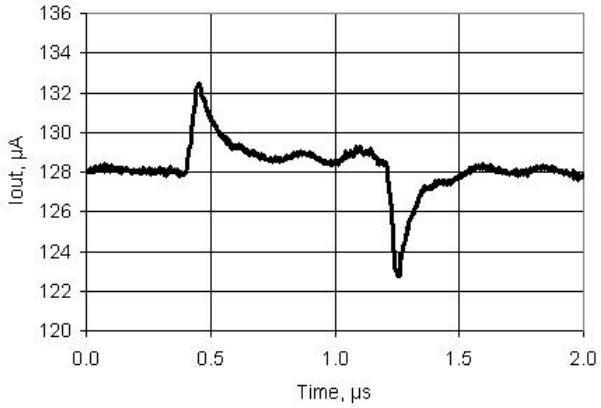


Figure 11-39. IDAC PSRR vs Frequency

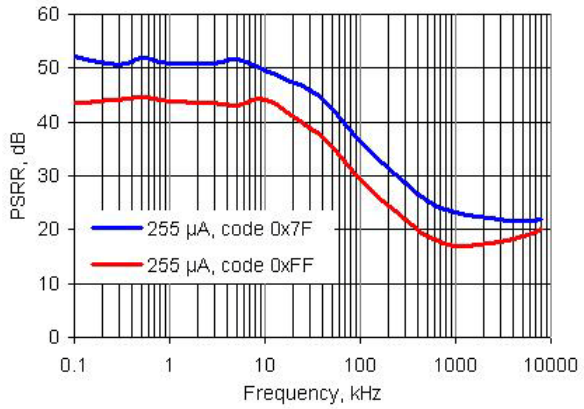


Figure 11-40. IDAC Current Noise, 255 µA Mode, Source Mode, High speed mode, Vdda = 5 V

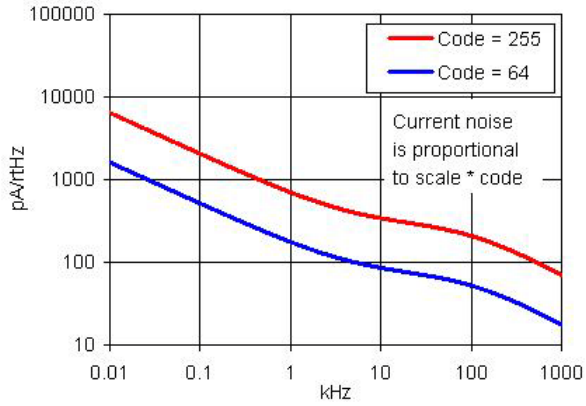


Figure 11-53. PGA Voffset Histogram, 4096 samples / 1024 parts

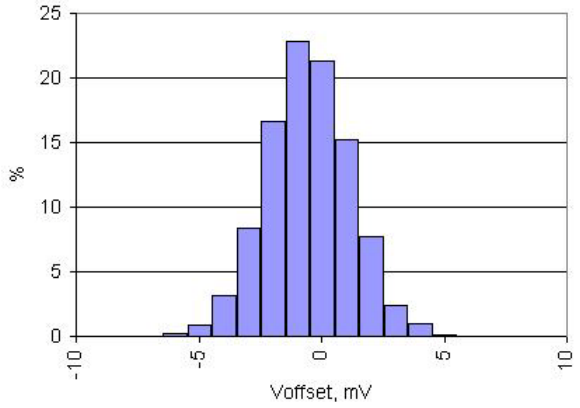
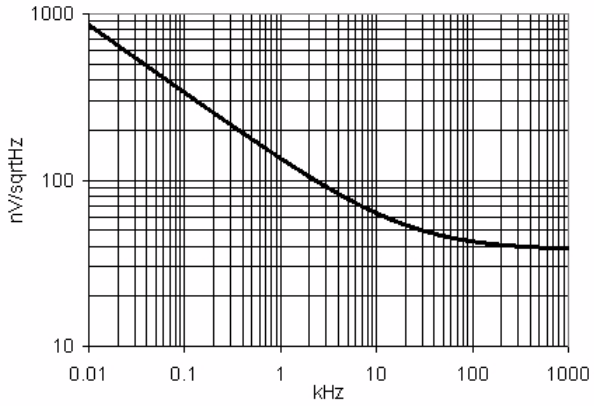


Table 11-33. PGA AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1, input = 100 mV peak-to-peak, Cl = 40 pF	5.5	8	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	–	–	V/µs
e_n	Input noise density	Power mode = high, Vdda = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

Figure 11-54. Noise vs. Frequency, Vdda = 5 V, Power Mode = High



11.5.11 Temperature Sensor

Table 11-34. Temperature Sensor Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Temp sensor accuracy	Range: –40 °C to +150 °C	-	±5	-	°C

11.6 Digital Peripherals

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.6.1 Timer

Table 11-37. Timer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit timer, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	50 MHz		–	260	–	µA

Table 11-38. Timer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	DC	-	50 [45]	MHz
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	DC	-	50	MHz
	Capture pulse width (Internal)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	15	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	21	-	-	ns
	Capture pulse width (external)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	30	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	42	-	-	ns
	Timer resolution	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	15	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	21	-	-	ns
	Enable pulse width	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	15	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	21	-	-	ns
	Enable pulse width (external)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	30	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	42	-	-	ns
	Reset pulse width	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	15	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	21	-	-	ns
	Reset pulse width (external)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	30	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	42	-	-	ns

Note
45. Applicable at -40°C to 85°C; 50 MHz at -40°C to 125°C.

11.6.2 Counter

Table 11-39. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	50 MHz		–	260	–	µA

Table 11-40. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	DC	-	50[46]	MHz
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	DC	-	50	MHz
	Capture pulse	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	15	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	21	-	-	ns
	Resolution	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	15	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	21	-	-	ns
	Pulse width	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	15	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	21	-	-	ns
	Pulse width (external)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	30	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	42	-	-	ns
	Enable pulse width	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	15	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	21	-	-	ns
	Enable pulse width (external)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	30	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	42	-	-	ns
	Reset pulse width	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	15	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	21	-	-	ns
	Reset pulse width (external)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	30	-	-	ns
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	42	-	-	ns

Note
46. Applicable at -40°C to 85°C; 50 MHz at -40°C to 125°C.

11.6.4 I^2C

Table 11-43. Fixed I^2C DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	Enabled, configured for 100 kbps	–	–	250	µA
	–	Enabled, configured for 400 kbps	–	–	260	µA
	–	Wake from sleep mode	–	–	30	µA

Table 11-44. Fixed I^2C AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate		-	-	1	Mbps

11.6.5 Controller Area Network[48]

Table 11-45. CAN DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	500 kbps	-	-	285	µA
		1 Mbps	-	-	330	µA

Table 11-46. CAN AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate	Minimum 8 MHz clock	-	-	1	Mbit

Note
48. Refer to ISO 11898 specification for details.
49. Applicable at -40°C to 85°C; 50 MHz at -40°C to 125°C.

11.7 Memory

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-49. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	Vddd pin	1.71	-	5.5	V

Table 11-50. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Twrite	Block write time (erase + program)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	15	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	15	ms
Terase	Block erase time	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	10	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	10	ms
	Block program time	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	5	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	5	ms
Tbulk	Bulk erase time (16 KB to 64 KB)[51]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	35	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	TBD	ms
	Sector erase time (8 KB to 16 KB)[51]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	15	ms
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 140°C	-	-	15	ms
	Total device program time (including JTAG, etc.)	No overhead [52]	-	-	5	seconds
	Flash data retention time, retention period measured from last erase cycle [53]	Average ambient temp. $T_A \leq 55$ °C, 100 K erase/program cycles	20	–	–	years
		Retention period measured from last erase cycle after 100k progra/erase cycles at $T_A \leq 85$ °C	10	–	–	

Notes
51. ECC not included.
52. See PSoC® 3 Device Programming Specifications for a description of a low-overhead method of programming PSoC 3 flash. (Please take care of Foot note numbers)
53. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +125 °C ambient temperature range. Contact customercare@cypress.com.

11.7.5 External Memory Interface

Figure 11-56. Asynchronous Read Cycle Timing

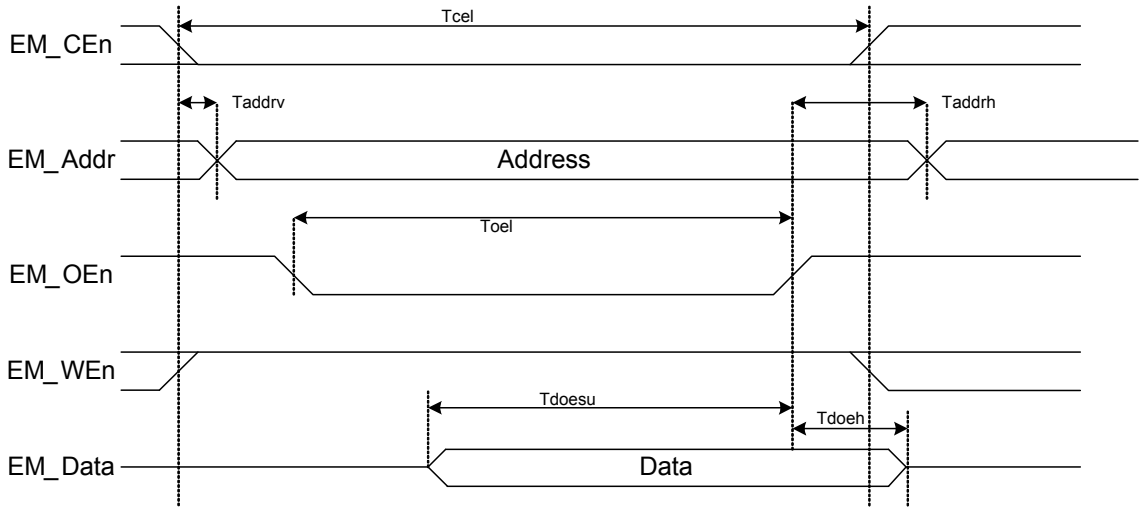


Table 11-57. Asynchronous Read Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock period[54]	Vdda ≥ 3.3 V	30.3	–	–	ns
Tcel	EM_CEn low time		2T – 5	–	2T+ 5	ns
Taddrv	EM_CEn low to EM_Addr valid		–	–	5	ns
Taddrh	Address hold time after EM_Wen high		T	–	–	ns
Toel	EM_OEn low time		2T – 5	–	2T + 5	ns
Tdoesu	Data to EM_OEn high setup time		T + 15	–	–	ns
Tdoeh	Data hold time after EM_OEn high		3	–	–	ns

Note
54. Limited by GPIO output frequency, see .

11.9 Clocking

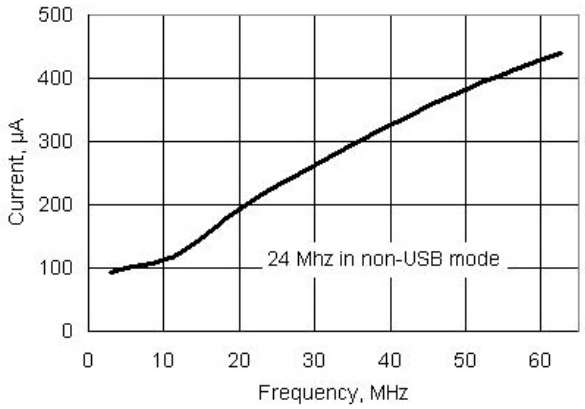
Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.9.1 Internal Main Oscillator

Table 11-69. IMO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	62.6 MHz		–	–	600	µA
	48 MHz		–	–	500	µA
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	µA
	24 MHz – non USB mode		–	–	300	µA
	12 MHz		–	–	200	µA
	6 MHz		–	–	180	µA
	3 MHz		–	–	150	µA

Figure 11-62. IMO Current vs. Frequency



12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C34 device includes: a precision on-chip voltage reference, precision oscillators, Flash, ECC, DMA, a fixed function I^2C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and Analog Subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C34 derivatives incorporate device and Flash security in user-selectable security levels; see TRM for details.

Table 12-1. CY8C34 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[67]				Package	JTAG ID[68]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks	Opamps	DFB	CapSense	UDBs[66]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
16 KB Flash																						
CY8C3444PVE-118	50	16	2	0.5	-	12-bit Del-Sig	2	4	2	2	-	✔	16	4	-	-	29	25	4	0	48-SSOP	0x1E076069
CY8C3444AXA-116	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	-	✔	16	4	-	-	70	62	8	0	100-TQFP	0x1E074069
CY8C3444PVA-100	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	-	✔	16	4	-	-	29	25	4	0	48-SSOP	0x1E064069
32 KB Flash																						
CY8C3445AXE-097	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	-	70	62	8	0	100-TQFP	0x1E061069
CY8C3445AXE-107	50	32	4	1	-	12-bit Del-Sig	2	4	2	2	-	✔	20	4	✔	-	72	62	8	2	100-TQFP	0x1E06B069
CY8C3445AXE-181	50	32	4	1	-	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	✔	70	62	8	0	100-TQFP	0x1E0B5069
CY8C3445AXA-104	50	32	4	1	-	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	-	70	62	8	0	100-TQFP	0x1E068069
CY8C3445AXA-108	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	-	✔	20	4	✔	-	72	62	8	2	100-TQFP	0x1E06C069
CY8C3445AXA-181	50	32	4	1	-	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	✔	70	62	8	0	100-TQFP	0x1E0B5069
CY8C3445PVA-090	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	-	✔	20	4	✔	-	31	25	4	2	48-SSOP	0x1E05A069
CY8C3445PVA-094	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	-	29	25	4	0	48-SSOP	0x1E05E069
64 KB Flash																						
CY8C3446AXE-099	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	✔	-	72	62	8	2	100-TQFP	0x1E063069
CY8C3446AXE-115	50	64	8	2	-	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	-	70	62	8	0	100-TQFP	0x1E073069
CY8C3446PVE-082	50	64	8	2	-	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	-	29	25	4	0	48-SSOP	0x0E052069
CY8C3446PVE-102	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E066069
CY8C3446AXA-099	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	✔	-	72	62	8	2	100-TQFP	0x1E063069
CY8C3446AXA-105	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	-	70	62	8	0	100-TQFP	0x1E069069
CY8C3446PVA-076	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	✔	-	31	25	4	2	48-SSOP	0x1E04C069
CY8C3446PVA-091	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	-	29	25	4	0	48-SSOP	0x1E05B069
CY8C3446PVA-102	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E066069

Notes

66. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the "Example Peripherals" section on page 40 for more information on how UDBs may be used.
67. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the ""I/O System and Routing" section on page 33" for details on the functionality of each of these types of I/O.
68. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

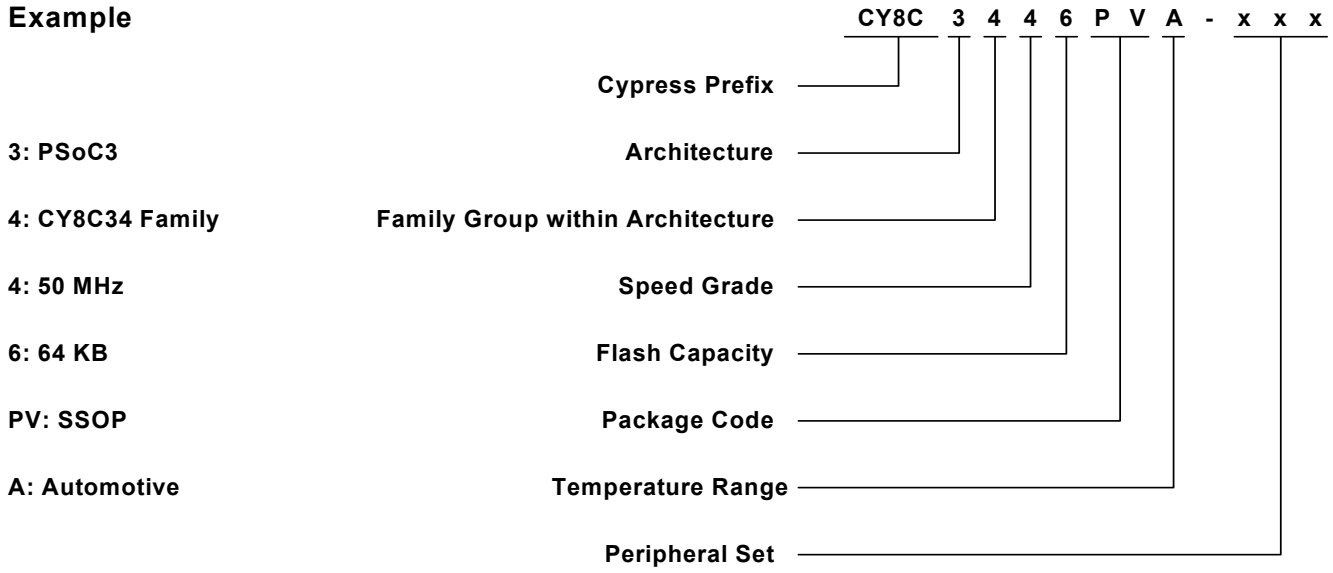
12.1 Part Numbering Conventions

PSoC 3 devices follow the part numbering convention described below. All fields are single character alphanumeric (0, 1, 2, …, 9, A, B, …, Z) unless stated otherwise.

CY8Cabcdefg-xxx

- a: Architecture
  - 3: PSoC 3
  - 5: PSoC 5
- b: Family Group within Architecture
  - 2: CY8C32 family
  - 4: CY8C34 family
  - 6: CY8C36 family
  - 8: CY8C38 family
- c: Speed Grade
  - 4: 50 MHz
- d: Flash Capacity
  - 4: 16 KB
  - 5: 32 KB
  - 6: 64 KB
- ef: Package Code
  - Two character alphanumeric
  - AX: TQFP
  - LT: QFN
  - PV: SSOP
- g: Temperature Range
  - C: commercial 0°C to 70°C
  - I: industrial -40°C to 85°C
  - A: automotive -40°C to 85°C
  - E: extended -40°C to 125°C
- xxx: Peripheral Set
  - Three character numeric
  - No meaning is associated with these three characters.

Example



All devices in the PSoC 3 CY8C34 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other "end of life" requirements.

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts

17. Revision History

Description Title: PSoC® 3: CY8C34 Automotive Family Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 001-57331				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2800070	01/05/10	SECA	New data sheet.
*A	2921624	04/26/10	MKEA	Updated Active Mode Idd values in Table 11-2 Updated Boost AC and DC specifications Updated solder paste reflow temperature (Table 11-3) Moved Filo spec from ILO DC to ILO AC table Updated Figure 7-14, Interrupt and DMA processing Added Bytes column in Tables 4-1 and 4-5 Updated Figure 6-3, Power mode transitions Updated JTAG and SWD specifications Updated Interrupt Vector table Updated Sales links Updated PCB Schematic Updated Vbias spec Added UDBs subsection under 11.6 Digital Peripherals Updated Iout parameter in LCD Direct Drive DC Specs table Added footnote in PLL AC Specification table Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table Updated Icc parameter in LCD Direct Drive DC Specs table Updated Tstartup parameter in AC Specifications table Updated LVD in Tables 6-2 and 6-3 In page 1, updated internal oscillator range under Prescision programmable clocking to start from 3 MHz Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9 Added PLL intermediate frequency row with footnote in PLL AC Specs table Added bullets on CapSense in page 1; added CapSense column in Section Updated Figure 2-6 (PCB Layout) Updated Tstartup values in Table 11-3 Updated IMO frequency Updated section 5.2 and Table 11-2 to correct suggestion of execution from Flash Updated Vref specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Tresp, high and low power modes, in Table 11-24. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table 71. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Updated SNR condition in Table 11-20
*B	3490494	01/11/2012	GIR	Updated Figure 6-7 on page 34
*C	3994809	05/08/2013	KPAT	Updated all tables in Electrical Specifications. Updated Ordering Information (Updated part numbers, JTAG ID). Removed all references of Vboost across the document.
*D	4040790	06/27/2013	RASB	Changed status from Preliminary to FInal. Updated Features. Updated Architectural Overview. Updated Pinouts. Updated Pin Descriptions. Updated Memory. Updated System Integration. Updated Digital Subsystem. Updated Analog Subsystem. Updated Electrical Specifications.