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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |   |
|----------------------------|---|
| Product Status             | Active  |
| Core Processor             | 8051  |
| Core Size                  | 8-Bit   |
| Speed                      | 50MHz   |
| Connectivity               | EBI/EMI, I <sup>2</sup> C, LINbus, SPI, UART/USART  |
| Peripherals                | CapSense, DMA, POR, PWM, WDT  |
| Number of I/O              | 25  |
| Program Memory Size        | 16KB (16K x 8)  |
| Program Memory Type        | FLASH   |
| EEPROM Size                | 512 x 8   |
| RAM Size                   | 2K x 8  |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V  |
| Data Converters            | A/D 16x12b; D/A 2x8b  |
| Oscillator Type            | Internal  |
| Operating Temperature      | -40°C ~ 125°C (TA)  |
| Mounting Type              | Surface Mount   |
| Package / Case             | 48-BSSOP (0.295", 7.50mm Width)   |
| Supplier Device Package    | 48-SSOP   |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3444pve-118">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3444pve-118</a> |

## ■ Program branching instructions

### 4.3.1 Instruction Set Summary

#### 4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. [Table 4-1](#) lists the different arithmetic instructions.

**Table 4-1. Arithmetic Instructions**

| Mnemonic      | Description  | Bytes | Cycles |
|---------------|--|-------|--------|
| ADD A,Rn      | Add register to accumulator                          | 1     | 1      |
| ADD A,Direct  | Add direct byte to accumulator                       | 2     | 2      |
| ADD A,@Ri     | Add indirect RAM to accumulator                      | 1     | 2      |
| ADD A,#data   | Add immediate data to accumulator                    | 2     | 2      |
| ADDC A,Rn     | Add register to accumulator with carry               | 1     | 1      |
| ADDC A,Direct | Add direct byte to accumulator with carry            | 2     | 2      |
| ADDC A,@Ri    | Add indirect RAM to accumulator with carry           | 1     | 2      |
| ADDC A,#data  | Add immediate data to accumulator with carry         | 2     | 2      |
| SUBB A,Rn     | Subtract register from accumulator with borrow       | 1     | 1      |
| SUBB A,Direct | Subtract direct byte from accumulator with borrow    | 2     | 2      |
| SUBB A,@Ri    | Subtract indirect RAM from accumulator with borrow   | 1     | 2      |
| SUBB A,#data  | Subtract immediate data from accumulator with borrow | 2     | 2      |
| INC A         | Increment accumulator                                | 1     | 1      |
| INC Rn        | Increment register                                   | 1     | 2      |
| INC Direct    | Increment direct byte                                | 2     | 3      |
| INC @Ri       | Increment indirect RAM                               | 1     | 3      |
| DEC A         | Decrement accumulator                                | 1     | 1      |
| DEC Rn        | Decrement register                                   | 1     | 2      |
| DEC Direct    | Decrement direct byte                                | 2     | 3      |
| DEC @Ri       | Decrement indirect RAM                               | 1     | 3      |
| INC DPTR      | Increment data pointer                               | 1     | 1      |
| MUL           | Multiply accumulator and B                           | 1     | 2      |
| DIV           | Divide accumulator by B                              | 1     | 6      |
| DAA           | Decimal adjust accumulator                           | 1     | 3      |

#### 4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. [Table 4-5](#) shows the list of jump instructions.

**Table 4-5. Jump Instructions**

| Mnemonic             | Description  | Bytes | Cycles |
|----------------------|--|-------|--------|
| ACALL addr11         | Absolute subroutine call                                     | 2     | 4      |
| LCALL addr16         | Long subroutine call   | 3     | 4      |
| RET                  | Return from subroutine                                       | 1     | 4      |
| RETI                 | Return from interrupt  | 1     | 4      |
| AJMP addr11          | Absolute jump  | 2     | 3      |
| LJMP addr16          | Long jump  | 3     | 4      |
| SJMP rel             | Short jump (relative address)                                | 2     | 3      |
| JMP @A + DPTR        | Jump indirect relative to DPTR                               | 1     | 5      |
| JZ rel               | Jump if accumulator is zero                                  | 2     | 4      |
| JNZ rel              | Jump if accumulator is nonzero                               | 2     | 4      |
| CJNE A, Direct, rel  | Compare direct byte to accumulator and jump if not equal     | 3     | 5      |
| CJNE A, #data, rel   | Compare immediate data to accumulator and jump if not equal  | 3     | 4      |
| CJNE Rn, #data, rel  | Compare immediate data to register and jump if not equal     | 3     | 4      |
| CJNE @Ri, #data, rel | Compare immediate data to indirect RAM and jump if not equal | 3     | 5      |
| DJNZ Rn, rel         | Decrement register and jump if not zero                      | 2     | 4      |
| DJNZ Direct, rel     | Decrement direct byte and jump if not zero                   | 3     | 5      |
| NOP                  | No operation   | 1     | 1      |

## 4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

### 4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight multi-layer AHB bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8-, 16-, 24-, and 32-bit addressing and data

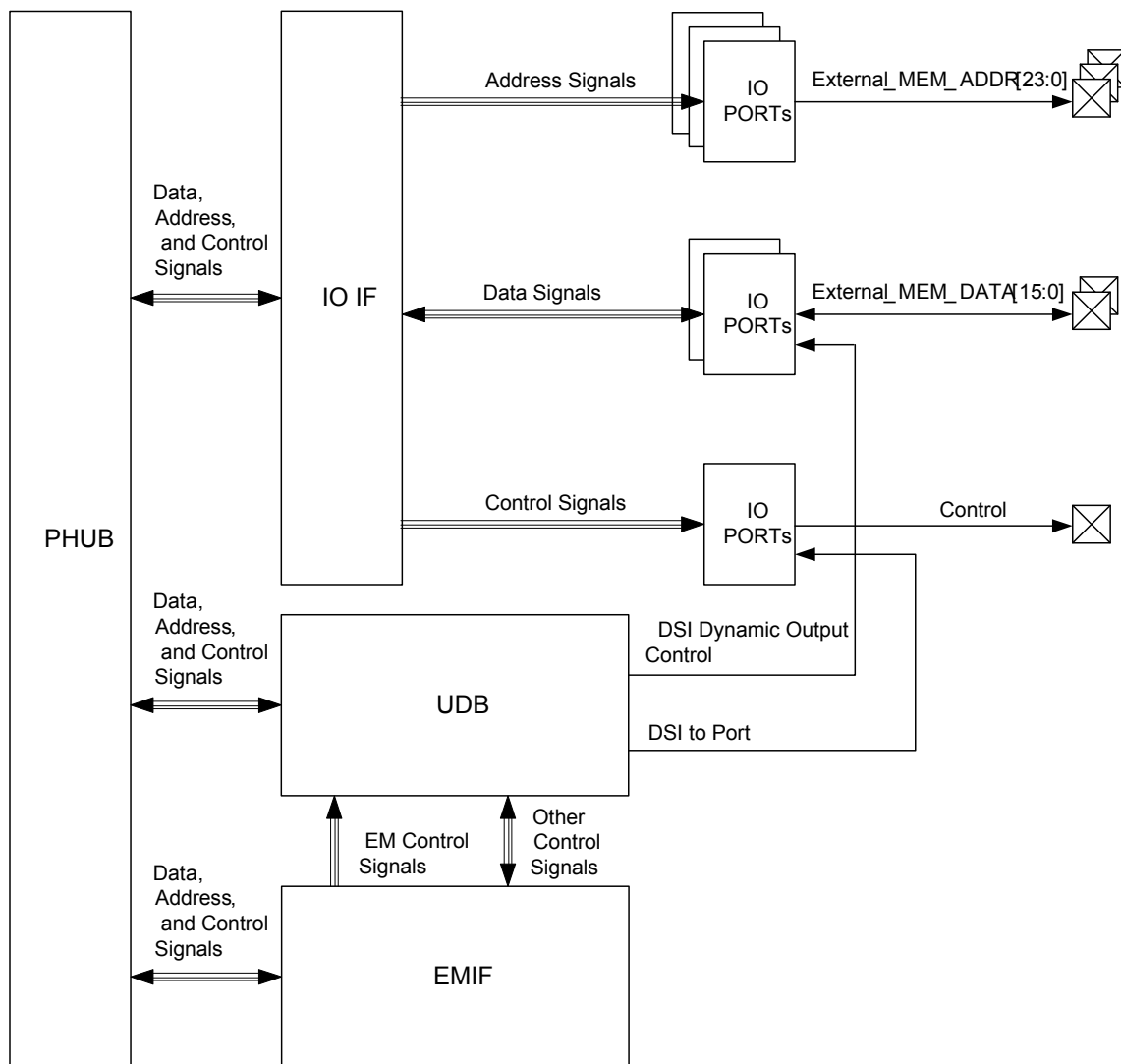
**Table 4-6. PHUB Spokes and Peripherals**

| PHUB Spokes | Peripherals   |
|-------------|---|
| 0           | SRAM  |
| 1           | IOs, PICU, EMIF   |
| 2           | PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface |
| 3           | Analog interface and trim, Decimator  |
| 4           | USB, CAN, I <sup>2</sup> C, Timers, Counters, and PWMs  |
| 5           | Reserved  |
| 6           | UDBs group 1  |
| 7           | UDBs group 2  |

## 5.6 External Memory Interface

CY8C34 provides an EMIF for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles. [Figure 5-1](#) is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C34 supports only one type of external memory device at a time. External memory can be accessed through the 8051 xdata space; up to 24 address bits can be used. See “[xdata Space](#)” section on page 25. The memory can be 8 or 16 bits wide.

**Figure 5-1. EMIF Block Diagram**

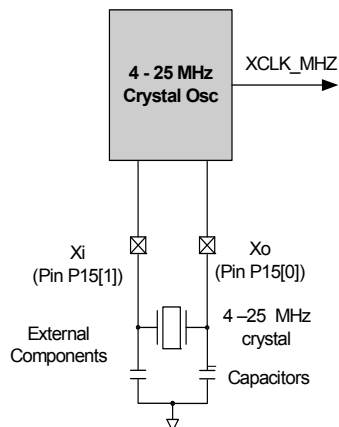


## 6.1.2 External Oscillators

### 6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see [Figure 6-2](#)). It supports a wide variety of crystal types, in the range of 4 to 25 MHz. When used in conjunction with the PLL, it can generate other clocks up to the device's maximum frequency (see [PLL](#)). The GPIO pins connecting to the external crystal and capacitors are fixed. MHzECO accuracy depends on the crystal chosen.

**Figure 6-2. MHzECO Block Diagram**

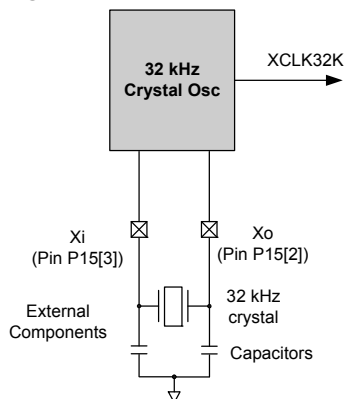


### 6.1.2.2 32.768-kHz ECO

The 32.768-kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see [Figure 6-3](#)). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1-second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

**Figure 6-3. 32kHzECO Block Diagram**



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance,  $CL1CL2 / (CL1 + CL2)$ , including pin and trace

capacitance, should equal the crystal CL value. For more information, refer to application note [AN54439: PSoC 3 and PSoC 5 External Oscillators](#). See also pin capacitance specifications in the "GPIO" section on page 74.

### 6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

## 6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The master clock is used to select and supply the fastest clock in the system for general clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the master clock to generate the bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADC and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50 percent duty cycle clocks, master clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

### 6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

The USBIO pins (P15[7] and P15[6]), when enabled for I/O mode, have limited drive mode control. The drive mode is set using the PRT15.DM0[7, 6] register. A resistive pull option is also available at the USBIO pins, which can be enabled using the PRT15.DM1[7, 6] register. When enabled for USB mode, the drive mode control has no impact on the configuration of the USB pins. Unlike the GPIO and SIO configurations, the port wide configuration registers do not configure the USB drive mode bits. Table 6-6 shows the drive mode configuration for the USBIO pins.

**Table 6-6. USBIO Drive Modes (P15[7] and P15[6])**

| PRT15.DM1[7,6]<br>Pull up enable | PRT15.DM0[7,6]<br>Drive Mode enable | PRT15.DR[7,6] = 1 | PRT15.DR[7,6] = 0 | Description                   |
|----------------------------------|-------------------------------------|-------------------|-------------------|-------------------------------|
| 0                                | 0                                   | High Z            | Strong Low        | Open Drain, Strong Low        |
| 0                                | 1                                   | Strong High       | Strong Low        | Strong Outputs                |
| 1                                | 0                                   | Res High (5k)     | Strong Low        | Resistive Pull Up, Strong Low |
| 1                                | 1                                   | Strong High       | Strong Low        | Strong Outputs                |

■ High impedance analog

The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

■ High impedance digital

The input buffer is enabled for digital signal input. This is the standard high impedance (High Z) state recommended for digital inputs.

■ Resistive pull-up or resistive pull-down

Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pullup and pull-down are not available with SIO in regulated output mode.

■ Open drain, drives high and open drain, drives low

Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I<sup>2</sup>C bus signal lines.

■ Strong drive

Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

■ Resistive pull-up and pull-down

Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pullup and pull-down are not available with SIO in regulated output mode.

#### 6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

#### 6.4.3 Bidirectional Mode

High speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRT×DM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

#### 6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRT×SLW registers.



Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

#### 7.2.2.3 Conditionals

Each datapath has two compares, with bit masking options. Compare operands include the two accumulators and the two data registers in a variety of configurations. Other conditions include zero detect, all ones detect, and overflow. These conditions are the primary datapath outputs, a selection of which can be driven out to the UDB routing matrix. Conditional computation can use the built in chaining to neighboring UDBs to operate on wider data widths without the need to use routing resources.

#### 7.2.2.4 Variable MSB

The most significant bit of an arithmetic and shift function can be programmatically specified. This supports variable width CRC and PRS functions, and in conjunction with ALU output masking, can implement arbitrary width timers, counters and shift blocks.

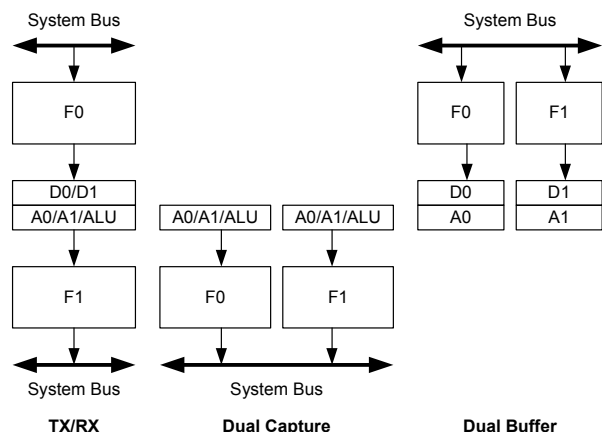
#### 7.2.2.5 Built in CRC/PRS

The datapath has built-in support for single cycle CRC computation and PRS generation of arbitrary width and arbitrary polynomial. CRC/PRS functions longer than 8 bits may be implemented in conjunction with PLD logic, or built in chaining may be use to extend the function into neighboring UDBs.

#### 7.2.2.6 Input/Output FIFOs

Each datapath contains two four-byte deep FIFOs, which can be independently configured as an input buffer (system bus writes to the FIFO, datapath internal reads the FIFO), or an output buffer (datapath internal writes to the FIFO, the system bus reads from the FIFO). The FIFOs generate status that are selectable as datapath outputs and can therefore be driven to the routing, to interact with sequencers, interrupts, or DMA.

**Figure 7-5. Example FIFO Configurations**



#### 7.2.2.7 Chaining

The datapath can be configured to chain conditions and signals such as carries and shift data with neighboring datapaths to create higher precision arithmetic, shift, CRC/PRS functions.

#### 7.2.2.8 Time Multiplexing

In applications that are over sampled, or do not need high clock rates, the single ALU block in the datapath can be efficiently shared with two sets of registers and condition generators. Carry and shift out data from the ALU are registered and can be selected as inputs in subsequent cycles. This provides support for 16-bit functions in one (8-bit) datapath.

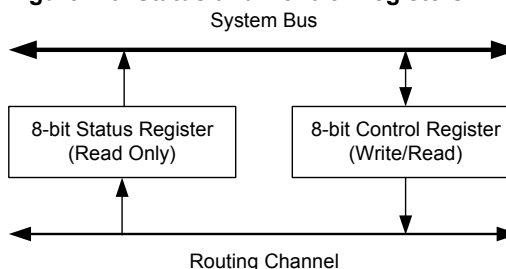
#### 7.2.2.9 Datapath I/O

There are six inputs and six outputs that connect the datapath to the routing matrix. Inputs from the routing provide the configuration for the datapath operation to perform in each cycle, and the serial data inputs. Inputs can be routed from other UDB blocks, other device peripherals, device I/O pins, and so on. The outputs to the routing can be selected from the generated conditions, and the serial data outputs. Outputs can be routed to other UDB blocks, device peripherals, interrupt and DMA controller, I/O pins, and so on.

#### 7.2.3 Status and Control Module

The primary purpose of this circuitry is to coordinate CPU firmware interaction with internal UDB operation.

**Figure 7-6. Status and Control Registers**



The bits of the control register, which may be written to by the system bus, are used to drive into the routing matrix, and thus provide firmware with the opportunity to control the state of UDB processing. The status register is read-only and it allows internal UDB state to be read out onto the system bus directly from internal routing. This allows firmware to monitor the state of UDB processing. Each bit of these registers has programmable connections to the routing matrix and routing connections are made depending on the requirements of the application.

#### 7.2.3.1 Usage Examples

As an example of control input, a bit in the control register can be allocated as a function enable bit. There are multiple ways to enable a function. In one method the control bit output would be routed to the clock control block in one or more UDBs and serve as a clock enable for the selected UDB blocks. A status example is a case where a PLD or datapath block generated a condition, such as a "compare true" condition that is captured and latched by the status register and then read (and cleared) by CPU firmware.

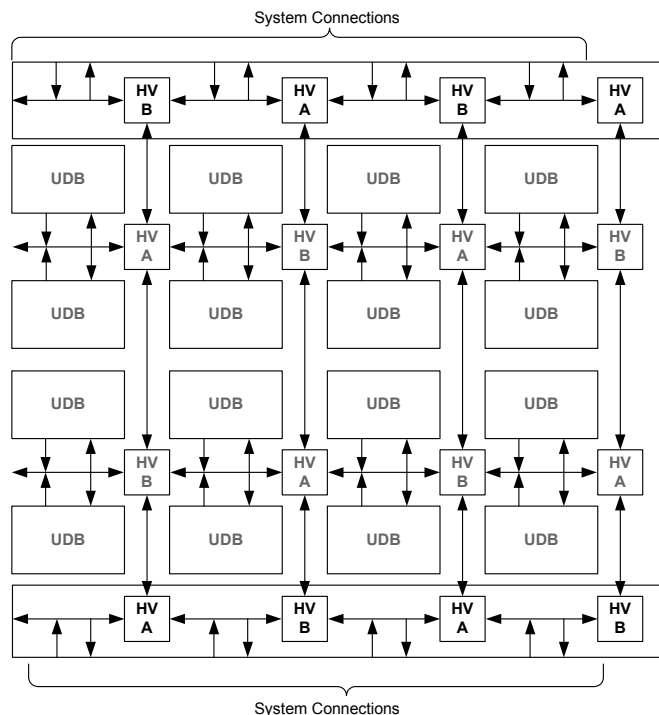
### 7.2.3.2 Clock Generation

Each subcomponent block of a UDB including the two PLDs, the datapath, and Status and Control, has a clock selection and control block. This promotes a fine granularity with respect to allocating clocking resources to UDB component blocks and allows unused UDB resources to be used by other functions for maximum system efficiency.

## 7.3 UDB Array Description

Figure 7-7 shows an example of a 16 UDB array. In addition to the array core, there are DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

**Figure 7-7. Digital System Interface Structure**

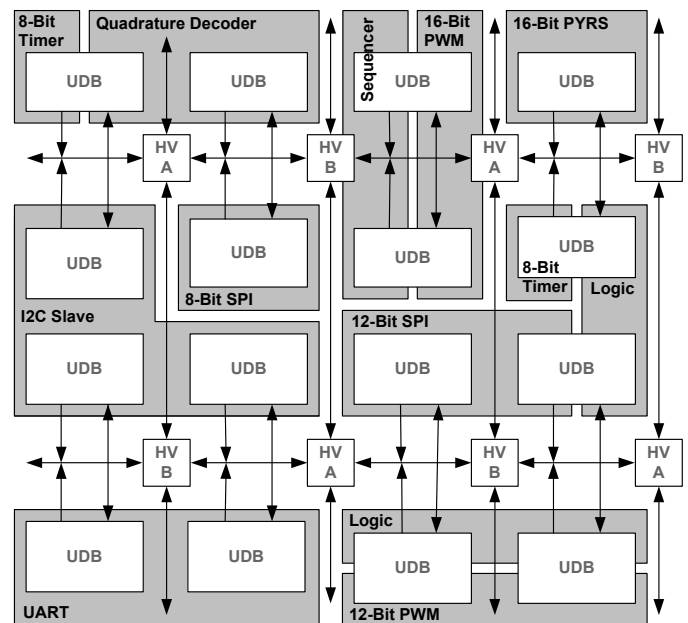


### 7.3.1 UDB Array Programmable Resources

Figure 7-8 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

**Figure 7-8. Function Mapping Example in a Bank of UDBs**



## 7.4 DSI Routing Interface Description

The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-9 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.



## 7.8 I<sup>2</sup>C

The I<sup>2</sup>C peripheral provides a synchronous two wire interface designed to interface the PSoC device with a two wire I<sup>2</sup>C serial communication bus. It is compatible<sup>[15]</sup> with I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O may be implemented with GPIO or SIO in open-drain modes. Additional I<sup>2</sup>C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

To eliminate the need for excessive CPU intervention and overhead, I<sup>2</sup>C specific support is provided for status detection and generation of framing bits. I<sup>2</sup>C operates as a slave, a master, or multimaster (Slave and Master).<sup>[16]</sup> In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I<sup>2</sup>C interfaces through DSI routing and allows direct connections to any GPIO or SIO pins.

I<sup>2</sup>C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup

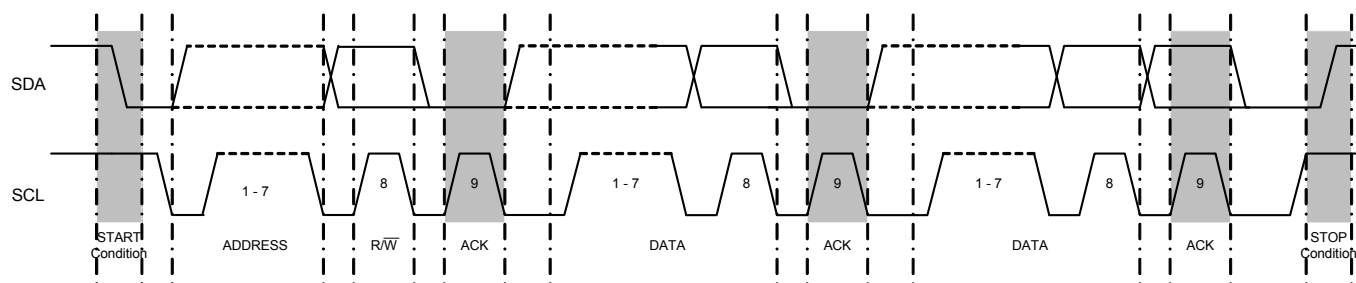
functionality is required, I<sup>2</sup>C pin connections are limited to the two special sets of SIO pins.

I<sup>2</sup>C features include:

- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in Figure 7-18. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

**Figure 7-18. I<sup>2</sup>C Complete Transfer Timing**



### Notes

15. The I<sup>2</sup>C peripheral is non-compliant with the NXP I<sup>2</sup>C specification in the following areas: analog glitch filter, I/O  $V_{OL}/I_{OL}$ , I/O hysteresis. The I<sup>2</sup>C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in "Inputs and Outputs" section on page 74 for details.
16. Fixed-block I<sup>2</sup>C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I<sup>2</sup>C component should be used instead.

### 8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

### 8.2.2.4 Multi Sample (Turbo)

The multi sample (turbo) mode operates identical to the Multi-sample mode for resolutions of 8 to 16 bits. For resolutions of 17 to 20 bits, the performance is about four times faster than the multi sample mode, because the ADC is only reset once at the end of conversion.

More information on output formats is provided in the Technical Reference Manual.

### 8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

### 8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

## 8.3 Comparators

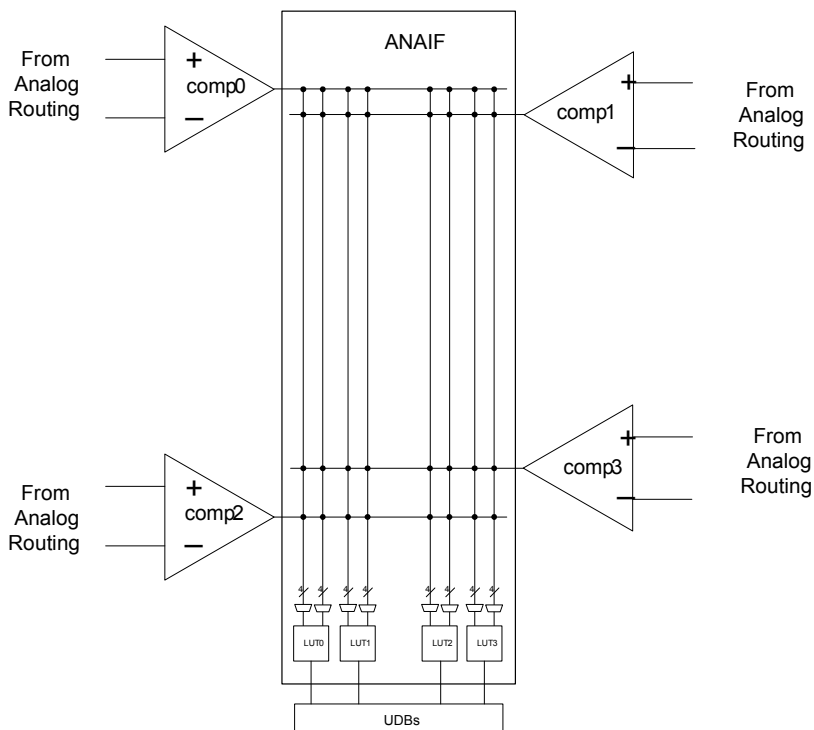
The CY8C34 family of devices contains four comparators in a device. Comparators have these features:

- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (VSSA to VDDA)
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

### 8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB DSI.

**Figure 8-5. Analog Comparator**



The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- PGA – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

#### 8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650  $\mu$ A. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

#### 8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

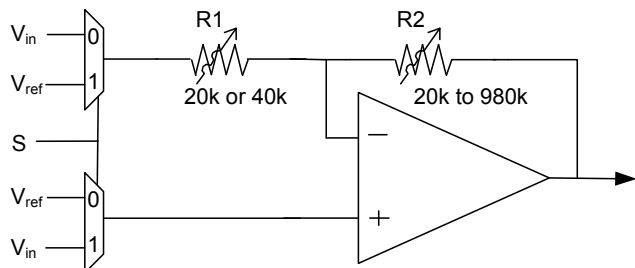
#### 8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-8. The schematic in Figure 8-8 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

**Table 8-3. Bandwidth**

| Gain | Bandwidth |
|------|-----------|
| 1    | 5.5 MHz   |
| 24   | 340 kHz   |
| 48   | 220 kHz   |
| 50   | 215 kHz   |

**Figure 8-8. PGA Resistor Settings**



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

#### 8.5.4 TIA

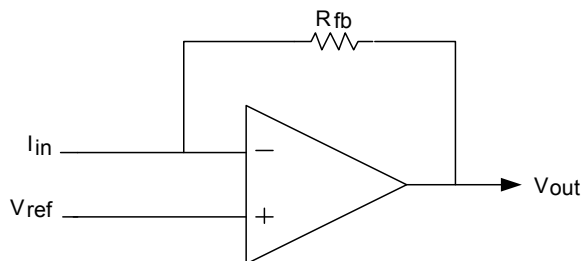
The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current  $I_{in}$ , the output voltage is  $V_{REF} - I_{in} \times R_{fb}$ , where  $V_{REF}$  is the value placed on the non inverting input. The feedback resistor  $R_{fb}$  is programmable between 20 K $\Omega$  and 1 M $\Omega$  through a configuration register.

Table 8-4 shows the possible values of  $R_{fb}$  and associated configuration settings.

**Table 8-4. Feedback Resistor Settings**

| Configuration Word | Nominal $R_{fb}$ (K $\Omega$ ) |
|--------------------|--------------------------------|
| 000b               | 20                             |
| 001b               | 30                             |
| 010b               | 40                             |
| 011b               | 60                             |
| 100b               | 120                            |
| 101b               | 250                            |
| 110b               | 500                            |
| 111b               | 1000                           |

**Figure 8-9. Continuous Time TIA Schematic**



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the  $V_{REF}$  TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

## 8.6 LCD Direct Drive

The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C34 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

## 11.2 Device Level Specifications

Specifications are valid for  $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$  and  $T_j \leq 150^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### 11.2.1 Device Level Specifications

**Table 11-2. DC Specifications**

| Parameter         | Description  | Conditions                      | Min  | Typ | Max              | Units |
|-------------------|--|---------------------------------|------|-----|------------------|-------|
| $V_{DDA}$         | Analog supply voltage and input to analog core regulator     | Analog core regulator enabled   | 1.8  | —   | 5.5              | V     |
| $V_{DDA}$         | Analog supply voltage, analog regulator bypassed             | Analog core regulator disabled  | 1.71 | 1.8 | 1.89             | V     |
| $V_{DDD}$         | Digital supply voltage relative to $V_{SSD}$                 | Digital core regulator enabled  | 1.8  | —   | $V_{DDA}^{[21]}$ | V     |
| $V_{DDD}$         | Digital supply voltage, digital regulator bypassed           | Digital core regulator disabled | 1.71 | 1.8 | 1.89             | V     |
| $V_{DDIO}^{[22]}$ | I/O supply voltage relative to $V_{SSIO}$                    |                                 | 1.71 | —   | $V_{DDA}^{[21]}$ | V     |
| $V_{CCA}$         | Direct analog core voltage input (Analog regulator bypass)   | Analog core regulator disabled  | 1.71 | 1.8 | 1.89             | V     |
| $V_{CCD}$         | Direct digital core voltage input (Digital regulator bypass) | Digital core regulator disabled | 1.71 | 1.8 | 1.89             | V     |

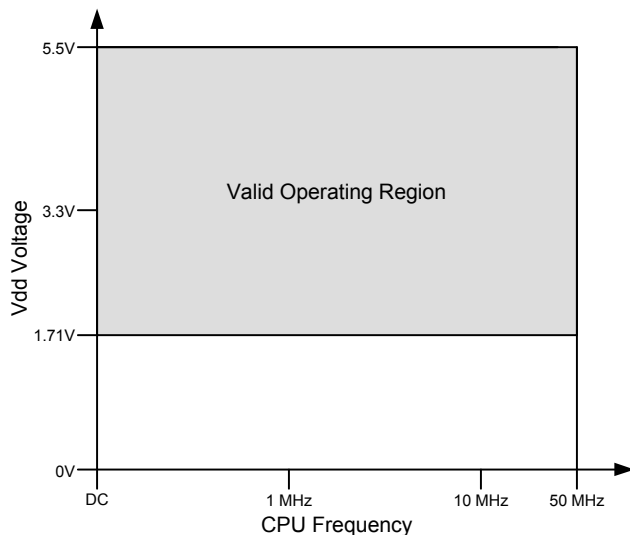
#### Notes

21.  $V_{DDX} = 3.3$  V.

22. Based on device specifications (not production tested).

**Table 11-3. AC Specifications<sup>[29]</sup>**

| Parameter           | Description  | Conditions   | Min | Typ | Max   | Units |
|---------------------|--|--|-----|-----|-------|-------|
| F <sub>CPU</sub>    | CPU frequency  | 1.71 V ≤ V <sub>ddd</sub> ≤ 5.5 V, -40°C ≤ T <sub>a</sub> ≤ 85°C and T <sub>j</sub> ≤ 100°C  | DC  | –   | 50    | MHz   |
|                     |  | 1.71 V ≤ V <sub>ddd</sub> ≤ 5.5 V, -40°C ≤ T <sub>a</sub> ≤ 125°C and T <sub>j</sub> ≤ 150°C   | DC  | –   | 50    | MHz   |
| F <sub>busclk</sub> | Bus frequency  | 1.71 V ≤ V <sub>ddd</sub> ≤ 5.5 V, -40°C ≤ T <sub>a</sub> ≤ 85°C and T <sub>j</sub> ≤ 100°C  | DC  | –   | 50    | MHz   |
|                     |  | 1.71 V ≤ V <sub>ddd</sub> ≤ 5.5 V, -40°C ≤ T <sub>a</sub> ≤ 125°C and T <sub>j</sub> ≤ 150°C   | DC  | –   | 50    | MHz   |
| Sv <sub>dd</sub>    | V <sub>dd</sub> ramp rate  |  | –   | –   | 0.066 | V/μs  |
| Tio_init            | Time from V <sub>ddd</sub> /V <sub>dda</sub> /V <sub>ccd</sub> /V <sub>cca</sub> ≥ IPOR to I/O ports set to their reset states |  | –   | –   | 10    | μs    |
| Tstartup            | Time from V <sub>ddd</sub> /V <sub>dda</sub> /V <sub>ccd</sub> /V <sub>cca</sub> ≥ PRES to CPU executing code at reset vector  | V <sub>cca</sub> /V <sub>ccd</sub> = regulated from V <sub>dda</sub> /V <sub>ddd</sub> , no PLL used, slow IMO boot mode (12 MHz typ.) | –   | –   | 66    | μs    |
| Tsleep              | Wakeup from sleep mode - Occurrence of LVD interrupt to beginning of execution of next CPU instruction                         | 1.71 V ≤ V <sub>ddd</sub> ≤ 5.5 V, T <sub>j</sub> ≤ 100°C  | –   | –   | 15    | μs    |
| Thibernate          | Wakeup from hibernate mode - Application of external interrupt to beginning of execution of next CPU instruction               |  | –   | –   | 100   | μs    |

**Figure 11-2. F<sub>cpu</sub> vs. V<sub>dd</sub>**

**Note**

29. Based on device characterization (not production tested).

### 11.3 Power Regulators

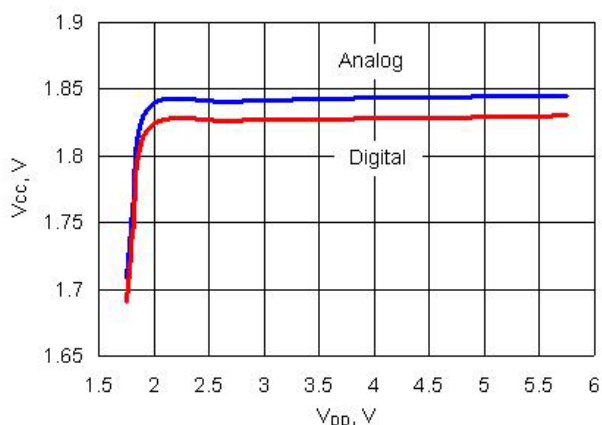
Specifications are valid for  $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$  and  $T_j \leq 150^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

#### 11.3.1 Digital Core Regulator

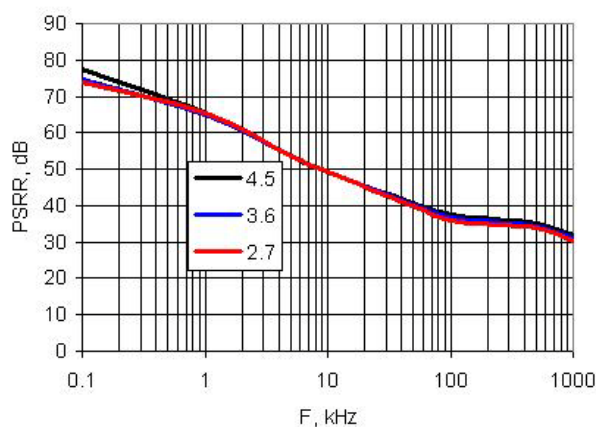
**Table 11-4. Digital Core Regulator DC Specifications**

| Parameter        | Description                  | Conditions  | Min | Typ  | Max | Units         |
|------------------|------------------------------|---|-----|------|-----|---------------|
| V <sub>ddd</sub> | Input voltage                |   | 1.8 | -    | 5.5 | V             |
| V <sub>ccd</sub> | Output voltage               |   | -   | 1.80 | -   | V             |
|                  | Regulator output capacitance | Total capacitance on the two V <sub>ccd</sub> pins. Each capacitor is $\pm 10\%$ , X5R ceramic or better, see <a href="#">Power System</a> on page 29 | -   | 1    | -   | $\mu\text{F}$ |

**Figure 11-3. Regulators V<sub>CC</sub> vs V<sub>DD</sub>**



**Figure 11-4. Digital Regulator PSRR vs Frequency and V<sub>DD</sub>**





#### 11.4.2 SIO

**Table 11-8. SIO DC Specifications**

| Parameter | Description  | Conditions                           | Min            | Typ | Max           | Units |
|-----------|--|--------------------------------------|----------------|-----|---------------|-------|
| Vinmax    | Maximum input voltage                                      | All allowed values of Vddio and Vddd | –              | –   | 5.5           | V     |
| Vinref    | Input voltage reference (Differential input mode)          |                                      | 0.5            | –   | 0.52 × Vddio  | V     |
| Voutref   | Output voltage reference (Regulated output mode)           |                                      |                |     |               |       |
|           |  | Vddio > 3.7                          | 1              | –   | Vddio-1       | V     |
|           |  | Vddio < 3.7                          | 1              | –   | Vddio - 0.5   | V     |
| Vih       | Input voltage high threshold                               |                                      |                |     |               |       |
|           | GPIO mode  | CMOS input                           | 0.7 × Vddio    | –   | –             | V     |
|           | Differential input mode                                    | With hysteresis                      | SIO_ref + 0.2  | –   | –             | V     |
| Vil       | Input voltage low threshold                                |                                      |                |     |               |       |
|           | GPIO mode  | CMOS input                           | –              | –   | 0.3 × Vddio   | V     |
|           | Differential input mode                                    | With hysteresis                      | –              | –   | SIO_ref – 0.2 | V     |
| Voh       | Output voltage high  |                                      |                |     |               |       |
|           | Unregulated mode   | Ioh = 4 mA, Vddio = 3.3 V            | Vddio - 0.4    | –   | –             | V     |
|           | Regulated mode <sup>[32]</sup>                             | Ioh = 1 mA                           | SIO_ref - 0.65 | –   | SIO_ref + 0.2 | V     |
|           | Regulated mode <sup>[32]</sup>                             | Ioh = 0.1 mA                         | SIO_ref - 0.3  | –   | SIO_ref + 0.2 | V     |
| Vol       | Output voltage low   |                                      |                |     |               |       |
|           |  | Vddio = 3.30 V, Iol = 25 mA          | –              | –   | 0.8           | V     |
|           |  | Vddio = 1.80 V, Iol = 4 mA           | –              | –   | 0.4           | V     |
|           |  | VDDIO = 3.3 V, IOL = 20 mA           | –              | –   | 0.4           | V     |
| Rpullup   | Pull up resistor   |                                      | 3.5            | 5.6 | 8.5           | kΩ    |
| Rpulldown | Pull down resistor   |                                      | 3.5            | 5.6 | 8.5           | kΩ    |
| Iil       | Input leakage current (absolute value) <sup>[33]</sup>     |                                      |                |     |               |       |
|           | Vih ≤ Vddsio   | 25°C, Vddsio = 3.0 V, Vih = 3.0 V    | –              | –   | 14            | nA    |
|           | Vih > Vddsio   | 25°C, Vddsio = 0 V, Vih = 3.0 V      | –              | –   | 10            | μA    |
| Cin       | Input Capacitance <sup>[33]</sup>                          |                                      | –              | –   | 7             | pF    |
| Vh        | Input voltage hysteresis (Schmitt-Trigger) <sup>[33]</sup> | Single ended mode (GPIO mode)        | –              | 40  | –             | mV    |
|           |  | Differential mode                    | –              | 35  | –             | mV    |
| Idiode    | Current through protection diode to Vssio                  |                                      | –              | –   | 100           | μA    |

**Notes**

32. See Figure 6-8 on page 35 for more information on SIO reference.

33. Based on device characterization (not production tested).

#### 11.4.4 XRES

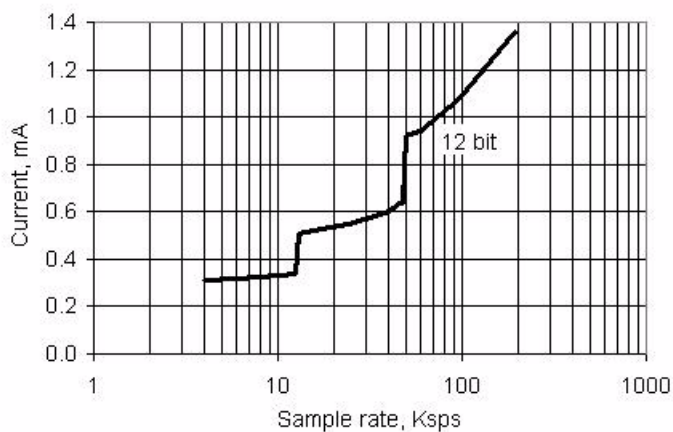
**Table 11-13. XRES DC Specifications**

| Parameter | Description  | Conditions                | Min                   | Typ | Max                   | Units      |
|-----------|--|---------------------------|-----------------------|-----|-----------------------|------------|
| Vih       | Input voltage high threshold                               | CMOS Input, PRT[x]CTL = 0 | $0.7 \times V_{ddio}$ | -   | -                     | V          |
| Vil       | Input voltage low threshold                                | CMOS Input, PRT[x]CTL = 0 | -                     | -   | $0.3 \times V_{ddio}$ | V          |
| Rpullup   | Pull up resistor   |                           | 3.5                   | 5.6 | 8.5                   | k $\Omega$ |
| Cin       | Input capacitance <sup>[29]</sup>                          |                           | -                     | 3   | -                     | pF         |
| Vh        | Input voltage hysteresis (Schmitt-Trigger) <sup>[29]</sup> |                           | -                     | 100 | -                     | mV         |
| Idiode    | Current through protection diode to Vddio and Vssio        |                           | -                     | -   | 100                   | $\mu$ A    |

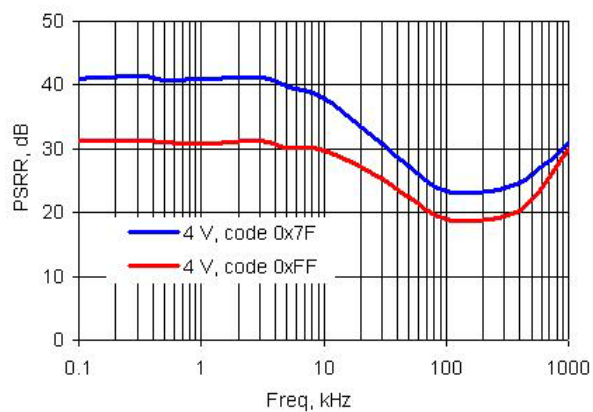
**Table 11-14. XRES AC Specifications**

| Parameter | Description       | Conditions | Min | Typ | Max | Units   |
|-----------|-------------------|------------|-----|-----|-----|---------|
| Treset    | Reset pulse width |            | 1   | -   | -   | $\mu$ s |

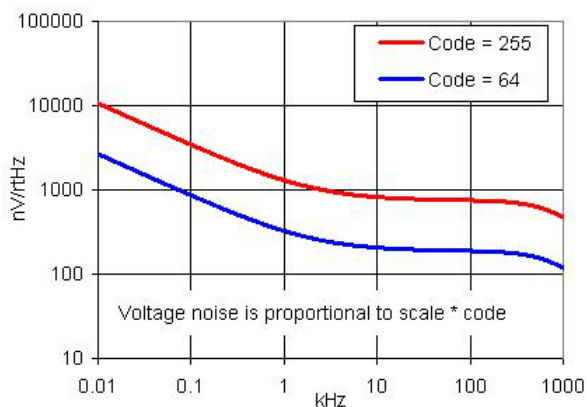
**Figure 11-24. Delta-sigma ADC IDD vs sps, Range =  $\pm 1.024$  V, Continuous Sample Mode, Input Buffer Bypassed**



**Figure 11-51. VDAC PSRR vs Frequency**



**Figure 11-52. VDAC Voltage Noise, 1 V Mode, High speed mode, Vdda = 5 V**



### 11.6.3 Pulse Width Modulation

**Table 11-41. PWM DC Specifications**

| Parameter | Description               | Conditions                                  | Min | Typ | Max | Units |
|-----------|---------------------------|---|-----|-----|-----|-------|
|           | Block current consumption | 16-bit PWM, at listed input clock frequency | –   | –   | –   | μA    |
|           | 3 MHz                     |   | –   | 15  | –   | μA    |
|           | 12 MHz                    |   | –   | 60  | –   | μA    |
|           | 50 MHz                    |   | –   | 260 | –   | μA    |

**Table 11-42. Pulse Width Modulation (PWM) AC Specifications**

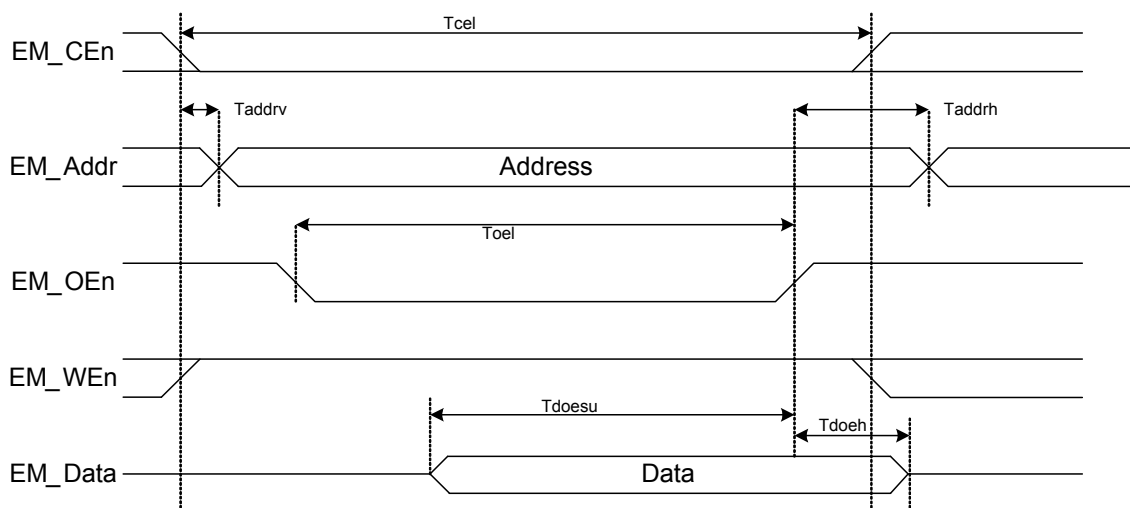
| Parameter | Description                   | Conditions   | Min | Typ | Max                | Units |
|-----------|-------------------------------|--|-----|-----|--------------------|-------|
|           | Operating frequency           | $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$  | DC  | –   | 50 <sup>[47]</sup> | MHz   |
|           |                               | $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$ | DC  | –   | 50                 | MHz   |
|           | Pulse width                   | $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$  | 15  | –   | –                  | ns    |
|           |                               | $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$ | 21  | –   | –                  | ns    |
|           | Pulse width (external)        | $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$  | 30  | –   | –                  | ns    |
|           |                               | $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$ | 42  | –   | –                  | ns    |
|           | Kill pulse width              | $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$  | 15  | –   | –                  | ns    |
|           |                               | $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$ | 21  | –   | –                  | ns    |
|           | Kill pulse width (external)   | $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$  | 30  | –   | –                  | ns    |
|           |                               | $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$ | 42  | –   | –                  | ns    |
|           | Enable pulse width            | $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$  | 15  | –   | –                  | ns    |
|           |                               | $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$ | 21  | –   | –                  | ns    |
|           | Enable pulse width (external) | $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$  | 30  | –   | –                  | ns    |
|           |                               | $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$ | 42  | –   | –                  | ns    |
|           | Reset pulse width             | $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$  | 15  | –   | –                  | ns    |
|           |                               | $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$ | 21  | –   | –                  | ns    |
|           | Reset pulse width (external)  | $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $T_j \leq 100^{\circ}\text{C}$  | 30  | –   | –                  | ns    |
|           |                               | $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$ | 42  | –   | –                  | ns    |

**Note**

 47. Applicable at  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ; 50 MHz at  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### 11.7.5 External Memory Interface

**Figure 11-56. Asynchronous Read Cycle Timing**



**Table 11-57. Asynchronous Read Cycle Specifications**

| Parameter   | Description                         | Conditions                   | Min      | Typ | Max      | Units |
|-------------|-------------------------------------|------------------------------|----------|-----|----------|-------|
| T           | EMIF clock period <sup>[54]</sup>   | $V_{dda} \geq 3.3 \text{ V}$ | 30.3     | –   | –        | ns    |
| $T_{cel}$   | EM_CEn low time                     |                              | $2T - 5$ | –   | $2T + 5$ | ns    |
| $T_{addrv}$ | EM_CEn low to EM_Addr valid         |                              | –        | –   | 5        | ns    |
| $T_{addrh}$ | Address hold time after EM_WEn high |                              | T        | –   | –        | ns    |
| $T_{oel}$   | EM_OEn low time                     |                              | $2T - 5$ | –   | $2T + 5$ | ns    |
| $T_{doesu}$ | Data to EM_OEn high setup time      |                              | $T + 15$ | –   | –        | ns    |
| $T_{doeh}$  | Data hold time after EM_OEn high    |                              | 3        | –   | –        | ns    |

**Note**

54. Limited by GPIO output frequency, see .



## 11.9 Clocking

Specifications are valid for  $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$  and  $T_j \leq 150^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### 11.9.1 Internal Main Oscillator

**Table 11-69. IMO DC Specifications**

| Parameter | Description           | Conditions                         | Min | Typ | Max | Units         |
|-----------|-----------------------|------------------------------------|-----|-----|-----|---------------|
|           | Supply current        |                                    |     |     |     |               |
|           | 62.6 MHz              |                                    | –   | –   | 600 | $\mu\text{A}$ |
|           | 48 MHz                |                                    | –   | –   | 500 | $\mu\text{A}$ |
|           | 24 MHz – USB mode     | With oscillator locking to USB bus | –   | –   | 500 | $\mu\text{A}$ |
|           | 24 MHz – non USB mode |                                    | –   | –   | 300 | $\mu\text{A}$ |
|           | 12 MHz                |                                    | –   | –   | 200 | $\mu\text{A}$ |
|           | 6 MHz                 |                                    | –   | –   | 180 | $\mu\text{A}$ |
|           | 3 MHz                 |                                    | –   | –   | 150 | $\mu\text{A}$ |

**Figure 11-62. IMO Current vs. Frequency**

