Welcome to E-XFL.COM

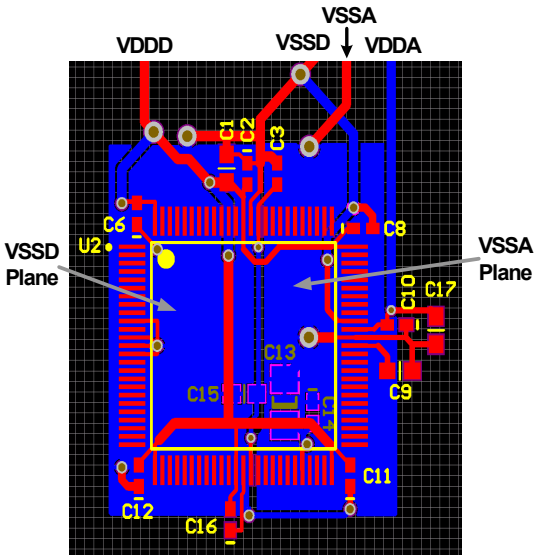
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3445axe-097

Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC2

Low resistance output pin for high current DACs (IDAC).

Opamp0OUT, Opamp2OUT

High current output of uncommitted opamp[10].

Extref0, Extref1

External reference input to the analog system.

Opamp0–, Opamp2–

Inverting input to uncommitted opamp.

Opamp0+, Opamp2+

Noninverting input to uncommitted opamp.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[10].

I2C0: SCL, I2C1: SCL

I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 25-MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV

Single wire viewer debug output.

TCK

JTAG test clock programming and debug port connection.

TDI

JTAG test data in programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

TMS

JTAG test mode select programming and debug port connection.

Note
10. GPIOs with opamp outputs are not recommended for use with CapSense.

USBIO, D+

Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from VDDD instead of from a VDDIO. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D–

Provides D– connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from VDDD instead of from a VDDIO. Pins are Do Not Use (DNU) on devices without USB.

VCCA.

Output of the analog core regulator or the input to the analog core. Requires a 1uF capacitor to VSSA. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator, (internally regulated mode, the default), do not tie any power to this pin. For details see Power System on page 29.

VCCD.

Output of the digital core regulator or the input to the digital core. The two VCCD pins must be shorted together, with the trace between them as short as possible, and a 1uF capacitor to VSSD. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator (internally regulated mode, the default), do not tie any power to this pin. For details see Power System on page 29.

VDDA

Supply for all analog peripherals and analog core regulator. VDDA must be the highest voltage present on the device. All other supply pins must be less than or equal to VDDA.

VDDD

Supply for all digital peripherals and digital core regulator. VDDD must be less than or equal to VDDA.

VSSA

Ground for all analog peripherals.

VSSD

Ground for all digital logic and I/O pins.

VDDIO0, VDDIO1, VDDIO2, VDDIO3

Supply for I/O pins. Each VDDIO must be tied to a valid operating voltage (1.71 V to 5.5 V), and must be less than or equal to VDDA.

$\overline{\text{XRES}}$ (and configurable $\overline{\text{XRES}}$)

External reset pin. Active low with internal pull-up. Pin P1[2] may be configured to be a XRES pin; see "Nonvolatile Latches (NVLs)" on page 22.

4. CPU

4.1 8051 CPU

The CY8C34 devices use a single cycle 8051 CPU, which is fully compatible with the original MCS-51 instruction set. The CY8C34 family uses a pipelined RISC architecture, which executes most instructions in 1 to 2 cycles to provide peak performance of up to 33 MIPS with an average of 2 cycles per instruction. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.

The 8051 CPU subsystem includes these features:

- Single cycle 8051 CPU
- Up to 64 KB of flash memory, up to 2 KB of EEPROM, and up to 8 KB of SRAM
- 512-byte instruction cache between CPU and flash
- Programmable nested vector interrupt controller
- DMA controller
- Peripheral HUB (PHUB)
- External memory interface (EMIF)

4.2 Addressing Modes

The following addressing modes are supported by the 8051:

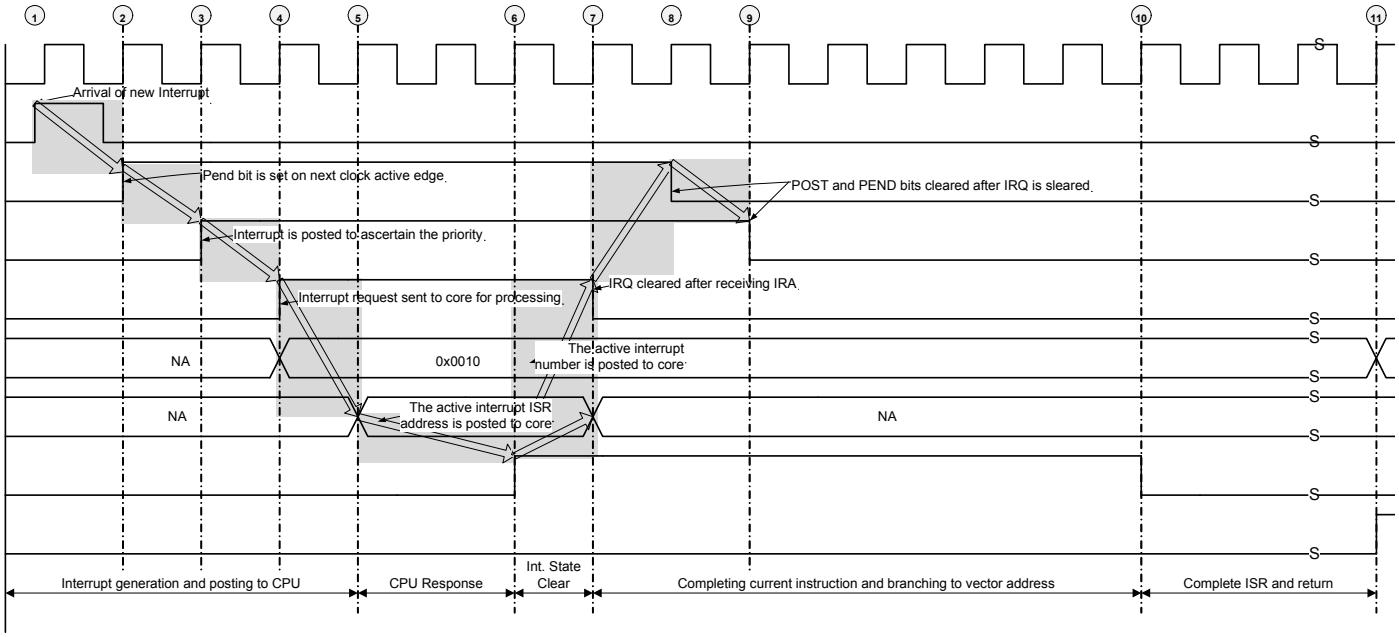
- Direct Addressing: The operand is specified by a direct 8-bit address field. Only the internal RAM and the SFRs can be accessed using this mode.
- Indirect Addressing: The instruction specifies the register which contains the address of the operand. The registers R0 or R1 are used to specify the 8-bit address, while the data pointer (DPTR) register is used to specify the 16-bit address.
- Register Addressing: Certain instructions access one of the registers (R0 to R7) in the specified register bank. These instructions are more efficient because there is no need for an address field.
- Register Specific Instructions: Some instructions are specific to certain registers. For example, some instructions always act on the accumulator. In this case, there is no need to specify the operand.
- Immediate Constants: Some instructions carry the value of the constants directly instead of an address.
- Indexed Addressing: This type of addressing can be used only for a read of the program memory. This mode uses the Data Pointer as the base and the accumulator value as an offset to read a program memory.
- Bit Addressing: In this mode, the operand is one of 256 bits.

4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions
- Data transfer instructions
- Boolean instructions

Figure 4-2. Interrupt Processing Timing Diagram



Notes

- 1: Interrupt triggered asynchronous to the clock
- 2: The PEND bit is set on next active clock edge to indicate the interrupt arrival
- 3: POST bit is set following the PEND bit
- 4: Interrupt request and the interrupt number sent to CPU core after evaluation priority (Takes 3 clocks)
- 5: ISR address is posted to CPU core for branching
- 6: CPU acknowledges the interrupt request
- 7: ISR address is read by CPU for branching
- 8, 9: PEND and POST bits are cleared respectively after receiving the IRA from core
- 10: IRA bit is cleared after completing the current instruction and starting the instruction execution from ISR location (Takes 7 cycles)
- 11: IRC is set to indicate the completion of ISR, Active int. status is restored with previous status

The total interrupt latency (ISR execution)

= POST + PEND + IRQ + IRA + Completing current instruction and branching

= 1+1+1+2+7 cycles

= 12 cycles

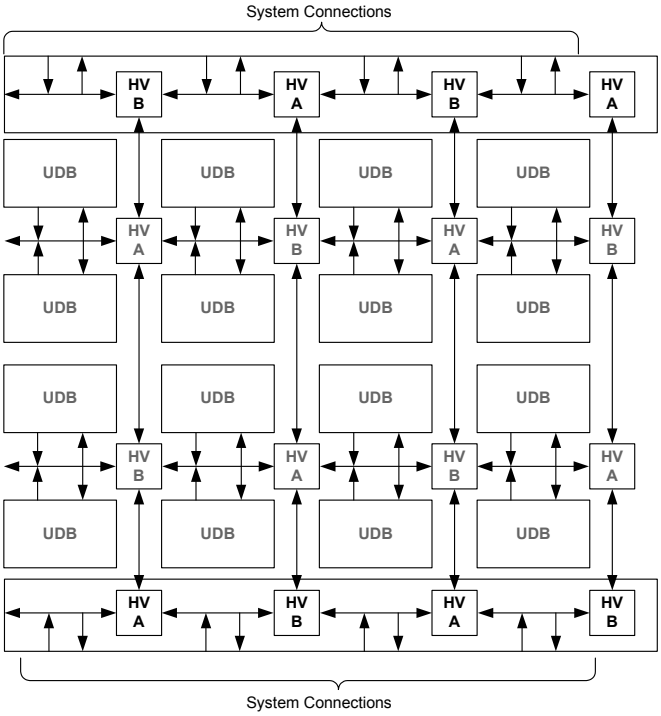
7.2.3.2 Clock Generation

Each subcomponent block of a UDB including the two PLDs, the datapath, and Status and Control, has a clock selection and control block. This promotes a fine granularity with respect to allocating clocking resources to UDB component blocks and allows unused UDB resources to be used by other functions for maximum system efficiency.

7.3 UDB Array Description

Figure 7-7 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-7. Digital System Interface Structure

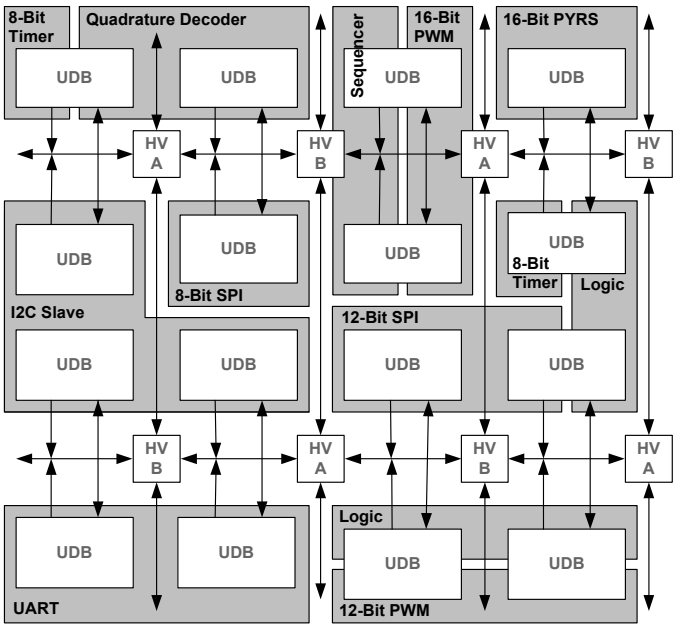


7.3.1 UDB Array Programmable Resources

Figure 7-8 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-8. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-9 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

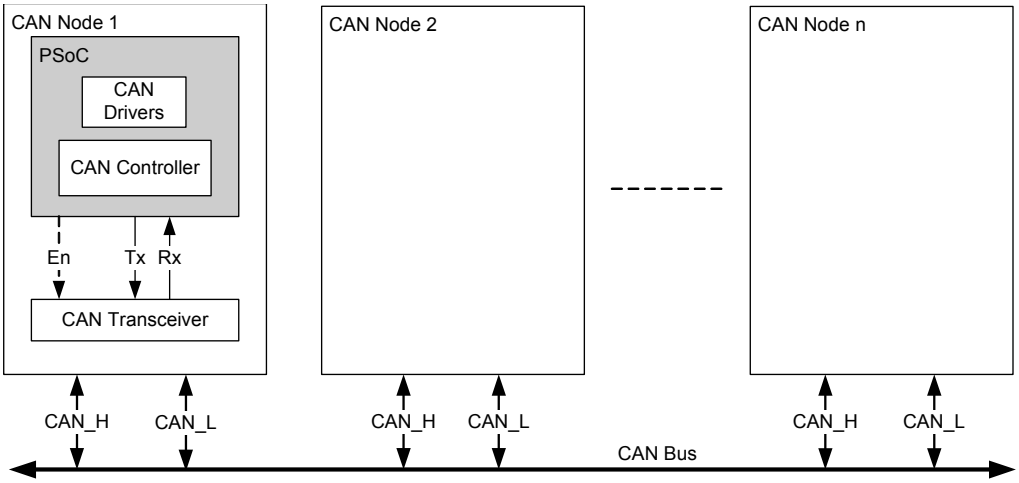
Signals in this category include:

- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

7.5 CAN

The CAN peripheral is a fully functional controller area network (CAN) supporting communication baud rates up to 1 Mbps. The CAN controller implements the CAN2.0A and CAN2.0B specifications as defined in the Bosch specification and conforms to the ISO-11898-1 standard. The CAN protocol was originally designed for automotive applications with a focus on a high level of fault detection. This ensures high communication reliability at a low cost. Because of its success in automotive applications, CAN is used as a standard communication protocol for motion oriented machine control networks (CANOpen) and factory automation applications (DeviceNet). The CAN controller features allow the efficient implementation of higher level protocols without affecting the performance of the microcontroller CPU. Full configuration support is provided in PSoC Creator.

Figure 7-14. CAN Bus System Implementation



7.5.1 CAN Features

- CAN2.0A/B protocol implementation – ISO 11898 compliant
  - Standard and extended frames with up to 8 bytes of data per frame
  - Message filter capabilities
  - Remote Transmission Request (RTR) support
  - Programmable bit rate up to 1 Mbps
- Listen Only mode
- SW readable error counter and indicator
- Sleep mode: Wake the device from sleep with activity on the Rx pin
- Supports two or three wire interface to external transceiver (Tx, Rx, and Enable). The three-wire interface is compatible with the Philips PHY; the PHY is not included on-chip. The three wires can be routed to any I/O
- Enhanced interrupt controller
  - CAN receive and transmit buffers status
  - CAN controller error status including BusOff
- Receive path
  - 16 receive buffers each with its own message filter
  - Enhanced hardware message filter implementation that covers the ID, IDE, and RTR
  - DeviceNet addressing support
  - Multiple receive buffers linkable to build a larger receive message array
  - Automatic transmission request (RTR) response handler
  - Lost received message notification
- Transmit path
  - Eight transmit buffers
  - Programmable transmit priority
  - Round robin
  - Fixed priority
  - Message transmissions abort capability

7.5.2 Software Tools Support

CAN Controller configuration integrated into PSoC Creator:

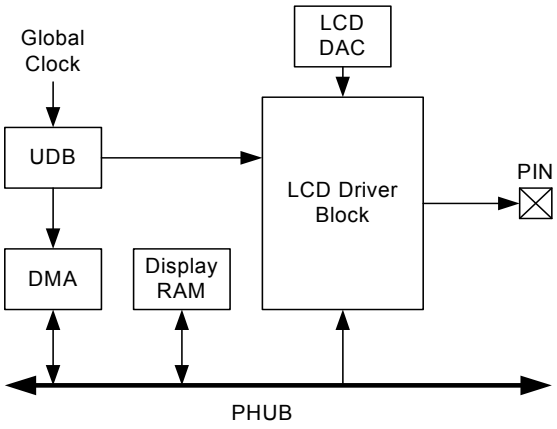
- CAN Configuration walkthrough with bit timing analyzer
- Receive filter setup

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-10. LCD System



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers through the DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.8 Temp Sensor

Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

11.2 Device Level Specifications

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled	1.8	–	5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled	1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to V_{SSD}	Digital core regulator enabled	1.8	–	V_{DDA}[21]	V
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled	1.71	1.8	1.89	V
V_{DDIO}[22]	I/O supply voltage relative to V_{SSIO}		1.71	–	V_{DDA}[21]	V
V_{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled	1.71	1.8	1.89	V
V_{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled	1.71	1.8	1.89	V

Notes
21. V_{DDX} = 3.3 V.
22. Based on device specifications (not production tested).

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ	Max	Units
	Sleep Mode[25]						
	CPU OFF RTC = ON (= ECO32K ON, in low power mode) Sleep timer = ON (= ILO ON at 1 kHz) [26] WDT = OFF I^2C Wake = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V–5.5 V	T = –40 °C	–	1.1	–	µA
			T = 25 °C	–	1.1	–	µA
			T = 85 °C	–	15	–	µA
			T = 125 °C	–	20.3	–	µA
		$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = –40 °C	–	1	–	µA
			T = 25 °C	–	1	–	µA
			T = 85 °C	–	12	–	µA
			T = 125 °C	–	18.5	–	µA
		$V_{CC} = V_{DDIO}$ = 1.71 V–1.95 V	T = 25 °C	–	2.2	–	µA
			T = 125 °C	–	16.2	–	µA
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I^2C Wake = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = 25 °C	–	2.2	–	µA
	I^2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V–3.6 V	T = 25 °C	–	2.2	–	µA

Notes
25. If Vccd and Vcca are externally regulated, the voltage difference between Vccd and Vcca must be less than 50 mV.
26. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.

Figure 11-6. GPIO Output High Voltage and Current

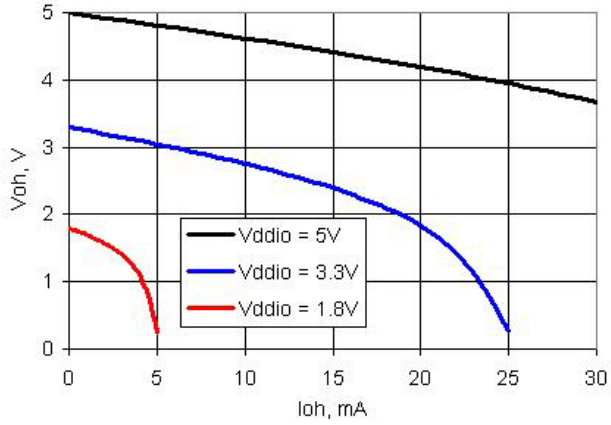


Figure 11-7. GPIO Output Low Voltage and Current

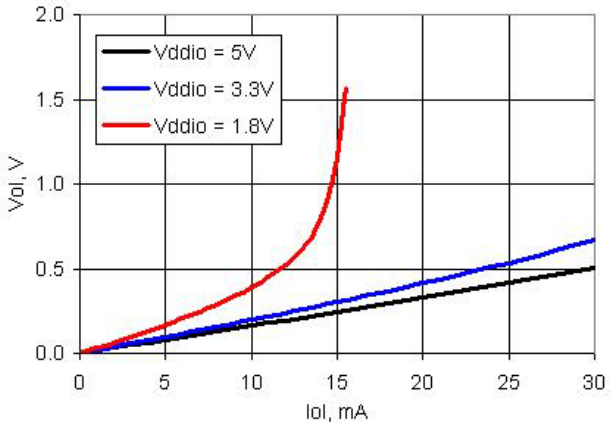


Figure 11-8. SIO Output High Voltage and Current, Unregulated Mode

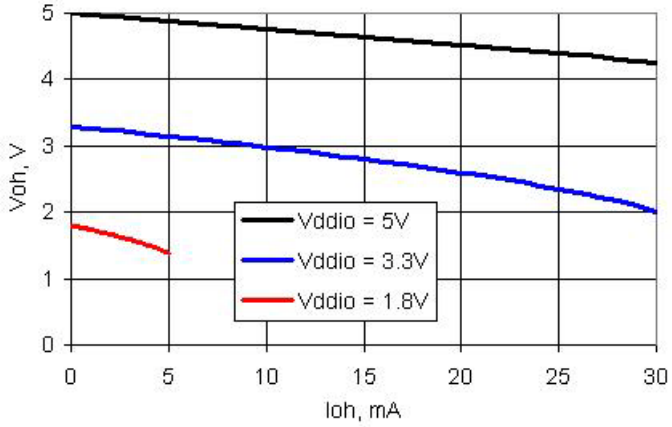


Figure 11-9. SIO Output Low Voltage and Current, Unregulated Mode

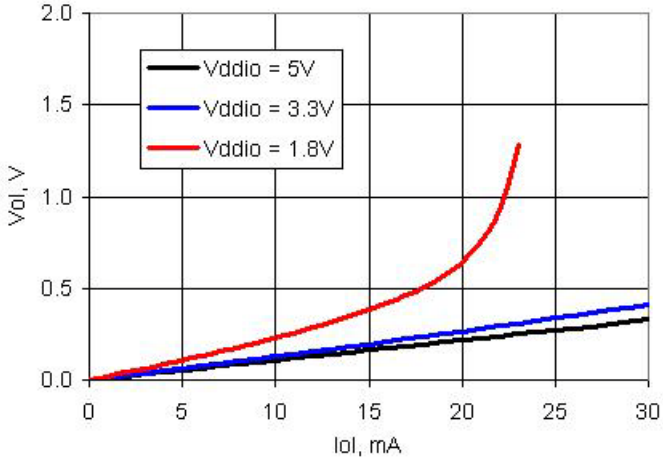


Figure 11-10. SIO Output High Voltage and Current, Regulated Mode

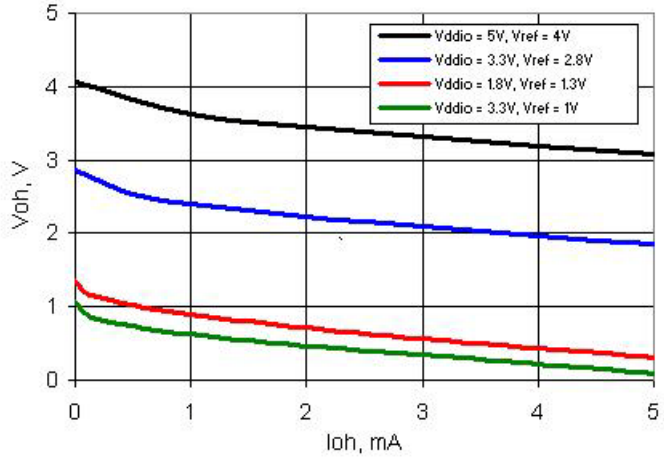


Table 11-9. SIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%)[29]	Cload = 25 pF, Vddio = 3.3 V	–	–	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%)[29]	Cload = 25 pF, Vddio = 3.3 V	–	–	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%)[29]	Cload = 25 pF, Vddio = 3.0 V	–	–	80	ns
TfallS	Fall time in Slow Strong Mode (90/10%)[29]	Cload = 25 pF, Vddio = 3.0 V	–	–	70	ns
Fsioout	SIO output operating frequency					
	3.3 V < Vddio < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	33	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	24	MHz
	1.71 V < Vddio < 3.3 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% Vddio into 25 pF	-	-	16	MHz
	3.3 V < Vddio < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% Vddio into 25 pF	-	-	5	MHz
	1.71 V < Vddio < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% Vddio into 25 pF	-	-	4	MHz
	3.3 V < Vddio < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	-	-	20	MHz
	1.71 V < Vddio < 3.3 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	-	-	10	MHz
	1.71 V < Vddio < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	-	-	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ Vddio ≤ 5.5 V	90/10% better than 60/40 duty cycle, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	66	MHz
		90/10% better than 60/40 duty cycle, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	50	MHz

Figure 11-31. IDAC INL vs Temperature, Range = 255 µA, High speed mode

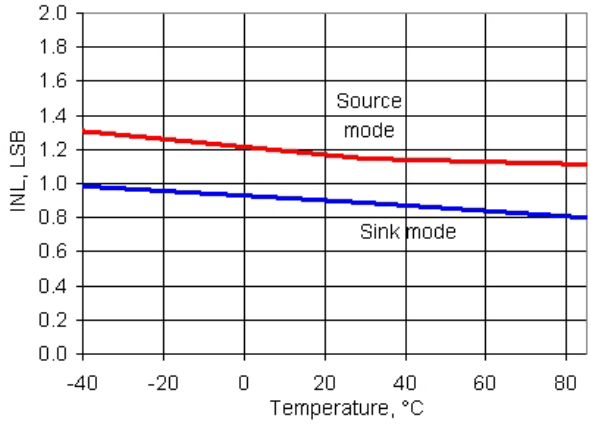


Figure 11-32. IDAC DNL vs Temperature, Range = 255 µA, High speed mode

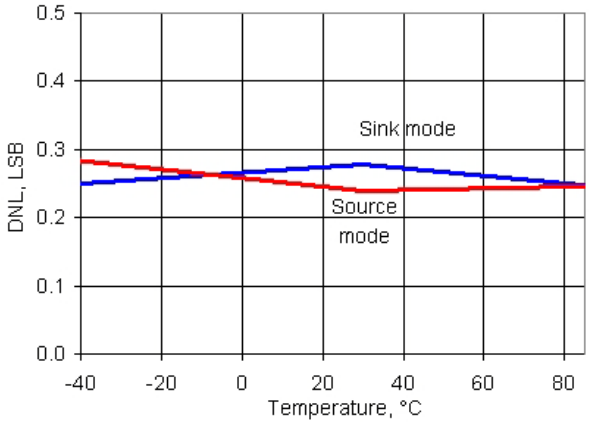


Figure 11-33. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

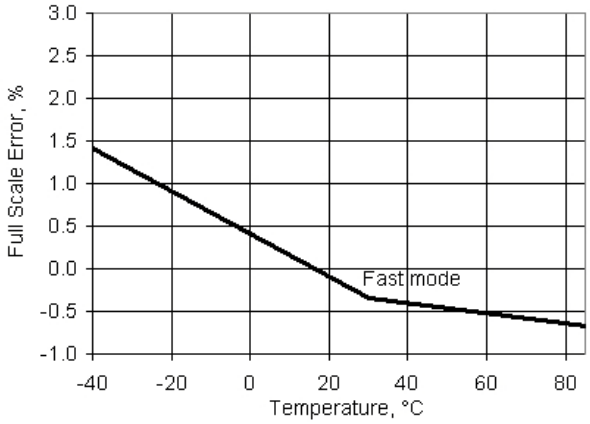


Table 11-25. IDAC (Current Digital-to-Analog Converter) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fdac	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, High speed mode, Vdda = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-37. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, Vdda = 5 V

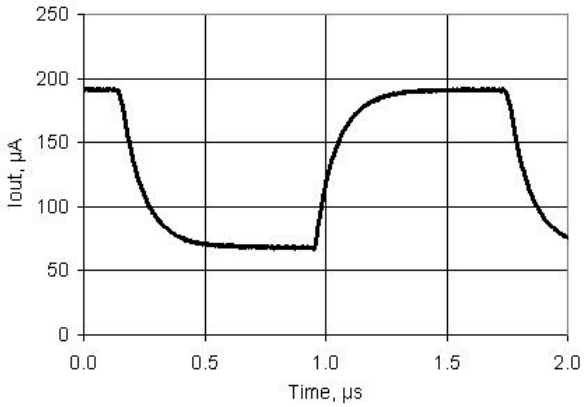
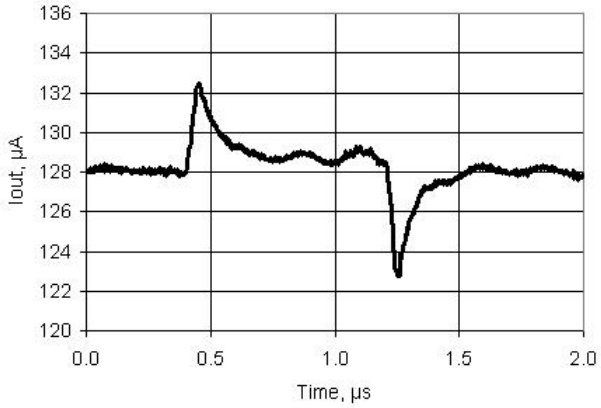


Figure 11-38. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, Vdda = 5 V



11.5.7 VDAC

Table 11-26. VDAC (Voltage Digital-to-Analog Converter) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Resolution			-	8	-	
Rout	Output resistance[29]					
	High	Vout = 4 V	-	16	-	kΩ
	Low	Vout = 1 V	-	4	-	kΩ
Vout	Output voltage range, code = 255	1 V scale	–	1.02	–	V
		4 V scale, Vdda = 5 V	–	4.08	–	V
INL	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
DNL	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
	Monotonicity		–	–	Yes	–
Eg	Gain error	1 V scale,	–	–	±2.5	%
		4 V scale	–	–	±2.5	%
TC_Eg	Temperature coefficient, gain error	1 V scale,	–	–	0.03	%FSR / °C
		4 V scale	–	–	0.03	%FSR / °C
VDAC_ICC	Operating current	Low speed mode	–	–	100	µA
		High speed mode	–	–	500	µA
V_{OS}	Zero scale error		–	0	±0.9	LSB

Figure 11-41. VDAC INL vs Input Code, 1 V Mode

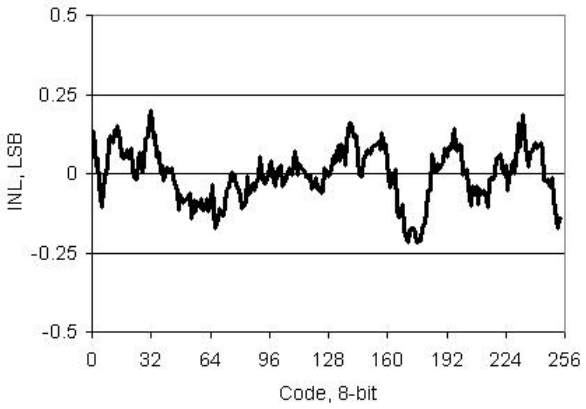
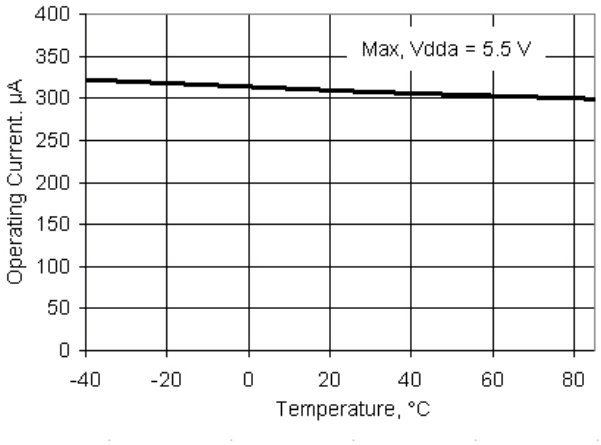


Figure 11-48. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode



11.8 PSoC System Resources

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.8.1 POR with Brown Out

For brown out detect in regulated mode, Vddd and Vdda must be ≥ 2.0 V. Brown out detect is available in externally regulated mode.

Table 11-61. Precise Power On Reset (PRES) with Brown Out DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRESR	Rising trip voltage	Factory trim	1.64	–	1.68	V
PRESF	Falling trip voltage		1.62	–	1.66	V

Table 11-62. Precise Power On Reset (PRES) with Brown Out AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRES_TR	Response time		–	–	0.5	µs
	V_{DDD}/V_{DDA} droop rate	Sleep mode	–	5	–	V/sec

11.8.2 Voltage Monitors

Table 11-63. Voltage Monitors DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

Table 11-64. Voltage Monitors AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Response time[57]		–	–	1	µs

Note
57. Based on device characterization (Not production tested).

11.9.2 Internal Low Speed Oscillator

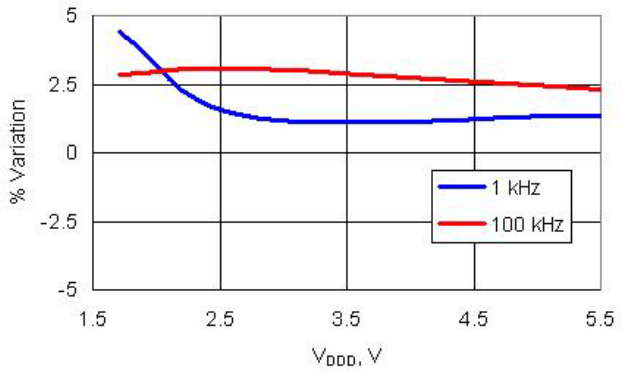
Table 11-71. ILO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current[61]	F_{OUT} = 1 kHz	–	–	1.7	µA
		F_{OUT} = 33 kHz	–	–	2.6	µA
		F_{OUT} = 100 kHz	–	–	2.6	µA
	Leakage current[61]	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	2.0	15	nA
		Power down mode				
	Leakage current[61]	-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	200	nA
		Power down mode				

Table 11-72. ILO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time	Turbo mode	-	-	2	ms
Filo	ILO frequencies (trimmed)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C				
	100 kHz		45	100	200	kHz
	1 kHz		0.5	1	2	kHz
	ILO frequencies (untrimmed)	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C				
	100 kHz		30	100	300	kHz
	1 kHz		0.3	1	3.5	kHz
Filo	ILO frequencies (trimmed)	-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C				
	100 kHz		45	-	450	kHz
	1 kHz		0.5	-	5	kHz
	ILO frequencies (untrimmed)	-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C				
	100 kHz		150	-	500	kHz
	1 kHz		0.3	-	6.5	kHz

Figure 11-65. ILO Frequency Variation vs. V_{DD}



Note
61. This value is calculated, not measured.
62. Based on device characterization (Not production tested).

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C34 device includes: a precision on-chip voltage reference, precision oscillators, Flash, ECC, DMA, a fixed function I^2C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and Analog Subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C34 derivatives incorporate device and Flash security in user-selectable security levels; see TRM for details.

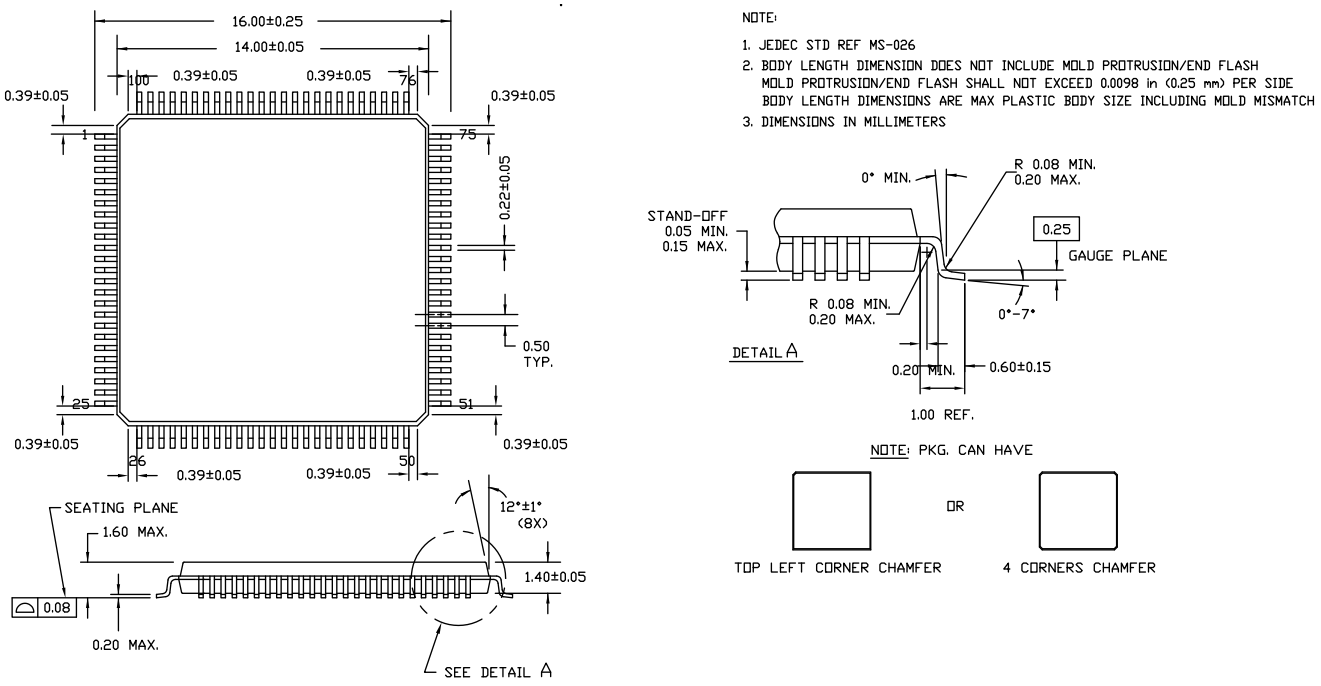
Table 12-1. CY8C34 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[67]				Package	JTAG ID[68]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks	Opamps	DFB	CapSense	UDBs[66]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
16 KB Flash																						
CY8C3444PVE-118	50	16	2	0.5	-	12-bit Del-Sig	2	4	2	2	-	✔	16	4	-	-	29	25	4	0	48-SSOP	0x1E076069
CY8C3444AXA-116	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	-	✔	16	4	-	-	70	62	8	0	100-TQFP	0x1E074069
CY8C3444PVA-100	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	-	✔	16	4	-	-	29	25	4	0	48-SSOP	0x1E064069
32 KB Flash																						
CY8C3445AXE-097	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	-	70	62	8	0	100-TQFP	0x1E061069
CY8C3445AXE-107	50	32	4	1	-	12-bit Del-Sig	2	4	2	2	-	✔	20	4	✔	-	72	62	8	2	100-TQFP	0x1E06B069
CY8C3445AXE-181	50	32	4	1	-	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	✔	70	62	8	0	100-TQFP	0x1E0B5069
CY8C3445AXA-104	50	32	4	1	-	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	-	70	62	8	0	100-TQFP	0x1E068069
CY8C3445AXA-108	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	-	✔	20	4	✔	-	72	62	8	2	100-TQFP	0x1E06C069
CY8C3445AXA-181	50	32	4	1	-	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	✔	70	62	8	0	100-TQFP	0x1E0B5069
CY8C3445PVA-090	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	-	✔	20	4	✔	-	31	25	4	2	48-SSOP	0x1E05A069
CY8C3445PVA-094	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	-	✔	20	4	-	-	29	25	4	0	48-SSOP	0x1E05E069
64 KB Flash																						
CY8C3446AXE-099	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	✔	-	72	62	8	2	100-TQFP	0x1E063069
CY8C3446AXE-115	50	64	8	2	-	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	-	70	62	8	0	100-TQFP	0x1E073069
CY8C3446PVE-082	50	64	8	2	-	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	-	29	25	4	0	48-SSOP	0x0E052069
CY8C3446PVE-102	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E066069
CY8C3446AXA-099	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	✔	-	72	62	8	2	100-TQFP	0x1E063069
CY8C3446AXA-105	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	-	70	62	8	0	100-TQFP	0x1E069069
CY8C3446PVA-076	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	✔	-	31	25	4	2	48-SSOP	0x1E04C069
CY8C3446PVA-091	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	-	29	25	4	0	48-SSOP	0x1E05B069
CY8C3446PVA-102	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	-	✔	24	4	-	✔	29	25	4	0	48-SSOP	0x1E066069

Notes

66. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the "Example Peripherals" section on page 40 for more information on how UDBs may be used.
67. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the ""I/O System and Routing" section on page 33" for details on the functionality of each of these types of I/O.
68. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

Figure 13-2. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline



51-85048 *I

18. Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support