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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3445pva-094

Figure 2-4. 100-pin TQFP Part Pinout

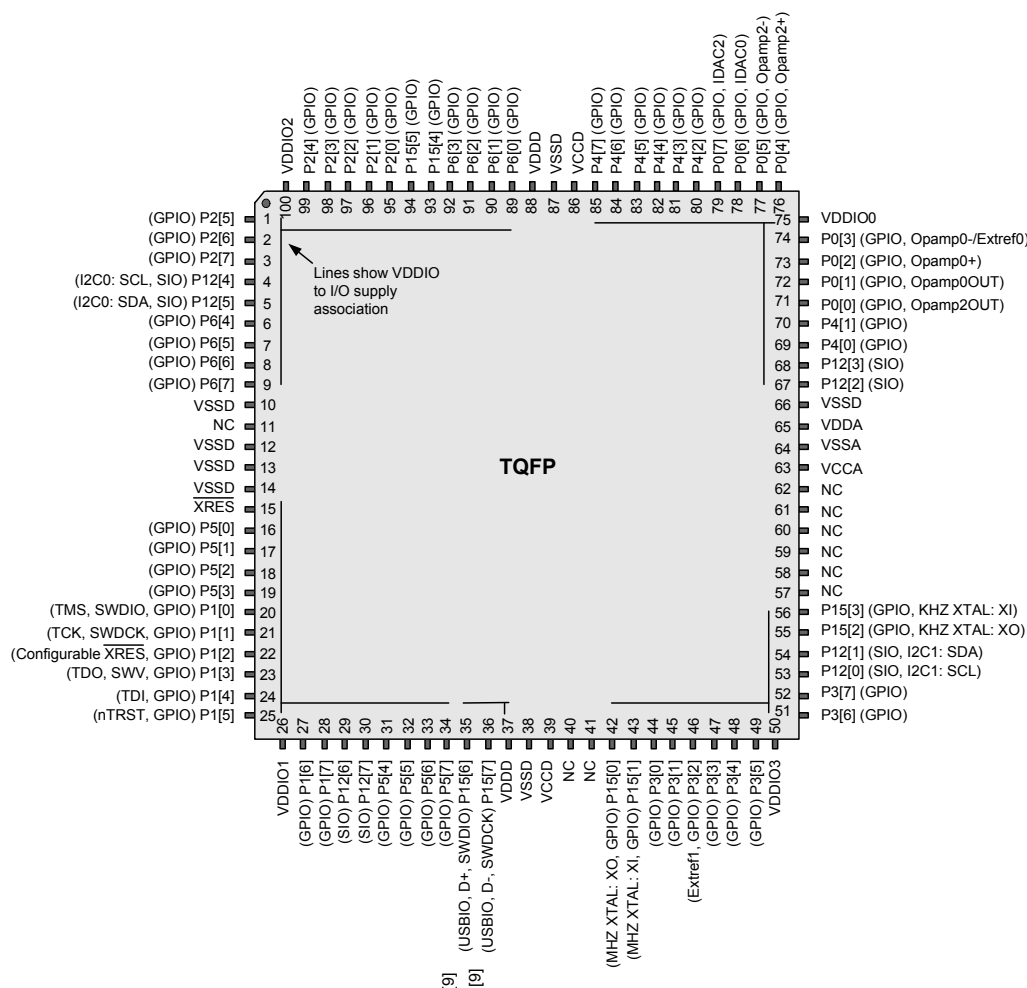


Figure 2-5 and Figure 2-6 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-5 and Power System on page 29. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled Vssd must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note, [AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5](#).

Note

9. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. [Table 4-5](#) shows the list of jump instructions.

Table 4-5. Jump Instructions

Mnemonic	Description	Bytes	Cycles
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A + DPTR	Jump indirect relative to DPTR	1	5
JZ rel	Jump if accumulator is zero	2	4
JNZ rel	Jump if accumulator is nonzero	2	4
CJNE A, Direct, rel	Compare direct byte to accumulator and jump if not equal	3	5
CJNE A, #data, rel	Compare immediate data to accumulator and jump if not equal	3	4
CJNE Rn, #data, rel	Compare immediate data to register and jump if not equal	3	4
CJNE @Ri, #data, rel	Compare immediate data to indirect RAM and jump if not equal	3	5
DJNZ Rn, rel	Decrement register and jump if not zero	2	4
DJNZ Direct, rel	Decrement direct byte and jump if not zero	3	5
NOP	No operation	1	1

4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight multi-layer AHB bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8-, 16-, 24-, and 32-bit addressing and data

Table 4-6. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, CAN, I ² C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

5.7 Memory Map

The CY8C34 8051 memory map is very similar to the MCS-51 memory map.

5.7.1 Code Space

The CY8C34 8051 code space is 64 KB. Only main flash exists in this space. See the [Flash Program Memory](#) on page 21.

5.7.2 Internal Data Space

The CY8C34 8051 internal data space is 384 bytes, compressed within a 256-byte space. This space consists of 256 bytes of RAM (in addition to the SRAM mentioned in [Static RAM](#) on page 21) and a 128-byte space for special function registers (SFR). See [Figure 5-2](#). The lowest 32 bytes are used for 4 banks of registers R0-R7. The next 16 bytes are bit-addressable.

Figure 5-2. 8051 Internal Data Space

0x00	4 Banks, R0-R7 Each	
0x1F		
0x20	Bit Addressable Area	
0x2F		
0x30	Lower Core RAM Shared with Stack Space (direct and indirect addressing)	
0x7F		
0x80	Upper Core RAM Shared with Stack Space (indirect addressing)	SFR Special Function Registers (direct addressing)
0xFF		

In addition to the register or bit address modes used with the lower 48 bytes, the lower 128 bytes can be accessed with direct or indirect addressing. With direct addressing mode, the upper 128 bytes map to the SFRs. With indirect addressing mode, the upper 128 bytes map to RAM. Stack operations use indirect addressing; the 8051 stack space is 256 bytes. See the [“Addressing Modes”](#) section on page 10.

5.7.3 SFRs

The SFR space provides access to frequently accessed registers. The memory map for the SFR memory space is shown in [Table 5-4](#).

Table 5-4. SFR Map

Address	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	SFRPRT15DR	SFRPRT15PS	SFRPRT15SEL	–	–	–	–	–
0xF0	B	–	SFRPRT12SEL	–	–	–	–	–
0xE8	SFRPRT12DR	SFRPRT12PS	MXAX	–	–	–	–	–
0xE0	ACC	–	–	–	–	–	–	–
0xD8	SFRPRT6DR	SFRPRT6PS	SFRPRT6SEL	–	–	–	–	–
0xD0	PSW	–	–	–	–	–	–	–
0xC8	SFRPRT5DR	SFRPRT5PS	SFRPRT5SEL	–	–	–	–	–
0xC0	SFRPRT4DR	SFRPRT4PS	SFRPRT4SEL	–	–	–	–	–
0xB8				–	–	–	–	–
0xB0	SFRPRT3DR	SFRPRT3PS	SFRPRT3SEL	–	–	–	–	–
0xA8	IE	–	–	–	–	–	–	–
0xA0	P2AX	–	SFRPRT1SEL	–	–	–	–	–
0x98	SFRPRT2DR	SFRPRT2PS	SFRPRT2SEL	–	–	–	–	–
0x90	SFRPRT1DR	SFRPRT1PS	–	DPX0	–	DPX1	–	–
0x88	–	SFRPRT0PS	SFRPRT0SEL	–	–	–	–	–
0x80	SFRPRT0DR	SP	DPL0	DPH0	DPL1	DPH1	DPS	–

The CY8C34 family provides the standard set of registers found on industry standard 8051 devices. In addition, the CY8C34 devices add SFRs to provide direct access to the I/O ports on the device. The following sections describe the SFRs added to the CY8C34 family.

6. System Integration

6.1 Clocking System

The clocking system generates, divides, and distributes clocks throughout the PSoC system. For the majority of systems, no external crystal is required. The IMO and PLL together can generate up to a 50 MHz clock, accurate to ± 1 percent over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. Any of the clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows you to build clocking systems with minimal input. You can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent in PSoC.

Key features of the clocking system include:

- Seven general purpose clock sources
 - 3- to 62-MHz IMO, $\pm 1\%$ at 3 MHz
 - 4- to 25-MHz external crystal oscillator (MHzECO)
 - Clock doubler provides a doubled clock frequency output for the USB block, see [USB Clock Domain](#) on page 28.
 - DSI signal from an external I/O pin or other logic
 - 24- to 50-MHz fractional PLL sourced from IMO, MHzECO, or DSI
 - 1-kHz, 33-kHz, 100-kHz ILO for WDT and sleep timer
 - 32.768-kHz external crystal oscillator (kHzECO) for RTC
- IMO has a USB mode that auto locks to the USB bus clock requiring no external crystal for USB (USB equipped parts only)
- Independently sourced clock in all clock dividers
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the bus clock
- Dedicated 4-bit divider for the CPU clock
- Automatic clock configuration in PSoC Creator

Table 6-1. Oscillator Summary

Source	Fmin	Tolerance at Fmin	Fmax	Tolerance at Fmax	Startup Time
IMO	3 MHz	$\pm 1\%$ over voltage and temperature	62 MHz	$\pm 7\%$	13 μ s max
MHzECO	4 MHz	Crystal dependent	25 MHz	Crystal dependent	5 ms typ, max is crystal dependent
DSI	0 MHz	Input dependent	50 MHz	Input dependent	Input dependent
PLL	24 MHz	Input dependent	50 MHz	Input dependent	250 μ s max
Doubler	48 MHz	Input dependent	48 MHz	Input dependent	1 μ s max
ILO	1 kHz	-50% , $+100\%$	100 kHz	-55% , $+100\%$	15 ms max in lowest power mode
kHzECO	32 kHz	Crystal dependent	32 kHz	Crystal dependent	500 ms typ, max is crystal dependent

6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-5. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-10 depicts a simplified pin view based on each of the eight drive modes. Table 6-5 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-10. Drive Mode

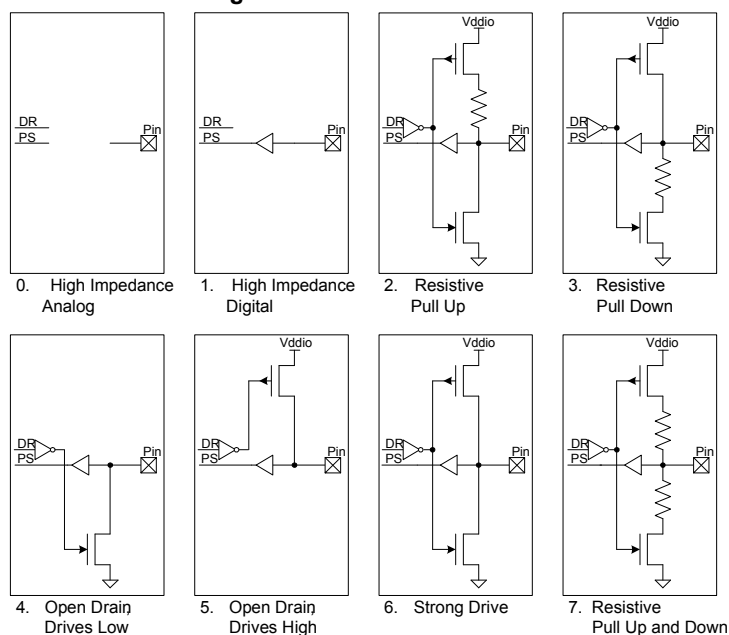


Table 6-5. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedance analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up ^[13]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down ^[13]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down ^[13]	1	1	1	Res High (5K)	Res Low (5K)

Note

¹³. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to '1' and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt. While level sensitive interrupts are not directly supported; UDB provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip's analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin. The SIO port pins support an additional regulated high output capability, as described in [Adjustable Output Level](#).

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders^[14]. See the ["CapSense"](#) section on page 58 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the ["LCD Direct Drive"](#) section on page 57 for details.

6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO's respective VDDIO. SIO pins are individually configurable to output either the standard VDDIO level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see [Figure 6-11](#)). The ["DAC"](#) section on page 59 has more details on VDAC use and reference routing to the SIO pins. Resistive pullup and pull-down drive modes are not available with SIO in regulated output mode.

6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which is used to set the digital input buffer reference level for interface to external signals that differ in voltage from VDDIO. The reference sets the pins voltage threshold for a high logic level (see [Figure 6-11](#)). Available input thresholds are:

- $0.5 \times VDDIO$
- $0.4 \times VDDIO$
- $0.5 \times V_{REF}$
- V_{REF}

Typically a voltage DAC (VDAC) generates the V_{REF} reference. ["DAC"](#) section on page 59 has more details on VDAC use and reference routing to the SIO pins.

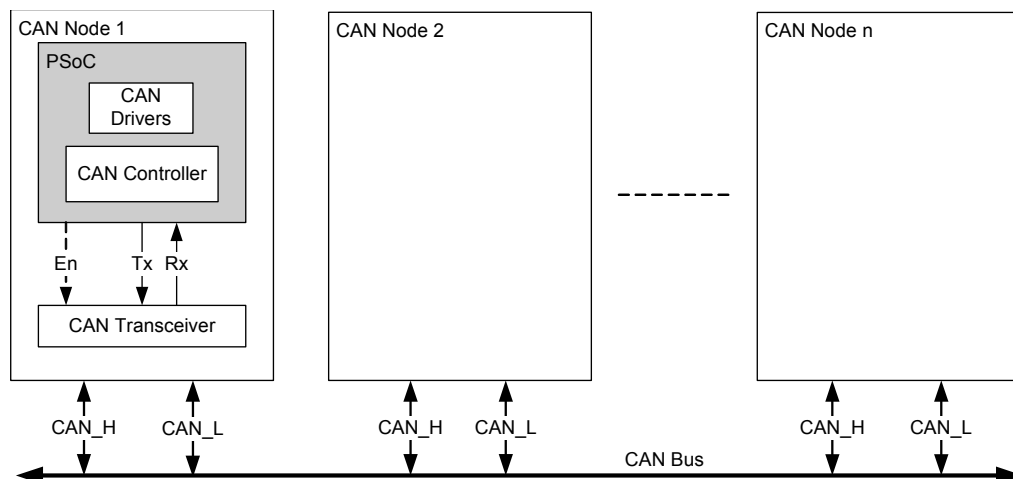
Note

14. GPIOs with opamp outputs are not recommended for use with CapSense.

7.5 CAN

The CAN peripheral is a fully functional controller area network (CAN) supporting communication baud rates up to 1 Mbps. The CAN controller implements the CAN2.0A and CAN2.0B specifications as defined in the Bosch specification and conforms to the ISO-11898-1 standard. The CAN protocol was originally designed for automotive applications with a focus on a high level of fault detection. This ensures high communication reliability at a low cost. Because of its success in automotive applications, CAN is used as a standard communication protocol for motion oriented machine control networks (CANOpen) and factory automation applications (DeviceNet). The CAN controller features allow the efficient implementation of higher level protocols without affecting the performance of the microcontroller CPU. Full configuration support is provided in PSoC Creator.

Figure 7-14. CAN Bus System Implementation



7.5.1 CAN Features

- CAN2.0A/B protocol implementation – ISO 11898 compliant
 - Standard and extended frames with up to 8 bytes of data per frame
 - Message filter capabilities
 - Remote Transmission Request (RTR) support
 - Programmable bit rate up to 1 Mbps
- Listen Only mode
- SW readable error counter and indicator
- Sleep mode: Wake the device from sleep with activity on the Rx pin
- Supports two or three wire interface to external transceiver (Tx, Rx, and Enable). The three-wire interface is compatible with the Philips PHY; the PHY is not included on-chip. The three wires can be routed to any I/O
- Enhanced interrupt controller
 - CAN receive and transmit buffers status
 - CAN controller error status including BusOff

- Receive path
 - 16 receive buffers each with its own message filter
 - Enhanced hardware message filter implementation that covers the ID, IDE, and RTR
 - DeviceNet addressing support
 - Multiple receive buffers linkable to build a larger receive message array
 - Automatic transmission request (RTR) response handler
 - Lost received message notification
- Transmit path
 - Eight transmit buffers
 - Programmable transmit priority
 - Round robin
 - Fixed priority
 - Message transmissions abort capability

7.5.2 Software Tools Support

CAN Controller configuration integrated into PSoC Creator:

- CAN Configuration walkthrough with bit timing analyzer
- Receive filter setup

The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

8.1 Analog Routing

The CY8C34 family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

For information on how to make pin selections for optimal analog routing, refer to the application note, [AN58304 - PSoC® 3 and PSoC® 5 - Pin Selection for Analog Designs](#).

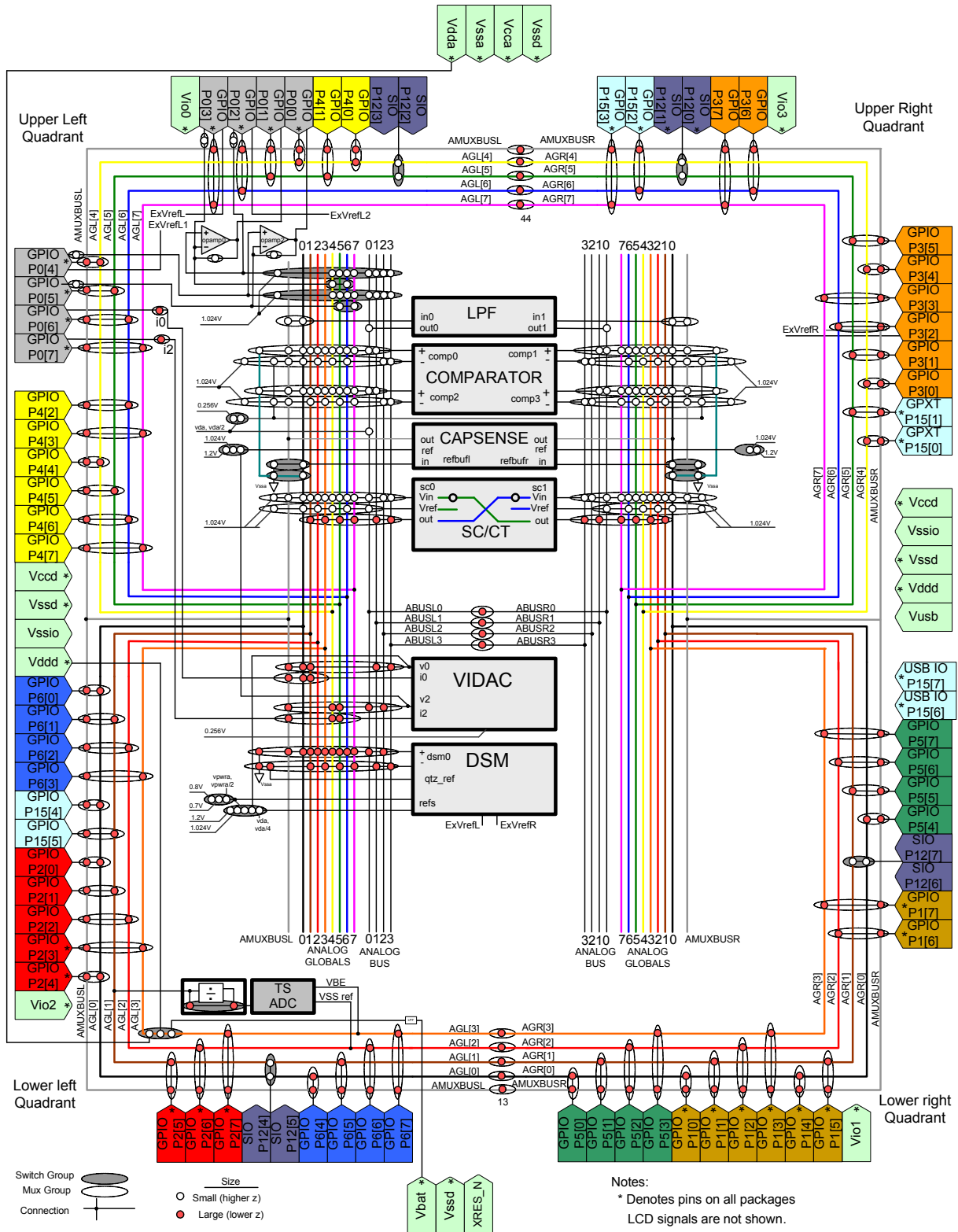
8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- Eight analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the CY8C34 family. The analog routing architecture is divided into four quadrants as shown in [Figure 8-2](#). Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in CY8C34, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in [Figure 8-2](#) on page 53.

Figure 8-2. CY8C34 Analog Interconnect



To preserve detail of this figure, this figure is best viewed with a PDF display program or printed on a 11" × 17" paper.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

8.2.2.4 Multi Sample (Turbo)

The multi sample (turbo) mode operates identical to the Multi-sample mode for resolutions of 8 to 16 bits. For resolutions of 17 to 20 bits, the performance is about four times faster than the multi sample mode, because the ADC is only reset once at the end of conversion.

More information on output formats is provided in the Technical Reference Manual.

8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

8.3 Comparators

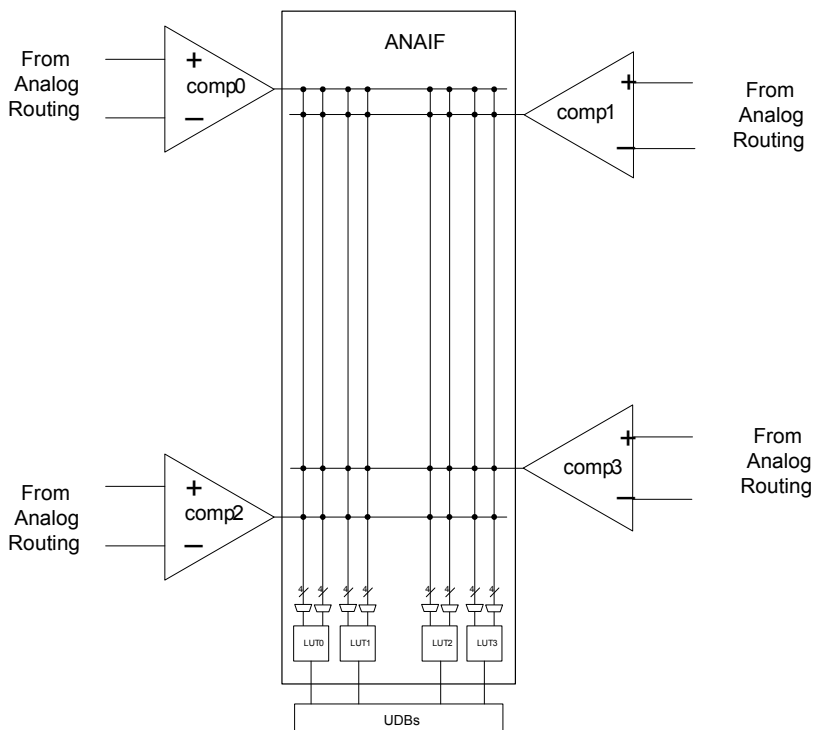
The CY8C34 family of devices contains four comparators in a device. Comparators have these features:

- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (VSSA to VDDA)
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB DSI.

Figure 8-5. Analog Comparator



8.3.2 LUT

The CY8C34 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

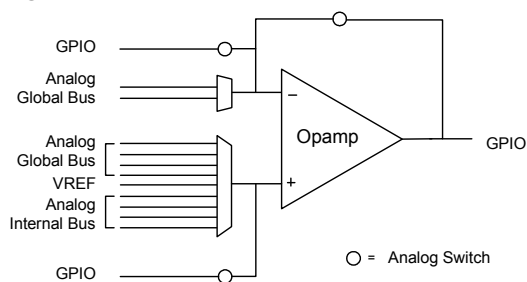
Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	FALSE ('0')
0001b	A AND B
0010b	A AND (NOT B)
0011b	A
0100b	(NOT A) AND B
0101b	B
0110b	A XOR B
0111b	A OR B
1000b	A NOR B
1001b	A XNOR B
1010b	NOT B
1011b	A OR (NOT B)
1100b	NOT A
1101b	(NOT A) OR B
1110b	A NAND B
1111b	TRUE ('1')

8.4 Opamps

The CY8C34 family of devices contain up to two general purpose opamps in a device.

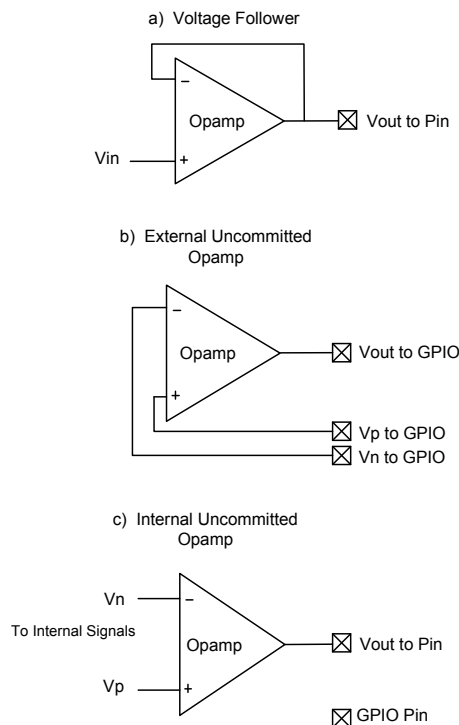
Figure 8-6. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower, or output buffer on external or internal signals.

See Figure 8-7. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-7. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.5 Programmable SC/CT Blocks

The CY8C34 family of devices contains up to two switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- PGA – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 μ A. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

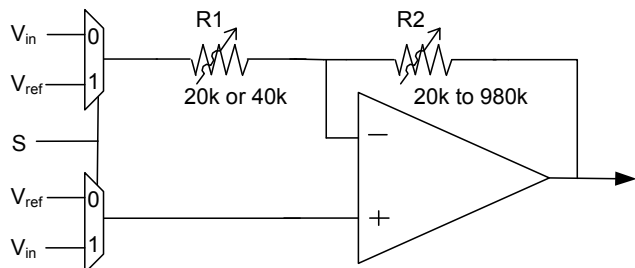
8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-8. The schematic in Figure 8-8 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	5.5 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-8. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

8.5.4 TIA

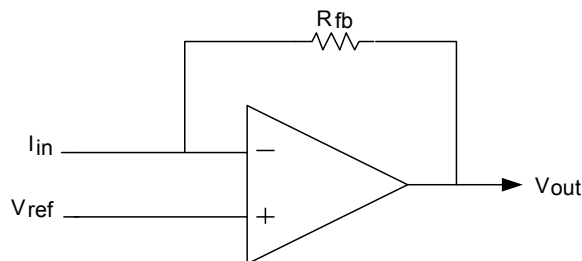
The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in} , the output voltage is $V_{REF} - I_{in} \times R_{fb}$, where V_{REF} is the value placed on the non inverting input. The feedback resistor R_{fb} is programmable between 20 K Ω and 1 M Ω through a configuration register.

Table 8-4 shows the possible values of R_{fb} and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (K Ω)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-9. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

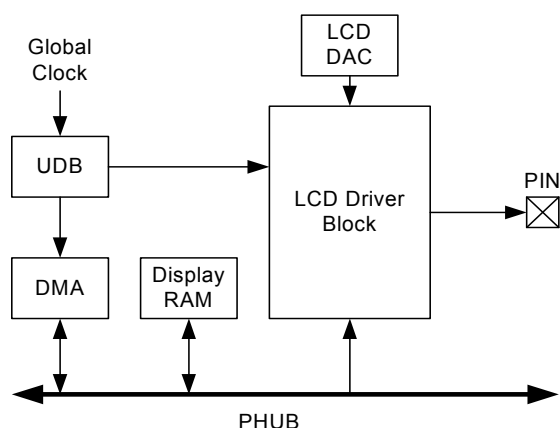
The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C34 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-10. LCD System



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers through the DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.7 CapSense

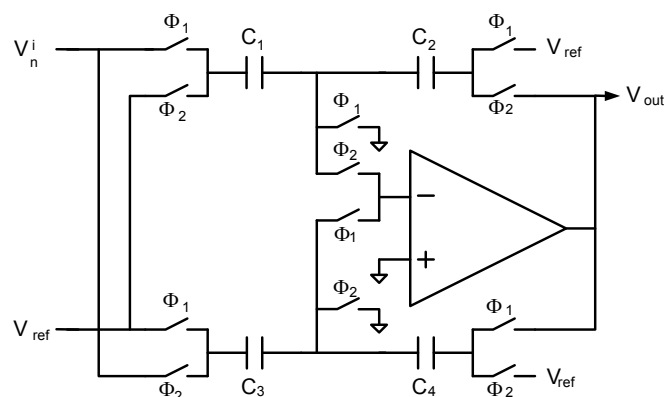
The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.8 Temp Sensor

Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

Figure 8-13. Sample and Hold Topology
(Φ_1 and Φ_2 are opposite phases of a clock)



8.11.1 Down Mixer

The SC/CT block can be used as a mixer to down convert an input signal. This circuit is a high bandwidth passive sample network that can sample input signals up to 14 MHz. This sampled value is then held using the opamp with a maximum clock rate of 4 MHz. The output frequency is at the difference between the input frequency and the highest integer multiple of the Local Oscillator that is less than the input.

8.11.2 First Order Modulator – SC Mode

A first order modulator is constructed by placing the SC/CT block in an integrator mode and using a comparator to provide a 1-bit feedback to the input. Depending on this bit, a reference voltage is either subtracted or added to the input signal. The block output is the output of the comparator and not the integrator in the modulator case. The signal is downshifted and buffered and then processed by a decimator to make a delta-sigma converter or a counter to make an incremental converter. The accuracy of the sampled data from the first-order modulator is determined from several factors.

The main application for this modulator is for a low-frequency ADC with high accuracy. Applications include strain gauges, thermocouples, precision voltage, and current measurement.

9. Programming, Debug Interfaces, Resources

PSoC devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. Three interfaces are available: JTAG, SWD, and SWV. JTAG and SWD support all programming and debug features of the device. JTAG also supports standard JTAG scan chains for board level test and chaining multiple JTAG devices to a single JTAG connection.

For more information on PSoC 3 Programming, refer to the [PSoC® 3 Device Programming Specifications](#).

Complete Debug on Chip (DoC) functionality enables full device debugging in the final system using the standard production

device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE software provides fully integrated programming and debug support for PSoC devices. The low cost MiniProg3 programmer and debugger is designed to provide full programming and debug support of PSoC devices in conjunction with the PSoC Creator IDE. PSoC JTAG, SWD, and SWV interfaces are fully compatible with industry standard third party tools.

All DOC circuits are disabled by default and can only be enabled in firmware. If not enabled, the only way to reenables them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables DOC. Disabling DOC features, robust flash protection, and hiding custom analog and digital functionality inside the PSoC device provide a level of security not possible with multichip application solutions. Additionally, all device interfaces can be permanently disabled (Device Security) for applications concerned about phishing attacks due to a maliciously reprogrammed device. Permanently disabling interfaces is not recommended in most applications because you cannot access the device later. Because all programming, debug, and test interfaces are disabled when device security is enabled, PSoCs with Device Security enabled may not be returned for failure analysis.

Table 9-1. Debug Configurations

Debug and Trace Configuration	GPIO Pins Used
All debug and trace disabled	0
JTAG	4 or 5
SWD	2
SWV	1
SWD + SWV	3

9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

PSoC 3 has certain timing requirements to be met for entering programming mode through the JTAG interface. Due to these timing requirements, not all standard JTAG programmers, or standard JTAG file formats such as SVF or STAPL, can support PSoC 3 programming. The list of programmers that support PSoC 3 programming is available at <http://www.cypress.com/go/programming>.

The JTAG clock frequency can be up to 14 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit transfers. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as GPIO instead.

11. Electrical Specifications

Specifications are valid for $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ and $T_j \leq 150^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component data sheets for full AC/DC specifications of individual functions. See the [Example Peripherals](#) on page 40 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications ^[17]

Parameter	Description	Conditions	Min	Typ	Max	Units
Tstorag	Storage temperature	Recommended storage temperature is 0°C – 50°C . Exposure to storage temperatures above 125°C for extended periods may affect device reliability	–55	25	125	$^{\circ}\text{C}$
Vdda	Analog supply voltage relative to Vssd		–0.5	–	6	V
Vddd	Digital supply voltage relative to Vssd		–0.5	–	6	V
Vddio	I/O supply voltage relative to Vssd		–0.5	–	6	V
Vcca	Direct analog core voltage input		–0.5	–	1.95	V
Vccd	Direct digital core voltage input		–0.5	–	1.95	V
Vssa	Analog ground voltage		Vssd – 0.5	–	Vssd + 0.5	V
Vgpiol ^[18]	DC input voltage on GPIO	Includes signals sourced by Vdda and routed internal to the pin	Vssd – 0.5	–	Vddio + 0.5	V
Vsio	DC input voltage on SIO	Output disabled	Vssd – 0.5	–	7	V
		Output enabled	Vssd – 0.5	–	6	V
Ivddio ^[19]	Current per Vddio supply pin	–40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	–	–	100	mA
		–40 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$	–	–	40	
I _{GPIO}	GPIO current		–30	–	41	mA
I _{SIO}	SIO current		–49	–	28	mA
I _{USBIO}	USBIO current		–56	–	59	mA
V _{EXTREF}	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current ^[20]		–140	–	140	mA
ESD _{HBM}	Electrostatic discharge voltage, Human body model	V _{SSA} tied to V _{SSD}	2200	–	–	V
		V _{SSA} not tied to V _{SSD}	750	–	–	V
ESD _{CDM}	Electro-static discharge voltage	Charge Device Model	500	–	–	V

Note Usage above the absolute maximum conditions listed in [Table 11-1](#) may cause permanent damage to the device. Exposure to maximum conditions for extended periods of time may affect device reliability. When used below maximum conditions but above normal operating conditions the device may not operate to specification.

Notes

17. Usage above the absolute maximum conditions listed in [Table 11-1](#) may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

18. The Vddio supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin $\leq V_{ddio} \leq V_{dda}$.

19. Maximum value 100 mA of Iddio applies only to -40°C to $+85^{\circ}\text{C}$ range and the limit of Iddio parameter for the -40°C to $+125^{\circ}\text{C}$ range is 40 mA.

20. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ	Max	Units
	Sleep Mode ^[25]						
	CPU OFF RTC = ON (= ECO32K ON, in low power mode) Sleep timer = ON (= ILO ON at 1 kHz) ^[26] WDT = OFF I ² C Wake = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 4.5 V–5.5 V	T = –40 °C	–	1.1	–	μA
			T = 25 °C	–	1.1	–	μA
			T = 85 °C	–	15	–	μA
			T = 125 °C	–	20.3	–	μA
		V _{DD} = V _{DDIO} = 2.7 V–3.6 V	T = –40 °C	–	1	–	μA
			T = 25 °C	–	1	–	μA
			T = 85 °C	–	12	–	μA
			T = 125 °C	–	18.5	–	μA
		V _{CC} = V _{DDIO} = 1.71 V–1.95 V	T = 25 °C	–	2.2	–	μA
			T = 125 °C	–	16.2	–	μA
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I ² C Wake = OFF POR = ON SIO Pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 2.7 V–3.6 V	T = 25 °C	–	2.2	–	μA
	I ² C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON SIO Pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 2.7 V–3.6 V	T = 25 °C	–	2.2	–	μA

Notes

 25. If V_{cc}d and V_{cca} are externally regulated, the voltage difference between V_{cc}d and V_{cca} must be less than 50 mV.

26. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.

Figure 11-24. Delta-sigma ADC IDD vs sps, Range = ± 1.024 V, Continuous Sample Mode, Input Buffer Bypassed

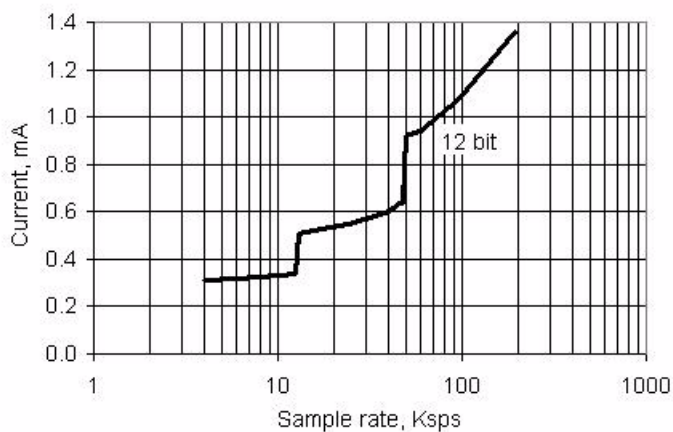


Figure 11-34. IDAC Full Scale Error vs Temperature, Range = 255 μ A, Sink Mode

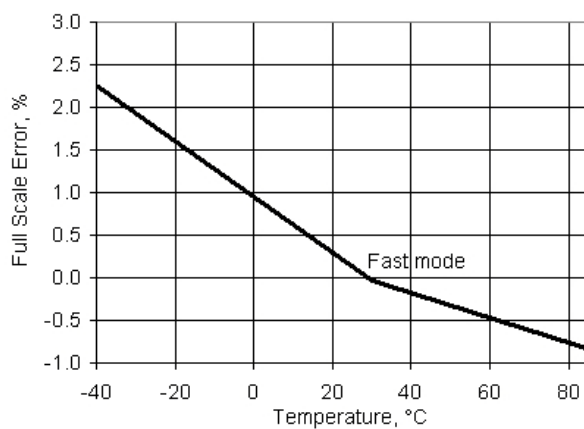


Figure 11-35. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Source Mode

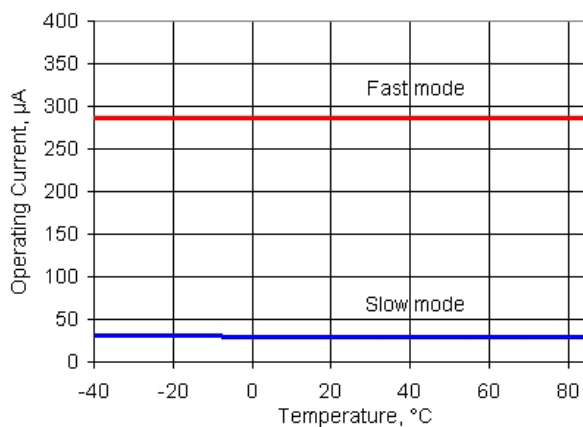


Figure 11-36. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Sink Mode

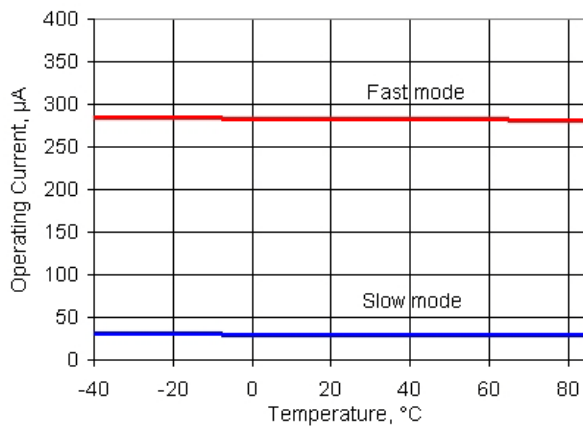


Figure 11-42. VDAC DNL vs Input Code, 1 V Mode

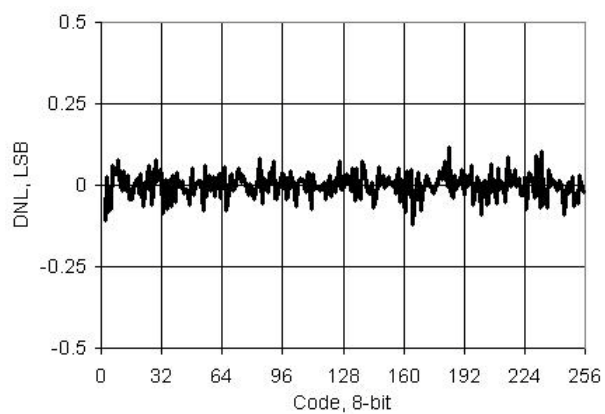


Figure 11-43. VDAC INL vs Temperature, 1 V Mode

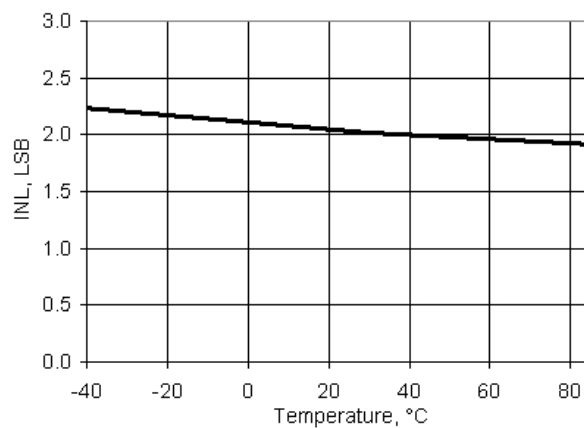
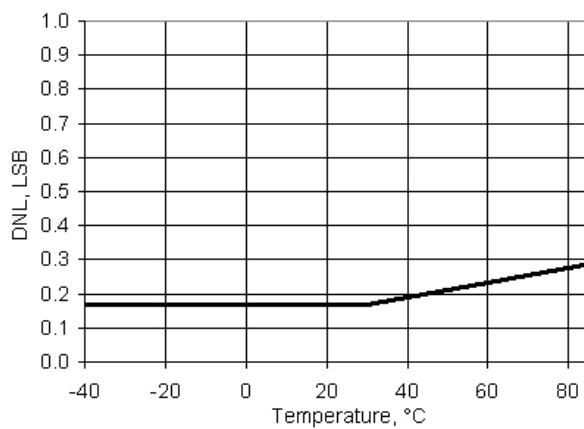


Figure 11-44. VDAC DNL vs Temperature, 1 V Mode



16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
μA	microamperes
μF	microfarads
μH	microhenrys
μs	microseconds
μV	microvolts
μW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts